GigaDevice Semiconductor Inc.

Migration guide from GD32F4xx Series to GD32H73x_H75x Series

Application Notes

AN112

Version 1.1

(Feb. 2026)

Table of Contents

List of Tables

1. Foreword

For designers who use GD32 MCU for product development, due to product and function upgradation, they usually need to replace one MCU with another MCU to add new functions while maintaining existing functions. To accelerate the launch of new products, designers often need to port applications to new MCUs.

This application note aims to help you migrate your applications from GD32F4xx MCU to GD32H73x_75x MCU.

To make better use of this application note, you need to download information of GD32 MCUs such as datasheet, user manual, official example, and development tools from the official website http://www.gd32mcu.com.

Table 1-1. Application series list

GD32F4xx series	GD32H73x_75x Series
GD32F405xx GD32F407xx GD32F425xx GD32F427xx GD32F450xx GD32F470xx	GD32H737xx GD32H757xx GD32H759xx

2. System architecture

GD32F4xx and GD32H73x_75x MCUs have the following differences in system architecture:

1. FPU of GD32H73x_75x MCU is of double-precision, while that of GD32F4xx MCU is of single-precision.
2. GD32H73x_75x MCU is equipped with I-Cache and D-Cache.
3. GD32H73x_75x MCU is equipped with ITCM and DTCM.
4. GD32H73x_75x MCU has 16 MPU regions, while GD32F4xx MCU has 8 MPU regions.
5. GD32H73x_75x MCU has up to 8 FPBs.
6. GD32H73x_75x MCU allows ETM trace.
7. GD32H73x_75x MCU is equipped with 64-bit AXI host.

3. Pin compatibility

To fulfill clients' demands, both GD32F4xx and GD32H73x_75x provide multiple packages. BGA100 pins are not compatible with BGA176 pins. LQFP100 pins are compatible with LQFP144 pins in configuration part. Detailed results are listed in the table below:

Table 3-1. Differences in packages of GD32F4xx series and GD32H73x_75x series

Package	GD32F4xx						GD32H73x_75x		
	GD32F405	GD32F407	GD32F425	GD32F427	GD32F450	GD32F470	GD32H737	GD32H757	GD32H759
LQFP64	√	√	√	√					
LQFP100	√	√	√	√	√	√	√	√	
LQFP144	√	√	√	√	√	√	√	√	
LQFP176							√		
BGA100	√	√	√	√		√		√	√
BGA176		√		√	√	√	√		√

Table3-2. Differences in pin configuration of GD32F4xx series and GD32H73x_75x series (LQFP144)

Pin number	Definition of pins of GD32F4xx series	Definition of pins of GD32H737/759 series
7	PC13-TAMPER-RTC	PC13
28	PC2	PC2_C
29	PC3	PC3_C
71	NC	VCORE
95	VDD	VDD33USB
103	PA11	USBHS0_DP
104	PA12	USBHS0_DM

Table3-3. Differences in pin configuration of GD32F4xx series and GD32H73x_75x series (LQFP100)

Pin number	Definition of pins of GD32F4xx series	Definition of pins of GD32H737/759 series
7	PC13-TAMPER-RTC	PC13
17	PC2	PC2_C
18	PC3	PC3_C
19	VDDA	VSSA
20	VSSA	VREFP
21	VREFP	VDDA
22	VDDA	PA0
24	PA1	PA2
25	PA2	PA3
26	PA3	VSS

Pin number	Definition of pins of GD32F4xx series	Definition of pins of GD32H737/759 series
27	VSS	VDD
28	VDD	PA4
29	PA4	PA5
30	PA5	PA6
31	PA6	PA7
32	PA7	PC4
33	PC4	PC5
34	PC5	PB0
35	PB0	PB1
36	PB1	PB2
37	PB2	PE7
38	PE7	PE8
39	PE8	PE9
40	PE9	PE10
41	PE10	PE11
42	PE11	PE12
43	PE12	PE13
44	PE13	PE14
45	PE14	PE15
46	PE15	PB10
47	PB10	PB11
48	PB11	VCORE
49	VCORE	NC
71	NC	VCORE
95	VDD	VDD33USB
70	PA11	USBHS0_DP
71	PA13	USBHS0_DM

Note: The information above only shows the differences in pin configuration. Even for same pin configuration, it is necessary to check if pins of datasheets have the same functions when porting.

4. Internal resource compatibility

Table 4-1. Overview of internal resource comparison between GD32F4xx series and GD32H73x_75x series gives an overview of resource comparison between GD32F4xx and GD32H73x_75x:

Table 4-1. Overview of internal resource comparison between GD32F4xx series and GD32H73x_75x series

On-chip resources	GD32F4xx	GD32H73x_75x	Compatibility description
Main frequency	168/200/240 MHz	600MHz	-
Core	M4 core	M7 core	-
Flash	512K/1024K/2048K/3072K	1024K/2048K/3840K	-
RAM	192 K/256 K/512 K/768 K	1024K	-
GPTIMER (16 bits)	8	12	Partially compatible
GPTIMER (32 bits)	2	4	Partially compatible
Advanced TIMER (16 bits)	2	2	Partially compatible
Basic TIMER (16 bits)	2	-	Partially compatible
Basic TIMER (32 bits)	-	2	Partially compatible
Basic TIMER (64 bits)	-	2	Partially compatible
WDG	2	2	Fully compatible
RTC	1	1	Compatible
USART	4	6	Partially compatible
UART	2-4	2	Partially compatible
I2C	3	4	Incompatible
SPI	3-6	5-6	Incompatible
CAN	2	2-3	Incompatible
I2S	2	4	Incompatible
USB	FS/HS	HS	Partially compatible
Ethernet	1	2	Partially compatible
DCI	1	1	Partially compatible
CTC	1	1	Fully compatible

On-chip resources	GD32F4xx	GD32H73x_75x	Compatibility description
EXMC	1	1	Partially compatible
PMU	1	1	Partially compatible
EXTI	1	1	Partially compatible
CRC	1	1	Fully compatible
DBG	1	1	Partially compatible
TRNG	1	1	Incompatible
DMA	2	2	Incompatible
ADC	12 bits	14 bits/12 bits	Partially compatible
DAC	2	1	Partially compatible
RTC	1	1	Fully compatible
TLI	1	1	Fully compatible
SDIO	1	2	Partially compatible

Notes: 1. Below are modules exclusively for GD32H73x_75x series: RAMECCMU, EFUSE, TRIGSEL, MDMA, DMAMUX, OSPIM, OSPI, CAU, HAU, RSPDIF, RTDEC, CMP, VREF, TMU, HPDF, FAC, LPDTS, CPDM, EDOUT, HWSEM, and MDIO.

2. Below is a module exclusively for GD32F4xx series: IREF.

5. Differences of peripheral devices

For peripheral devices where GD32F4xx is not compatible with GD32H73x_75x, users may port application codes according to the differences of peripheral devices listed below.

5.1. Power management unit (PMU)

Both GD32F4xx and GD32H73x_75x are equipped with PMUs, which are quite different as listed in the table below:

Table5-1. Differences in PMU specifications of GD32F4xx series and GD32H73x_75x series

PMU	GD32F4xx	GD32H73x_75x
Specifications	■ Three power domains: back-up domain, VDD/VDDA domain, and 1.2 V/0.9 V power domain; ■ Three power-saving modes: sleep mode, deep sleep mode, and standby mode; ■ Built- in low dropout regulator (LDO): LDO outputs voltage for saving consumption. ■ When VDD power supply is turned off, VBAT (battery) supplies power to the back-up domain. ■ They are equipped with the low voltage detector (LVD) to send interruption or event when the voltage is lower than the set threshold.	
	-	VBAT battery charging management, working mode management, voltage output control, low- consumption mode management
	-	USB power regulator
	LVD monitoring	Power supply monitoring: POR/PDR monitoring, BOR monitoring, LVD monitoring, VDDA voltage detection and monitoring (VAVD), VBAK threshold monitoring, and thermal threshold monitoring
		Switch mode power supply low dropout regulator (SMPS low dropout regulator)
	Back-up low dropout (BLDO) regulator of SRAM is exclusively used for backing up SRAM.	-
Application code	Software is partially compatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.2. Reset and clock unit (RCU)

The reset control unit (RCTL) is compatible.

The clock control unit (CCTL) is partially compatible, and some differences are shown as below.

The system frequency of GD32F4xx is up to 240 MHz while GD32H73x_75x is up to 600 MHz.

Table5-2. Differences in RCU specifications of GD32F4xx series and GD32H73x_75x series

<table>
<tr><th colspan="2">RCU</th><th>GD32F4xx</th><th>GD32H73x_75x</th></tr>
<tr><td colspan="2" rowspan="11">Specifications</td><td>4 - 32 MHz high speed crystal oscillator (HXTAL)</td><td>4 - 50 MHz high speed crystal oscillator (HXTAL)</td></tr>
<tr><td>Internal 16 MHz RC oscillator (IRC16M)</td><td>Internal 64 MHz RC oscillator (IRC64M)</td></tr>
<tr><td colspan="2">Internal 48 MHz RC oscillator (IRC48M)</td></tr>
<tr><td colspan="2">Low speed crystal oscillator (LXTAL)</td></tr>
<tr><td colspan="2">Internal 32K RC oscillator (IRC32K)</td></tr>
<tr><td>-</td><td>Low power internal 4 MHz RC oscillator (LPIRC4M)</td></tr>
<tr><td colspan="2">HXTAL clock monitor</td></tr>
<tr><td>-</td><td>LXTAL clock monitor</td></tr>
<tr><td>-</td><td>PLL supports integer and fractional frequency. The fractional frequency can be modified when running.</td></tr>
<tr><td>-</td><td>The peripheral clock can be switched dynamically.</td></tr>
<tr><td rowspan="6">Peripheral clock configuration</td><td>TRNG</td><td colspan="2">CK_48M</td></tr>
<tr><td>USBFS</td><td>CK_48M</td><td>-</td></tr>
<tr><td>USBHS</td><td>CK_48M</td><td>USBHS 48 M clock source
USBHS 60 M clock source</td></tr>
<tr><td>USART</td><td>CK_APB1 or CKAPB2</td><td>CK_APB1 or CKAPB2
CK_AHB
CK_LXTAL
CK_IRC64MDIV</td></tr>
<tr><td>I2C</td><td>CK_APB1</td><td>CK_APB1
CK_PLL2R
CK_HXTAL
CK_LPIRC4M</td></tr>
<tr><td>SPI</td><td>CK_APB1 or CKAPB2</td><td>SPI0 / SPI1 / SPI2:
CK_PLL0Q</td></tr>
</table>

RCU		GD32F4xx	GD32H73x_75x
			CK_PLL1P CK_PLL2P I2S_CKIN CK_PER SPI3 / SPI4: CK_APB2 CK_PLL1Q CK_PLL2Q CK_IRC64MDIV CK_LPIRC4M CK_HXTAL SPI5: CK_APB2 CK_PLL1Q CK_PLL2Q CK_IRC64MDIV CK_LPIRC4M CK_HXTAL
	I2S	PLLI2SR I2S_CKIN	Same as SPI
	OSPI	-	CK_AHB
	LPDTS	-	CK_APB4 CK_LXTAL
	CAN	CK_APB1	CK_HXTAL CK_APB2 CK_APB2 / 2 CK_IRC64MDIV
	RSPDIF	-	CK_PLL0Q CK_PLL1R CK_PLL2R CK_IRC64MDIV
	SAI0/ SAI1	-	CK_PLL0Q CK_PLL1P CK_PLL2P I2S_CKIN CK_PER
	SAI2	-	CK_PLL0Q CK_PLL1P CK_PLL2P I2S_CKIN CK_PER CK_RSPDIF_SYMB
	HPDF	-	Same as SAI0

RCU		GD32F4xx	GD32H73x_75x
	EXMC	CK_AHB	CK_AHB CK_PLL0Q CK_PLL1R CK_PER
	SDIO	CK_48M	CK_PLL0Q CK_PLL1R
	ENET	The input clock is provided by external pins (ENET_TX_CLK / ENET_RX_CLK).	
	TLI	2, 4, 8 or 16 division frequency of PLLSAIR	2, 4, 8 or 16 division frequency of PLL2R
	RTC	LXTAL IRC32K 2 - 31 division frequency of HXTAL	LXTAL IRC32K 2 - 63 division frequency of HXTAL
	FWDGT	IRC32K	
Application code		Software is partially compatible.	

5.3. General purpose and alternate function input/ output interface (GPIO and AFIO)

IO speed options of GPIO module of GD32F4xx include 2M, 25M, 50M, and MAX, while those of GD32H73x_75x include 12M, 60M, 85M, and 100_220M. When porting codes, make sure to modify parameters. The maximum option of H7xx (100M or 220M) depends on the external capacitor connected to the IO pin.

In addition, GD32H73x_75x has the function of filtering input signal to make it more stable. GD32F4xx doesn't have the function.

Table5-3. Differences in GPIO specifications of GD32F4xx series and GD32H73x_75x series

GPIO	GD32F4xx	GD32H73x_75x
Specifications	1. Input/output direction control; 2. Schmitt trigger input function enable control; 3. Each pin has weak pull-up/ pull-down function; 4. Output push-pull/ open-drain enable control; 5. Output set/reset control; 6. External interrupt with programmable trigger edge – using EXTI configuration registers; 7. Analog input/ output configuration; 8. Alternate function input/ output configuration; 9. Port configuration lock; 10. Single cycle toggle output capability.	

	IO speed can be 2M, 25M, 50M, or MAX.	IO speed can be 12M, 60M, 85M, or 100_220M.
	-	It has the function of filtering input signal.
Application code	Software is compatible.	

5.4. Direct memory access controller (DMA)

Table 5-4. Differences in DMA specifications of GD32F4xx series and GD32H73x_75x series

DMA	GD32F4xx	GD32H73x_75x
Specifications	1. Two AHB master interfaces for transferring data, and one AHB slave interface for programming DMA. 2. Support independent single, 4, 8, 16-beat incrementing burst memory and peripheral transfer. 3. Support switch-buffer transmission between peripheral and memory. 4. Software DMA channel priority (low, medium, high, ultra high) and hardware DMA channel priority. 5. Support independent 8, 16, 32-bit memory and peripheral transfer. 6. Support independent fixed and increasing address generation algorithm of memory and peripheral. 7. Support circular transfer mode. 8. Support single-data and multi-data modes, with the maximum FIFO depth of 32-bit. Multi-data mode: Pack/Unpack data when memory transfer width is different from peripheral transfer width. Single-data mode: Read data from source when FIFO is empty and write data to destination when one data has been pushed into FIFO. 9. One separate interrupt per channel with five types of event flags.	
	16 channels (each DMA has 8 channels), up to 8 peripherals per channel with fixed hardware peripheral requests.	16 channels (8 channels of DMA0 and 8 channels of DMA1). Each channel is configurable.
	Support three transfer modes: read from memory and write to peripheral, read from peripheral and write to memory, read from memory and write to memory (only for DMA1).	Support three transfer modes: read from memory and write to peripheral, read from peripheral and write to memory, read from memory and write to memory.
	It is unnecessary to use with DMAMUX.	It is necessary to use with DMAMUX.
Application code	Software is incompatible.	

For specific functions and register configurations, please refer to GD32H73x_75x User Manual.

5.5. Debug (DBG)

GD32H73x_75x has a new function of JTAG security debug, which can be enabled only if the JTAG debug interface locked by keys is unlocked according to the processes. SWD debug is identical between GD32H73x_75x and GD32F4xx, but for GD32H73x_75x, to switch to JTAG debug, it is required to write EFUSE register and it is not allowed to switch from JTAG debug to SWD debug.

5.6. Analog-to-digital converter (ADC)

Both GD32F4xx and GD32H73x_75x are equipped with ADC modules, which are slightly different as listed in the table below:

Table5-5. Differences in ADC specifications of GD32F4xx series and GD32H73x_75x series

ADC	GD32F4xx	GD32H73x_75x
Specifications	Not support differential sampling	Support differential sampling.
	Not support HPDF to manage sampling result	Support HPDF to manage sampling result.
	Support internal trigger and software trigger.	Support TRIGSEL and software trigger.
	Not support asynchronous sampling	It is of dual-clock domain architecture where AHB clock and asynchronous clock are allowed.
	Sampling time is fixed to several values.	Sampling time can be configured flexibly with a maximum value of 642.5 cycles.
	The maximum resolution is 12-bit resolution.	The maximum resolution is 14-bit resolution.
	The maximum clock frequency is 40 Mhz.	The maximum clock frequency is 80 Mhz for ADC2 and 72 Mhz for ADC0 and ADC1.
Application code	Partially compatible	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.7. Digital-to-analog converter (DAC)

On the basis of GD32F4xx, DAC of GD32H73x_75x has new sample and keep mode, output buffer calibration function, and low-power mode, so it is equipped with new calibration register (DAC_CALR), mode control register (DAC_MDCR), sample and keep sample time register 0 (DAC_SKSTR0), sample and keep sample time register 1 (DAC_SKSTR1), sample and keep keep time register (DAC_SKKTR), and sample and keep refresh time register (DAC_SKRTR). For detailed functions and register configuration, please refer to GD32H73x_75x User Manual.

5.8. Real-time clock (RTC)

Both GD32F4xx and GD32H73x_75x are equipped with RTC modules, which are slightly different as listed in the table below:

Table 5-6. Differences in RTC specifications of GD32F4xx series and GD32H73x_75x series

RTC	GD32F4xx	GD32H73x_75x
Specifications	Twenty 32-bit (80 bytes in total) general-purpose and back-up registers	Thirty two 32-bit (128 bytes in total) general-purpose and back-up registers
Application code	Software is compatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.9. Timer (TIMER)

Table5-7. Differences in TIMER specifications of GD32F4xx series and GD32H73x_75x series

TIMER	GD32F4xx	GD32H73x_75x
Specifications	(List advanced TIMER functions, based on which general TIMER functions are reduced.) ■ Selectable clock source: internal clock, internal trigger, external input, and external trigger. ■ Multiple counting modes: up counting, down counting and center-aligned counting. ■ Quadrature decoder: used for motion tracking and determination of both rotation direction and position. ■ Hall sensor function: used for 3-phase motor control. ■ Programmable prescaler: The 16-bit prescaler can be changed when running. ■ Programmable dead time insertion; ■ Auto reload function; ■ Programmable counter repetition function; ■ Single pulse output function; ■ Break input.	

TIMER	GD32F4xx	GD32H73x_75x
	■ Interrupt output and DMA requests: update event, trigger event, compare/capture event, and break input events. ■ Daisy chaining of timer module allows a single timer to start multiple timers. ■ Timer synchronization allows the selected timers to start counting on the same clock cycle. ■ Timer master-slave management	
	Supported 16-bit TIMER: TIMER0/7, TIMER2/3, TIMER8/9, TIMER9/10/12/13, and TIMER5/ 6. Supported 32-bit TIMER: TIMER1/4.	Supported 16-bit TIMER: TIMER0/7, TIMER2/3/30/31, TIMER14/40/41/42/43/44 and TIMER15/16. Supported 32-bit TIMER: TIMER1/4/22/23 and TIMER5/ 6. Supported 64-bit TIMER: TIMER50/51.
	Complementary channel: CHxN (x=0-3), where complementary mode (for complementary output with CHx) is only supported. The advanced TIMER (TIMER0/7) supports the function.	Multi mode channel: MCHx (x=0-3), where independent mode (independent input capture and independent output comparison) and complementary mode (only for complementary output with CHx) are supported. The advanced TIMER (TIMER0/7), L3 TIMER (TIMER14/40/41/42/43/44), and L4 TIMER (TIMER14/40/41/42/43/44) support this function.
	Internal connection of timers can only be achieved with fixed configuration.	Internal connection of timers can be achieved with fixed configuration and by selecting signal from TRIGSEL with ITI14.
	Only support one repetition register TIMERx_CREP whose CREP[7:0] bit-field is 8-bit.	Support two repetition registers TIMERx_CREP0/1. CREP0[7:0] bit-field of the TIMERx_CREP0 register is 8-bit, while CREP1[31:0] bit-field of the TIMERx_CREP1 register is 32-bit: advanced TIMER (TIMER0/7), L3 TIMER (TIMER14/40/41/42/43/44), and L4 TIMER (TIMER15/16).
	Input break function: BREAK	Input break function: BREAK0 and BREAK1

TIMER	GD32F4xx	GD32H73x_75x
	-	Locked break function
	-	Separate dead time insertion and break function: CHx_O and MCHx_O (x=0-3)
	-	Composite PWM function: advanced TIMER (TIMER0/7), L0 TIMER (TIMER1/2/3/4/22/23/30/31), and L3 TIMER (TIMER14/40/41/42/43/44)
	-	Output match pulse select function: advanced TIMER (TIMER0/7), L0 TIMER (TIMER1/2/3/4/22/23/30/31), and L3 TIMER (TIMER14/40/41/42/43/44)
	-	Delayable single pulse mode: advanced TIMER (TIMER0/7), L0 TIMER (TIMER1/2/3/4/22/23/30/31), and L3 TIMER (TIMER14/40/41/42/43/44)
	-	Non-quadrature decoder: advanced TIMER (TIMER0/7) and L0 TIMER (TIMER1/2/3/4/22/23/30/31)
	-	Quadrature decoder signal detection: signal jump detection and disconnection detection
	-	UPIF bit backup function
	-	Restart + event mode
Application code	Software is incompatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.10. Universal synchronous/asynchronous receiver/transmitter (USART)

Table 5-8. Differences in USART specifications of GD32F4xx series and GD32H73x_75x series

USART	GD32F4xx	GD32H73x_75x
USART/ UART	USART0 / 1 / 2 / 5 UART3 / 4 / 6 / 7	
Clock	Single clock domain	Dual clock domain
Baud rate	Up to 15 MBits/s	Up to 37.5 MBits/s;

USART	GD32F4xx	GD32H73x_75x
Programmable data width	8/9 bits	7 / 8 / 9 / 10 bits
Specifications	■ NRZ standard format ■ Full-duplex asynchronous communication ■ Half-duplex single wire communication ■ Programmable baud-rate generator ■ Fully programmable serial port feature ■ Separate enable bits for transmitter and receiver ■ Hardware modem operations (CTS / RTS) ■ LIN break generation and detection ■ IrDA supported ■ Synchronous mode and transmitter clock output for synchronous transmission ■ ISO 7816-3 compliant smartcard interface ■ Multiprocessor communication ■ Support DMA mode	
	-	Swappable Tx / Rx pin Support enabling RS485 driver. Support ModBus communication Support receive/transmit FIFO functions. USART can be waked from the deep sleep mode.
Application code	Software is incompatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.11. Inter-integrated circuit (I2C) bus interface

Both GD32F4xx and GD32H73x_75x are equipped with I2C interfaces for communication between MCU and external device, which are quite different as listed in the table below:

Table 5-9. Differences in I2C specifications of GD32F4xx series and GD32H73x_75x series

I2C	GD32F4xx	GD32H73x_75x
Specifications	■ Addressing mode: 7-bit and 10-bit addressing and general call addressing; ■ Support DMA mode; ■ Optional PEC generation and check; ■ Standard mode (up to 100 kHz) and fast mode (up to 400 kHz); ■ Multi-master mode capability. ■ Configurable SCL stretching in slave mode.	
	-	Fast mode plus (1 MHz)

I2C	GD32F4xx	GD32H73x_75x
	-	Programmable setup and hold time
	Compatible with SMBus2.0 and PMBus	Compatible with SMBus3.0and PMBus1.3
	SAM_V mode	-
	Support digital and analog noise filters.	Support programmable digital and analog noise filters.
	-	Wakeup from sleep mode and Deep-sleep mode on I2C address match.
Application code	Software is incompatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.12. Serial peripheral interface/inter-IC sound interface (SPI/I2S)

Both GD32F4xx and GD32H73x_75x are equipped with SPI/I2S interfaces for communication between MCU and external device, which are quite different as listed in the table below:

Table 5-10. Differences in SPI specifications of GD32F4xx series and GD32H73x_75x series

SPI	GD32F4xx	GD32H73x_75x
Specifications	■ Master-slave operation in full duplex and simplex modes; ■ Hardware CRC calculation, transmission, and verification; ■ Transmission and receiving can be achieved in the DMA mode. ■ Support SPI TI mode. ■ Quad-SPI configuration available in master mode. ■ Software and hardware NSS management; ■ Bit order can be LSB first or MSB first.	
	16-bit-wide separate transmit and receive buffers	32-bit-wide separate transmit and receive buffers
	8-bit or 16-bit data frame size	4-bit to 32-bit data frame size
	-	MOSI and MISO pin switch alternate function
	-	Protect configurations and settings
	-	Multi-master and multi-slave mode
	-	Both the minimum delay between data frames and the minimum delay between NSS and data stream are adjustable
	-	Configurable FIFO thresholds

SPI	GD32F4xx	GD32H73x_75x
	-	The underrun condition is configurable in the slave mode
Application code	Software is incompatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

Table5-11. Differences in I2S specifications of GD32F4xx series and GD32H73x_75x series

I2S	GD32F4xx	GD32H73x_75x
Specifications	■ Master or slave operation for transmission/reception; ■ Four I2S standards supported: Phillips, MSB justified, LSB justified and PCM standard. ■ Data length can be 16 bits, 24 bits, or 32 bits. ■ Channel length can be 16 bits or 32 bits. ■ Audio sample frequency can be 8 kHz to 192 kHz using I2S clock divider. ■ Programmable idle state clock polarity; ■ The master clock (MCK) can be output. ■ Transmission and reception can be achieved with DMA function. ■ Bit order can be LSB first or MSB first.	
	16-bit-wide separate transmit and receive buffers	32-bit-wide separate transmit and receive buffers
		Separate transmit and receive 32-bit FIFO
	Support full duplex mode	
		Error signal to improve reliability: underrun, overrun, and frame format errors
Application code	Software is incompatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.13. Digital camera interface (DCI)

DCIs of GD32H73x_75x and GD32F4xx series are slightly different as shown in the table below:

Table5-12. Differences in DCI specifications of GD32F4xx series and GD32H73x_75x series

DCI	GD32F4xx	GD32H73x_75x
Specifications	■ Capture of digital videos and images; ■ Support 8-bit, 10-bit, 12-bit, or 14-bit parallel interface. ■ High-efficiency transmission with DMA;	

DCI	GD32F4xx	GD32H73x_75x
	■ Support video and image clipping. ■ Support different pixel digital encoding formats like YCbCr422/RGB565/YUV420/and Bayer. ■ Support JPEG compression format. ■ Support embedded code synchronization and hardware synchronization.	
	Digital sensor interface	CCIR656 video interface and digital sensor interface
	-	Interlaced scanning mode
	-	Progressive scanning mode
	-	CCIR656 code error correction
Application code	Software is partially compatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.14. SDIO interface (SDIO)

SDIOs of GD32H73x_75x series and GD32F4xx series are quite different. SDIO of GD32H73x_75x is of brand-new design, particularly with updates in support card protocols which dramatically improve reading and writing speed of control cards. Detailed comparative differences are listed in the table below.

Table 5-13. Differences in SDIO specifications of GD32F4xx series and GD32H73x_75x series

SDIO	GD32F4xx	GD32H73x_75x
Specifications	■ Full support for Multimedia Card System Specification Version 4.2 (and previous versions) Card; ■ Full support for SD Memory Card Specifications Version 2.0; ■ Full support for SD I/O Card Specification Version 2.0 card and two different data bus modes: 1-bit (default) and 4-bit; ■ Support interrupt and DMA requests. ■ Maximum 8-bit data transfer mode.	
	There is only one SDIO.	There are two SDIOs (SDIO0 and SDIO1). SDIO0 can work in UHS-I but SDIO1 can not work in UHS-I.
	-	Support eMMC protocol 4.51 in five data bus modes: 1-bit (default), 4-bit (including SDR and DDR), and 8-bit (including SDR and DDR).
	-	Full support for SD Memory Card Specifications Version 3.0.

SDIO	GD32F4xx	GD32H73x_75x
	-	Full support for SD I/O Card Specification Version 3.0 and three different data bus modes: 1-bit (default) and 4-bit (SDR/DDR).
	Maximum 48 Mhz data transfer frequency	Maximum 104 Mhz data transfer frequency
	-	Data transfer can be achieved with DDR.
	Full support for CE-ATA digital protocol Version 1.1.	-
	-	Three internal clocks can be selected as the receive clock. There are directional signal lines for commands and data. CPDM module can be used for tuning of data sampling points. 1.8 V voltage can be switched.
	-	Three internal trigger lines are supported. Requests can be sent directly to MDMA to achieve continuous transmission operation without CPU intervention operation.
	-	There is internal DMA (IDMA) which can be in 8-beat burst transfer mode and provides two optional configurations of buffer channel.
Application code	Software is partially compatible.	

5.15. Controller area network (CAN)

The CANs of GD32H73x_75xseries and GD32F4xx series are quite different. CAN is a brand new design for the GD32H73x_75x series with flexible mailbox configuration system so that it can support filtering more identifiers. Detailed comparative differences are listed in the table below.

Table 5-14. Differences in CAN specifications of GD32F4xx series and GD32H73x_75x

series

CAN	GD32F4xx	GD32H73x_75x
Specifications	■ Support CAN bus protocol 2.0A/B. ■ Support CAN regular frame with a maximum of 8-byte data and the maximum communication baud rate of 1 Mbit/s. ■ Support transmit and receive timestamps.	
	Not support CAN-FD frame;	Support ISO11898-1:2015 and BOSCH CAN-FD specifications. Maximum communication baud rate of CAN-FD frame is 8 Mbit/s.
	3 transmit mailboxes	When each mailbox is configured as 8-byte data, a maximum of 32 mailboxes can be flexibly configured as transmit or receive mailboxes.
	Two receiving FIFOs with a capacity of 3 frames	Rx FIFO up to 6 frames capacity, with DMA supported
	Support four communication modes: normal mode, loopback mode, silent loopback mode, and silent mode.	Support four communication modes: normal mode, stop mode, silent loopback mode, and monitoring mode.
	Support one power-saving mode: sleep working mode.	Support two power-saving modes: CAN_Disable mode and virtual networking mode.
	Not support wake-up function.	Support two ways to awake MCU from pretended networking mode: matching awakening and overdue awakening.
	CAN0 and CAN1 share 28 filters.	Each CAN has following filters: One public filter register for receive mailboxes; One public filter register for receive FIFOs, 32 private filter registers for receive mailboxes or receive FIFO;
	Filtering function: Maximumly support 56 extended identifiers in 32-bit list mode. Maximumly support 112 extended identifiers in 16-bit list mode.	Filtering function: (receive FIFO) With the identifier filtering function, the receive FIFO can maximumly filter104 extended identifiers, 208 standard identifiers, or 8 bits of 416 identifiers.

<table>
<tr><th>CAN</th><th>GD32F4xx</th><th>GD32H73x_75x</th></tr>
<tr><td>Application code</td><td colspan="2">Software is incompatible.</td></tr>
</table>

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.16. Universal serial bus high-speed interface (USBHS)

USBHSs of GD32H73x_75x series and GD32F4xx series are slightly different. For detailed contrast differences, please refer to the table below.

Table5-15. Differences in USBHS specifications of GD32F4xx series and GD32H73x_75x series

<table>
<tr><th>USBHS</th><th>GD32F4xx</th><th>GD32H73x_75x</th></tr>
<tr><td rowspan="2">Specifications</td><td colspan="2">■ Support USB2.0 high-speed (480 Mb/s)/full-speed (12Mb/s)/low-speed (1.5 Mb/s) host mode.
■ Support USB2.0 high-speed (480Mb/s)/full-speed (12Mb/s) device mode.
■ Support OTG protocol that follows HNP (host negotiation protocol) and SRP (session request protocol).
■ Support all four transfer methods: control transfer, bulk transfer, interrupt transfer, and synchronous transfer.
■ Support high-bandwidth interrupt transfer and synchronous transfer.
■ In the host mode, the USB transaction scheduler is included to effectively handle the USB transaction request.
■ Include one 4 KB FIFO RAM.
■ In the host mode, two transmit FIFOs (cyclic transmit FIFO and non-cyclic transmit FIFO) and one receive FIFO (shared by all channels) are included.
■ In the host mode, if operating in the high speed mode, PING protocol is supported.
■ In the device mode, remote wake-up function is supported.
■ One USB PHY that follows USB OTG protocol is included.
■ One built-in DMA scheduler and engine are included. Data copying can be executed for each application request between USBHS and the system.
■ In the host mode, the time interval of SOF can be adjusted dynamically.
■ SOF pulse can be output to PAD.
■ The ID pin level and VBUS voltage can be detected.
■ In the host mode or OTG A device mode, external parts are required to supply power to connected USB device.</td></tr>
<tr><td>There is only one USBHS.</td><td>There are two USBHSs.</td></tr>
</table>

USBHS	GD32F4xx	GD32H73x_75x
	In the host mode, 12 channels are supported.	In the host mode, 16 channels are supported.
	In the device mode, 6 OUT endpoints and 6 IN endpoints are supported.	In the device mode, 8 OUT endpoints and 8 IN endpoints are supported.
	In the device mode, 6 transmit FIFOs (there is one transmit FIFO at each IN endpoint) and one receive FIFO (shared by all OUT endpoints) are included.	In the device mode, 8 transmit FIFOs (there is one transmit FIFO at each IN endpoint) and one receive FIFO (shared by all OUT endpoints) are included.
	External high-speed PHY is only supported.	Built-in high-speed PHY and external high-speed PHY are supported.
	-	Battery changing detection (BCD) specified in the battery charging specification 1.2 is supported.
	-	Additional detection protocol (ADP) specified in USB OTG supplementary protocol 2.0 is supported.
	-	Link power management (LPM) specified in the USB2.0 link layer power management appendix and USB2.0 engineering modification notice errata is supported.
Application code	Software is partially compatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.17. Flash memory controller (FMC)

Table 5-16. Differences in FMC specifications of GD32F4xx series and GD32H73x_75x series

FMC	GD32F4xx	GD32H73x_75x
Specifications	■ Option bytes are uploaded to the option byte control registers on every system reset. ■ Erase/program protection to prevent unexpected operation. ■ Flash security protection to prevent illegal code/data access.	
	Up to 3072KB of on-chip flash memory.	Up to 3840KB of on-chip flash memory.

FMC	GD32F4xx	GD32H73x_75x
	The region of the MCU executing instructions without waiting time is up to 1024K bytes (in case that flash size is equal to 256K or 512K, all memory has no waiting time). There is long delay when CPU fetches the instructions out of the range.	All memories need waiting time. There is a short delay when CPU fetches the instructions.
	Word/half-word/byte reading operation.	Double-word/word/half-word/byte reading operation.
	Word/half-word/byte programming, 4KB page erase, sector erase and mass erase operation.	Double-word/word programming, 4KB sector erase and mass erase operation.
	2 banks are adopted. Bank0 is used for the first 1024KB and bank1 is for the rest capacity.	-
	512B OTP (One-time program) block and 16B OTP lock block used for user data storage.	-
	30K bytes information block for boot loader.	64K bytes information block for boot loader.
	-	Provides one execute-only dedicated code read protection (DCRP) area.
	-	Provide one secure-access area which is accessible only in secure access mode (SCR mode).
Application code	Software is incompatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.18. External memory controller (EXMC)

Table5-17. Differences in EXMC specifications of GD32F4xx series and GD32H73x_75x series

EXMC	GD32F4xx	GD32H73x_75x
Specifications	■ SRAM ■ PSRAM ■ ROM ■ NOR Flash ■ 8-bit or 16-bit NAND Flash ■ SDRAM	

EXMC	GD32F4xx	GD32H73x_75x
	16-bit PC card	-
	Support two NAND Banks	Support one NAND Bank
	Switch between AMBA protocol and off-chip memory protocols	Switch between AXI protocol and off-chip memory protocols
	-	Support Bank re-mapping function to achieve switch between NOR/PSRAM bank and SDRAM device0.
	EXMC supports 8-bit and 16-bit SRAM.	EXMC only supports 16-bit SRAM.
Application code	Software is partially compatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

5.19. Image processing accelerator (IPA)

Table 5-18. Differences in IPA specifications of GD32F4xx series and GD32H73x_75x series

IPA	GD32F4xx	GD32H73x_75x
Specifications	■ Copy one source image to the destination image. ■ Copy one source image to the destination image with specific pixel format. ■ Convert and blend two source images to the destination image with specific pixel format. ■ Fill the target image area with specific color.	
	The foreground layer image can be in 11 pixel formats.	The foreground layer image can be in 16 pixel formats.
	Three 4-word 32-bit FIFOs	Three 4-double-word 64-bit FIFOs
	-	Support decimal scaling and bilinear scaling.
	-	Support image rotation (by 0°, 90°, 180°, and 270°)
	-	The foreground layer image can be of interlaced input.
Application code	Software is partially compatible.	

For specific functions and register settings, please refer to GD32H73x_75x User Manual.

6. Revision history

Table 6-1. Revision history

Revision No.	Description	Date
1.0	Initial release	April 15, 2023
1.1	Update the series name.	Feb. 11, 2026

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company according to the laws of the People’s Republic of China and other applicable laws. The Company reserves all rights under such laws and no Intellectual Property Rights are transferred (either wholly or partially) or licensed by the Company (either expressly or impliedly) herein. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

To the maximum extent permitted by applicable law, the Company makes no representations or warranties of any kind, express or implied, with regard to the merchantability and the fitness for a particular purpose of the Product, nor does the Company assume any liability arising out of the application or use of any Product. Any information provided in this document is provided only for reference purposes. It is the sole responsibility of the user of this document to determine whether the Product is suitable and fit for its applications and products planned, and properly design, program, and test the functionality and safety of its applications and products planned using the Product. The Product is designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and the Product is not designed or intended for use in (i) safety critical applications such as weapons systems, nuclear facilities, atomic energy controller, combustion controller, aeronautic or aerospace applications, traffic signal instruments, pollution control or hazardous substance management; (ii) life-support systems, other medical equipment or systems (including life support equipment and surgical implants); (iii) automotive applications or environments, including but not limited to applications for active and passive safety of automobiles (regardless of front market or aftermarket), for example, EPS, braking, ADAS (camera/fusion), EMS, TCU, BMS, BSG, TPMS, Airbag, Suspension, DMS, ICMS, Domain, ESC, DCDC, e-clutch, advanced-lighting, etc.. Automobile herein means a vehicle propelled by a self-contained motor, engine or the like, such as, without limitation, cars, trucks, motorcycles, electric cars, and other transportation devices; and/or (iv) other uses where the failure of the device or the Product can reasonably be expected to result in personal injury, death, or severe property or environmental damage (collectively "Unintended Uses"). Customers shall take any and all actions to ensure the Product meets the applicable laws and regulations. The Company is not liable for, in whole or in part, and customers shall hereby release the Company as well as its suppliers and/or distributors from, any claim, damage, or other liability arising from or related to all Unintended Uses of the Product. Customers shall indemnify and hold the Company, and its officers, employees, subsidiaries, affiliates as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Product.

Information in this document is provided solely in connection with the Product. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Product described herein at any time without notice. The Company shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Information in this document supersedes and replaces information previously supplied in any prior versions of this document.