**GigaDevice Semiconductor Inc.** 

**GD32 MCU Resonator-Based Clock Circuits** 

Application Note AN052



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# 1. MCU Clock Source

The clock signal is the basis of the logic circuit in the MCU, and provides a time reference for the state update of the logic circuit. The GD32 MCU can choose to use two different clock signal sources, internal or external. The internal clock source uses the RC oscillator integrated inside the MCU, and the external clock source uses the Pierce oscillator composed of a quartz crystal/ceramic resonator and the MCU internal start-up circuit; or an external active clock source directly provides the MCU with a clock signal. The purpose of this guide is to describe the principles and application considerations of the Pierce oscillator.

Using an external resonator to match the MCU's internal start-up circuit to generate a clock signal can achieve a balance between the clock signal stability and the hardware development cost, so it has been widely used. The schematic diagram of the Pierce oscillator circuit is shown in *Figure 1-1. Pierce Oscillator Schematic*.

#### Figure 1-1. Pierce Oscillator Schematic



R<sub>f</sub>: feedback resistor

Inv: inverter

X: quartz crystal/ceramic resonator

Rd: damping resistor

CL1 & CL2: resonator external matching capacitor

The MCU's internal vibrator, external resonator, and resistor-capacitor form a Pierce oscillator. When the Pierce oscillator circuit meets the Barkhausen criterion, a stable oscillating signal output can be achieved. Usually, the energy transients and noise when the MCU is powered on can provide the specific frequency signal required for the self-oscillation of the Pierce oscillator.



# 2. Resonator Working Principe

Quartz crystal and piezoelectric ceramics are both materials with piezoelectric effect. By adding metal electrodes and packaging to form a resonator, the conversion of mechanical energy and electrical energy can be realized. The characteristics of the piezoelectric effect of the resonator are shown in *Figure 2-1. Resonator Piezoelectric Effect*. When an alternating electric field is applied between the two pins of the resonator, mechanical vibration will be generated, and the mechanical vibration will generate an alternating electric field. The mechanical/electrical equivalent model of the resonator is shown in *Figure 2-2. Piezoelectric Material Equivalent Model (Mechanical/Electrical)*. In general, both the mechanical vibration and the amplitude of the alternating electric field are very small. However, when the frequency of the alternating electric field reaches a certain value, the amplitude of the resonator will suddenly increase, resulting in resonance. This phenomenon is called piezoelectric oscillation. This specific frequency is called the natural frequency or resonant frequency of the resonator.

#### Figure 2-1. Resonator Piezoelectric Effect



Figure 2-2. Piezoelectric Material Equivalent Model (Mechanical/Electrical)



The natural frequency of the resonator is determined by the size and cutting method of the piezoelectric material, and it has high stability (usually the frequency stability of quartz crystal is better than that of piezoelectric ceramics). The quartz crystal/piezoelectric ceramic material is encapsulated to form a resonator. The piezoelectric oscillation equivalent circuit of the resonator is shown in *Figure 2-3. Resonator Electrical Equivalent Model*. Compared with



the original equivalent circuit of the piezoelectric material Introduce static capacitance  $C_0$ . The equivalent parameters  $C_0$ ,  $L_1$ ,  $C_1$ , and  $R_1$  in the electrical equivalent circuit of the resonator are provided by the resonator manufacturer, and the specific values can refer to the corresponding datasheets.

#### Figure 2-3. Resonator Electrical Equivalent Model



 $C_0$ : shunt capacitor, when the resonator does not vibrate, can be equivalent to a plate capacitance  $C_0$ , the value of which depends on the size of the resonator, the electrode area, and the stray capacitance on the package.

L1: The inertia of the mechanical vibration of the resonator is equivalent to the inductance L1.

C1: The elasticity of the resonator is equivalent to the capacitance C1.

R<sub>1</sub>: The friction loss of the resonator vibration is equivalent to the resistance R<sub>1</sub>.

The impedance model of the resonator equivalent circuit is shown in formula (2-1):

$$Z = \frac{\frac{\omega L_1 - 1/\omega C_1}{\omega C_0} \frac{R_1}{j_\omega C_0}}{R_1 + j \left(\omega L_1 - \frac{1}{\omega C_1} - \frac{1}{\omega C_0}\right)}$$
(2-1)

The frequency response characteristics of the resonator impedance are shown in *Figure 2-4. Resonator Impedance Frequency Response Curve*.







When the L<sub>1</sub>, C<sub>1</sub>, and R<sub>1</sub> branches in the equivalent circuit generate series resonance, the branch is purely resistive. The reactance of the entire network at the resonant frequency is equal to R<sub>1</sub> in parallel with C<sub>0</sub>. Since R<sub>1</sub> is much smaller than  $|X_{C_0}|$ , it can be approximated that the resonator is purely resistive, and the equivalent resistance is R<sub>1</sub>. The calculation method of the resonance frequency frs is shown in formula (2-2).

$$f_{rs} = \frac{1}{2\pi\sqrt{L_1C_1}}$$
(2-2)

When  $f < f_{rs}$ , the L<sub>1</sub>, C<sub>1</sub>, and R<sub>1</sub> branches are capacitive, the reactances of C<sub>0</sub> and C<sub>1</sub> are larger and play a leading role, and the impedance of the resonator is capacitive.

When  $f_{rs} < f < f_{rp}$ , the L<sub>1</sub>, C<sub>1</sub>, R<sub>1</sub> branches are inductive, and they are connected in parallel with C<sub>0</sub> to form a parallel resonant circuit. At this time, the overall impedance of the resonator is inductive. As the frequency increases, the resonator impedance at the parallel resonance frequency  $f_{rp}$  It is also purely resistive, and the calculation method of the parallel resonance frequency  $f_{rp}$  is shown in formula (2-3).

$$f_{rp} = f_{rs} \sqrt{1 + \frac{C_1}{C_0}} \ \vec{x} \ f_{rp} = f_{rs} \left(1 + \frac{C_1}{2C_0}\right)$$
(2-3)

Since  $C_1$  is much smaller than  $C_0$ ,  $f_{rs}$  is close to  $f_{rp}$ . The closer the values of  $f_{rs}$  and  $f_{rp}$  are, the narrower the frequency band of the resonator, and the better the frequency selection effect.

When  $f > f_{rs}$ , the impedance of the resonator is mainly determined by C<sub>0</sub>. The resonator impedance is again capacitive.

The resonator in the Pierce oscillator works in the parallel resonance region, and its



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manufacturer adjusts the parallel resonance frequency of the resonator between  $f_{rs}$  and  $f_{rp}$  by giving the recommended parallel load capacitance  $C_L$ , and its equivalent circuit is shown in *Figure 2-5. Equivalent Model of Resonator with Load Capacitor*, the calculation method of the actual oscillation frequency  $f_L$  of the resonator after the load capacitor is connected in parallel is shown in formula (2-4):

#### Figure 2-5. Equivalent Model of Resonator with Load Capacitor



$$f_{L} = f_{rs} \left( 1 + \frac{C_{1}}{2 \times (C_{0} + C_{L})} \right)$$
 (2-4)

Formula (2-4) is to replace  $C_0$  in formula (2-3) with  $C_0+C_L$ . It can be seen from the formula that the oscillator frequency can be adjusted by adjusting the load capacitance  $C_L$ .



# 3. Pierce Oscillator Design

# 3.1. Principle of Pierce Oscillator

Pierce oscillation circuit is a kind of sine wave oscillation circuit. The distinctive feature of sine wave oscillation circuit is to achieve stable and controllable self-excited oscillation by introducing positive feedback and frequency selection network, as shown in *Figure 3-1. Pierce Oscillator Block Diagram*. The positive feedback and frequency selection network together form the feedback loop of the amplifier, as shown in *Figure 3-2. Pierce Oscillator Feedback Network*, and the maintenance of stable oscillation requires the Barkhausen criterion to be satisfied between the forward channel and the feedback loop, as shown in the formula (3-1) and (3-2).

#### Figure 3-1. Pierce Oscillator Block Diagram



#### Figure 3-2. Pierce Oscillator Feedback Network



In the Pierce oscillator circuit, the feedback is realized by connecting the input and output of the inverter through the feedback resistor Rf, so that the inverter works in the linear amplification region to provide the gain required for stable oscillation; The parallel resonance frequency selection feature enables the amplifier to amplify the signal of a specific frequency, and the signal of other frequencies will be attenuated. The phase condition specified in



formula (3-2) is provided by two parts, wherein the inverter part provides a 180-degree phase offset, and the frequency selective network provides another 180-degree phase offset.

# 3.2. Feedback resistor R<sub>f</sub>

In the Pierce oscillation circuit, the feedback resistor  $R_f$  is connected between the input and output terminals of the inverter, so that the inverter  $V_{OUT} = V_{IN} = V_{DD}/2$ , so that the inverter works stably in the linear region to form an inverting amplifier with high gain. If the feedback resistance is too large, the amount of feedback introduced from the output of the inverter to the input will be reduced, which may lead to instability of the static operating point of the amplifier; if the feedback resistance is too small, the gain of the inverting amplifier will be reduced, and the current consumption will be increased at the same time. In addition, the value of the feedback resistor is related to the operating frequency of the oscillator. The typical value range of the  $R_f$  resistor is shown in <u>Table 3-1. Feedback Resistor Rf Value Range</u>.

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Frequency	Feedback resistor range
32.768 kHz	10 to 25 MΩ
1 MHz	5 to 10 MΩ
10 MHz	1 to 5 MΩ
20 MHz	470 kΩ to 5 MΩ

#### Table 3-1. Feedback Resistor R<sub>f</sub> Value Range

Usually, the feedback resistance used in CMOS integrated circuits is between  $100K\Omega$  and  $10M\Omega$  (generally  $1M\Omega$ ), while the feedback resistance used in TTL integrated circuits is between  $1K\Omega$  and  $10K\Omega$  (generally  $4.7K\Omega$ ).

# 3.3. Load capacitor C<sub>L</sub>

The load capacitor plays a crucial role in the stability of the oscillating circuit, and the reasonable matching of the resonator and the load capacitor can make the resonator work stably in the parallel resonance region. Usually the manufacturer of the resonator gives the recommended load capacitance value in the product specification. In practical applications, the external parallel matching capacitor of the resonator is used to achieve the load capacitor value recommended by the specification. The relationship between the load capacitor C<sub>L</sub> and the matching capacitor is shown in formulas (3-3) and (3-4). When calculating the resonator matching capacitors C<sub>L1</sub> and C<sub>L2</sub>, the stray capacitor C<sub>s</sub> brought by the PCB Layout should be comprehensively considered, as shown in <u>Figure 3-3. Pierce Oscillator Parallel Capacitance Distribution</u>.



#### Figure 3-3. Pierce Oscillator Parallel Capacitance Distribution



$$C_{L} = \left(\frac{C_{L1}C_{L2}}{C_{L1}+C_{L2}}\right) + C_{S}$$
(3-3)

Where:

 $C_{L1}$ ,  $C_{L2}$ : Matching capacitors used in the Pierce oscillator circuit.  $C_{L1}$ ,  $C_{L2}$  and the resonator together form a frequency selection network.

 $C_s$ : Stray capacitor. There are stray capacitors on the PCB traces connecting the resonator to the OSC\_IN and OSC\_OUT pins of the MCU, as well as on the MCU package and pins. According to the MCU oscillator frequency, the typical value of the high-speed clock is 10pF, and the typical value of the low-speed clock is 5pF. The actual situation should be based on the actual measured value of the user's PCB board.

 $C_L$ : The load capacitance recommended in the resonator specification. The recommended value of different resonators is different, and the value recommended in the datasheet should be used as a reference standard. The Pierce oscillator circuit is an extension of the capacitive feedback oscillator circuit. There are two parallel capacitors  $C_{L1}$  and  $C_{L2}$  in the frequency selection network of the capacitive feedback oscillator circuit. At the same time, stray capacitance also needs to be considered. Therefore, the  $C_L$  value corresponds to the total value of  $C_{L1}$ ,  $C_{L2}$ , and  $C_s$  in parallel.

In most cases, the matching capacitor takes  $C_{L1}$  equal to  $C_{L2}$ . Therefore, the calculation method of the matching capacitor is shown in formula (3-4).

$$C_{L1} = C_{L2} = 2(C_{L} - C_{S})$$
 (3-4)

### 3.4. Oscillator safety factor OSF

The safety factor is an indicator used to judge that the resonator in the oscillator circuit can start normally and oscillate stably for a long time. The resonator will change its original electrical parameters due to the temperature change of the working environment and the aging caused by long-term operation. The increase of ESR may cause the resonator to stop vibrating, so it is necessary to reserve enough margin for it at the beginning of the circuit design. This margin can be represented by the safety factor  $S_f$ . Generally, when the safety



factor is greater than 5, the oscillator can work stably and reliably. The value range of  $S_f$  and the corresponding safety level are shown in <u>Table 3-2</u>. OSF Recommend Value Range.

OSF	MHz-oscillators	KHz-oscillators
OSF >= 10	Very Safe	Very Safe
5 =< OSF <= 10	Safe	Very Safe
3 =< OSF <= 5	Not Safe	Safe
OSF <= 3	Risky	Not Safe

#### Table 3-2. OSF Recommend Value Range

The measurement method of the safety factor  $S_f$  is to connect an adjustable resistor  $R_s$  in series at one end of the resonator (usually the end connected to OSC\_OUT), measure the maximum value of  $R_s$  when the resonator can maintain oscillation, and calculate  $S_f$  through the formula. During the test, the position of  $R_s$  in the Pierce oscillator is shown in *Figure 3-4. RS Measurement Schematic*. During the test, the default damping resistance  $R_d$  is 0 $\Omega$  or directly short-circuited, and then the resistance of the  $R_s$  potentiometer is increased from small to large until the resonator stops vibrating. Then the resistance value of the potentiometer is reduced in reverse. When the resonator resumes normal oscillation, the resistance value of the potentiometer is the maximum value of  $R_s$ .

#### Figure 3-4. R<sub>S</sub> Measurement Schematic



The calculation method of the safety factor  $S_f$  is shown in formulas (3-5) and (3-6), where the value of  $R_s$  is obtained through actual testing, and the value of ESR is obtained through formula calculation.  $R_s$  and ESR taken together call it negative resistance. The value of  $R_1$  for Equation (3-6) can be set to the maximum value provided in the datasheet when estimating under the most extreme conditions.

$$OSF = \frac{R_{S} + ESR}{ESR}$$
(3-5)

$$\mathsf{ESR}=\mathsf{R}_{1} \times \left(1 + \frac{\mathsf{C}_{0}}{\mathsf{C}_{L}}\right)^{2} \tag{3-6}$$

Where:

ESR: Series Equivalent Resistance of Resonators at Parallel Resonance.

R<sub>1</sub>: The friction loss of the resonator vibration is equivalent to the resistance R<sub>1</sub>.



It should be noted that  $R_s$  only introduces an oscillation circuit in the process of testing the safety factor, and there is no need to add this resistance in practical applications. If the output power of the inverter is too large and the resonator is over-oscillated, the drive level can be controlled by adding a damping resistor  $R_d$ .

## 3.5. Gain Margin GM

The gain margin GM is also an index used to judge that the resonator in the oscillator circuit can start normally and oscillate stably for a long time, which is equivalent to  $S_f$ . It quantifies the oscillator's ability to start and maintain oscillation normally when parameters such as ESR and amplifier transconductance change. The calculation method of GM is shown in formula (3-7), and it is generally recommended that the value of GM is greater than 5 as a relatively safe range.

$$GM = \frac{g_{m}}{\{4 \times ESR \times (2\pi F)^{2} \times (C_{0} + C_{L})^{2}\}}$$
(3-7)

Where:

gm: Oscillator Transconductance

F: Nominal Oscillation Frequency of the Resonator

## 3.6. Drive Level DL

The drive level characterizes the power consumed by the resonator during normal oscillation, and the drive level of the resonator will be clearly specified in its datasheet. In practical applications, it is necessary to meet its power requirements. When the power is too small, the oscillation amplitude of the resonator is small, which will cause the oscillator to fail to start normally; when the power is too large, the mechanical amplitude of the resonator will exceed the allowable range and cause damage to the resonator.

In the oscillator circuit, the power allocated to the resonator is dissipated by the ESR. The driving level of the resonator can be calculated by measuring the ESR and the effective value of the current flowing through the resonator. The calculation methods are as follows: (3-8), (3 -9) shown. The measurement method of the current flowing through the resonator is shown in *Figure 3-5. Schematic Diagram of the Resonator Current Test Method*. The connection at one end of the resonator is passed through the current probe, and the current probe is connected to an oscilloscope or other measurement equipment. The peak-to-peak value I<sub>pp</sub> of the current is measured by the equipment.



#### Figure 3-5. Schematic Diagram of the Resonator Current Test Method



The calculation method of the drive level is shown in formulas (3-8) and (3-9).

$$DL = ESR \times I_{RMS}^2$$
(3-8)

$$I_{\rm RMS} = \frac{I_{\rm PP}}{2\sqrt{2}} \tag{3-9}$$

Where:

 $I_{RMS}$ : Calculate the average value of peak current according to the measured  $I_{pp}$  current value.

## 3.7. Damping resistor R<sub>d</sub>

The damping resistor  $R_d$  is connected across the output end of the inverting amplifier and the passive resonator, and plays two roles. On the one hand, it plays a current limiting role. When the output power of the inverting amplifier is larger than the specified driving level of the resonator, the current limiting resistor  $R_d$  is increased to reduce the power distributed to the resonator in order to avoid over-oscillation of the resonator; On the other hand,  $R_d$  and  $C_{L2}$  form an RC filter circuit, and by adjusting the  $R_d$  value, the cut-off frequency of the RC filter circuit can be set to the oscillation frequency to filter out noise.

The estimated value of  $R_d$  can be calculated using the cut-off frequency calculation formula of the RC filter. It can be known from formulas (3-10) and (3-11) that the resistance value of  $R_d$  is equal to the reactance value of  $C_{L2}$ .

$$F = \frac{1}{2\pi R_{d} C_{L2}}$$
(3-10)

$$R_{d} = \frac{1}{2\pi F C_{L2}}$$
(3-11)

The value of  $C_{L2}$  can be calculated using the formula provided in Section 3.3, and then the value of  $R_d$  can be adjusted until the resonator drive level is met. After the value of  $R_d$  is determined, the GM of the oscillator needs to be recalculated. At this time, the value of ESR in formula (3-6) should be replaced by the value of ESR plus  $R_d$ .



## 3.8. Pullability

The frequency deviation or sensitivity of the resonator is an important indicator of oscillator circuit design, especially for the 32.768KHz oscillator circuit, the clock signal is often used as a time reference in electronic products. There are many factors that cause the frequency deviation of the resonator, including temperature, matching capacitor accuracy, etc., and the frequency deviation caused by temperature changes depends to a large extent on the cutting method and shape of the resonator; the frequency deviation caused by the change of load capacitance is mainly Introduced at the design stage, the load capacitance and the resonator's oscillation frequency are inversely related. The frequency migration caused by the unit is PPM/pF, which is used as the evaluation basis in the design stage.

Pullability<sub>(PPM/pF)</sub> = 
$$\frac{C_1}{2 \times (C_0 + C_L)^2} \times 10^6$$
 (3-12)

$$PPM_{(Budget)} = PPM_{(Crystal)} + C_{LD} \times Pullability_{(Crystal)}$$
(3-13)

Where:

PPM<sub>Budget</sub>: Estimation accuracy of oscillation frequency;

PPM<sub>Crystal</sub>: Resonator PPM accuracy specified in datasheet;

C<sub>LD</sub>: Deviation of Load Capacitor,which comes from deviation of matched capacitanceC<sub>L1</sub>&C<sub>L2</sub> (due to tolerance of matched capacitance value) and stray capacitance C<sub>S</sub>(due to PCB manufacturing process deviation);

Pullability<sub>(Crystal)</sub>: Pullability of the selected crystal.

### 3.9. Start-up time

The definition of oscillator start-up time generally takes the MCU power-on time as the timing starting point, and stops timing when the oscillator's amplitude reaches 90% of the stable oscillation amplitude. There is a power-on reset function inside the GD32 MCU, so the measurement of the start-up time can also be measured from the time point when the oscillation circuit starts to work. The specific measurement standard is selected according to the user's needs.

The length of the oscillator's start-up time is related to the oscillator's nominal frequency, resonator type, inverter drive capability (OSF/GM), etc. In general, the start-up time of ceramic resonators is about 10 times faster than that of quartz crystal resonators. In terms of different oscillation frequencies, the start-up time of a quartz crystal resonator with a frequency of MHz is at the millisecond level, while the start-up time of a 32.768kHz quartz crystal resonator is at the level of seconds. Usually, the reasons for the failure of oscillator start-up include improper matching of matching capacitors resulting in insufficient oscillator loop gain or mismatch between the MCU start-up circuit and the drive level of the resonator.



The ESR size of the resonator affects the start-up time of the oscillator, and the start-up time of a high-ESR resonator is longer than that of a low-ESR resonator.

The size of the resonator load capacitance affects the oscillator start-up time, and increasing the load capacitance will increase the oscillator start-up time.

The drive capability of the inverter affects the start-up time of the oscillator. The greater the drive capability of the inverter, the shorter the start-up time of the oscillator. The drive capability of the inverter in the MCU is based on the  $I_{DD}$  value of the external clock provided in the datasheet.

The quality factor of the resonator affects the start-up time of the oscillator, and the start-up time of a resonator with a high quality factor is longer than that of a resonator with a low quality factor. Generally, the quality factor of ceramic resonators is lower than that of quartz crystal resonators, so the start-up time of ceramic resonators of the same nominal frequency is shorter than that of quartz crystal resonators.



# 4. Resonator Selection and Precautions

## 4.1. Resonator selection steps

**Step 1:** Determine the required resonator type and operating frequency according to the MCU used by the user's product. GD32 MCUs have different requirements for external resonators according to their product lines. The high-speed clock of the MCU usually uses an 8MHz or 25MHz resonator, and the specific resonator operating frequency refers to the recommended value in the data sheet; the low-speed clock recommends using a 32.768KHz resonator, but not all MCUs support the use of external low-speed resonators , the data sheet shall prevail. Considering the accuracy and stability of the clock signal, it is recommended to use a resonator made of quartz crystal; considering the cost, a resonator made of piezoelectric ceramics can be considered.

**Step 2:** Calculate the gain margin GM based on the resonator parameters provided in the resonator's datasheet and the transconductance provided in the MCU datasheet. For the specific calculation method, please refer to Section 3.5. In addition, the safety factor can also be used to evaluate the stable oscillation margin of the resonator. The difference is that the calculation of the safety factor  $S_f$  needs to measure the negative resistance based on the actual PCB board. It is recommended that users use GM for pre-selection during model selection, and then use the prototype to measure  $S_f$  for double verification.

**Step 3:** Calculate the drive level of the resonator. For the specific calculation method, see Section 3.6. The current flowing through the resonator can refer to the current value provided in the MCU data sheet. If the calculated power consumption is greater than the nominal power consumption of the resonator, it is necessary to consider increasing the damping resistance  $R_d$  or re-selection. It should be noted that after increasing the damping resistance  $R_d$ , the values of GM and  $S_f$  need to be recalculated to ensure that the requirements are met. If they do not meet the requirements, they need to be re-selected.

**Step 4:** If you need to calculate the oscillator frequency adjustment, you can refer to the calculation method provided in Section 3.8 for verification. If the verification result does not meet the requirements, it needs to be re-selected.

## 4.2. Resonator precautions

**Item 1:** The clock frequency accuracy of the oscillator circuit is affected by the accuracy of the matching capacitor. In order to obtain a clock signal with better accuracy, it is recommended to use a class I ceramic capacitor (C0G/NP0) with a relatively small temperature coefficient.

**Item 2:** The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces to the OSC\_OUT and OSC\_IN pins due to space constraints in the PCB



layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the matching capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

**Item 3:** If the stray capacitance for the PCB board is estimated by empirical value, there may be an error range that the actual oscillation frequency exceeds the nominal frequency. At this time, the frequency can be adjusted by fine-tuning the matching capacitor. If the actual oscillation frequency is too large, increase the matching capacitor; if the actual oscillation frequency is too small, decrease the matching capacitor. The adjustment is made back and forth so that the oscillation frequency is in the proper range.

**Item 4:** The ESR of the resonator can be taken into consideration when choosing a resonator package. Usually, a resonator with a relatively small package has a smaller crystal size. The smaller the crystal size, the larger the ESR. The increase of ESR will increase the startup time to some extent. In addition, larger matching capacitors also increase the oscillator start-up time.

**Item 5:** The load capacitance of the same brand and the same package resonator usually has different nominal values. The power consumption of the resonator with a relatively large load capacitance is relatively high, but its frequency can be scheduled relatively low; on the contrary, a resonator with a relatively small load capacitance has relatively lower power consumption, but its frequency schedulability is relatively high. For products with more stringent power consumption requirements, it can be one of the factors to consider when selecting a resonator. In addition, the larger load capacitance reduces the oscillator's amplitude.

**Item 6:** The function of the feedback resistor in the Pierce oscillation circuit is very important. When the feedback resistor is integrated inside the MCU (refer to the corresponding data sheet), the normal vibration can usually be achieved without an external feedback resistor. If there is no vibration, you can try to connect an external feedback resistor in parallel. The selection criteria are described in Section 3.2. In addition, the size of the feedback resistance affects the loop gain. Increasing the feedback resistance can increase the loop gain. However, if the feedback resistance is too large, the amount of feedback introduced from the output end of the inverter to the input end will be reduced, resulting in an instablizition of the static operating point of the inverter.

**Item 7:** The 32.768KHz tuning fork type quartz crystal resonator is mostly used for low-speed resonators. This type of resonator should avoid impact and collision during the assembly process, and avoid high temperature during the welding process. For example, the resonator in the DT-26 package usually adopts the practice of soldering the shell and the GND of the PCB together to reduce interference. During the soldering process, the heating time for the resonator becomes longer due to the rapid heat dissipation of the GND plane. This process may cause If the crystal is damaged and does not vibrate, it is recommended to use a hot air pad to connect the GND used to connect the resonator case to the system GND, and the soldering time should not exceed 3 seconds.



**Item 8:** Some GD32 MCU products provide the function of internal drive capability adjustment for the low-speed clock module. Different levels of drive capability can be selected through the configuration register. For the specific usage method, please refer to the corresponding data sheet. It should be noted that the amplitude of the resonator will also increase correspondingly after the driving capacity is improved, and it needs to be set according to the actual needs of the product.

**Note:** Items 1 to 6 apply to both high-speed and low-speed oscillator designs, while Items 7 to 8 require extra attention in the design of low-speed oscillator circuits.



# 5. PCB Layout

The Pierce oscillator circuit is a pure analog circuit, and the anti-interference performance of the analog signal in the hardware system is weaker than that of the digital signal. The frequency accuracy of the Pierce oscillator circuit is easily affected by the spurious parameters of the PCB board, so a good PCB layout can help improve the stability of the circuit. The PCB Layout of the oscillator is shown in *Figure 5-1. Oscillator Layout Example*, the precautions in the PCB layout process for the Pierce oscillator circuit are as follows:

The MCU-based hardware system is generally an electronic system with mixed digital-analog signals. If conditions permit, the grounds of the digital signal and the analog signal are isolated to reduce the interference of the high-order harmonics in the digital signal to the oscillator.

The distance between MCU clock pins, resonators, external matching capacitors and other devices should be as close as possible and far away from high-speed devices. The PCB traces should be as short as possible to reduce the parasitic capacitance caused by the PCB traces.

The OSCIN pin is an input pin that has high impedance and is more sensitive to noise. The PCB traces in this part should be isolated as far as possible from high-frequency digital signals or other noise sources, and can be wrapped with ground rings or ground planes.

The components of the oscillating circuit are placed on the same layer, the signal line should be avoided from changing layers, the matching capacitor of the resonator should be placed as close as possible to the resonator and placed symmetrically, the grounding line of the matching capacitor should be as short as possible, and the ground connection between the two capacitors should be as close as possible.

Other high-speed signal lines and power lines in the system should be arranged as far away as possible from the oscillator. If conditions do not permit, parallel wiring between high-speed signal lines, power lines and oscillator signal lines should be avoided as much as possible to reduce crosstalk.

The ground of the oscillator is not connected to the system ground of the layer where it is located, and the oscillator part is not recommended to be grounded with copper. When the oscillator is protected by a grounding ring, the grounding ring of a single-layer board is connected to the system ground through a short line; for a multi-layer board, the ground of the oscillator part can be connected to the ground layer using a via hole.



Figure 5-1. Oscillator Layout Example







# 6. Revision history

### Table 6-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Apr.22 2022
1.1	Update	Dec.08.2022



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