GigaDevice Semiconductor Inc.

GD32G5xx Hardware Development Guide

Application Note
AN193

Revision 1.0

（Sep. 2024）

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1. Introduction

This document is specifically designed for developers of the 32-bit general-purpose MCU GD32G5xx series based on the Arm® Cortex®-M33 architecture, providing an overall introduction to the hardware development of the GD32G5xx series products, such as power supply, reset, clock, boot mode settings, and download debugging. The purpose of this application note is to enable developers to quickly get started with the GD32G5xx series products and to quickly proceed with product hardware development, saving time reading manuals and accelerating product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32G5xx series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32G5xx series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32G5xx series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32G5xx series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32G5xx series.
6. Reference circuit and PCB Layout design, mainly introduces GD32G5xx series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32G5xx series.

This document also satisfies the minimum system hardware resources used in application development based on GD32G5xx series products.

Table 1-1. Applicable Products

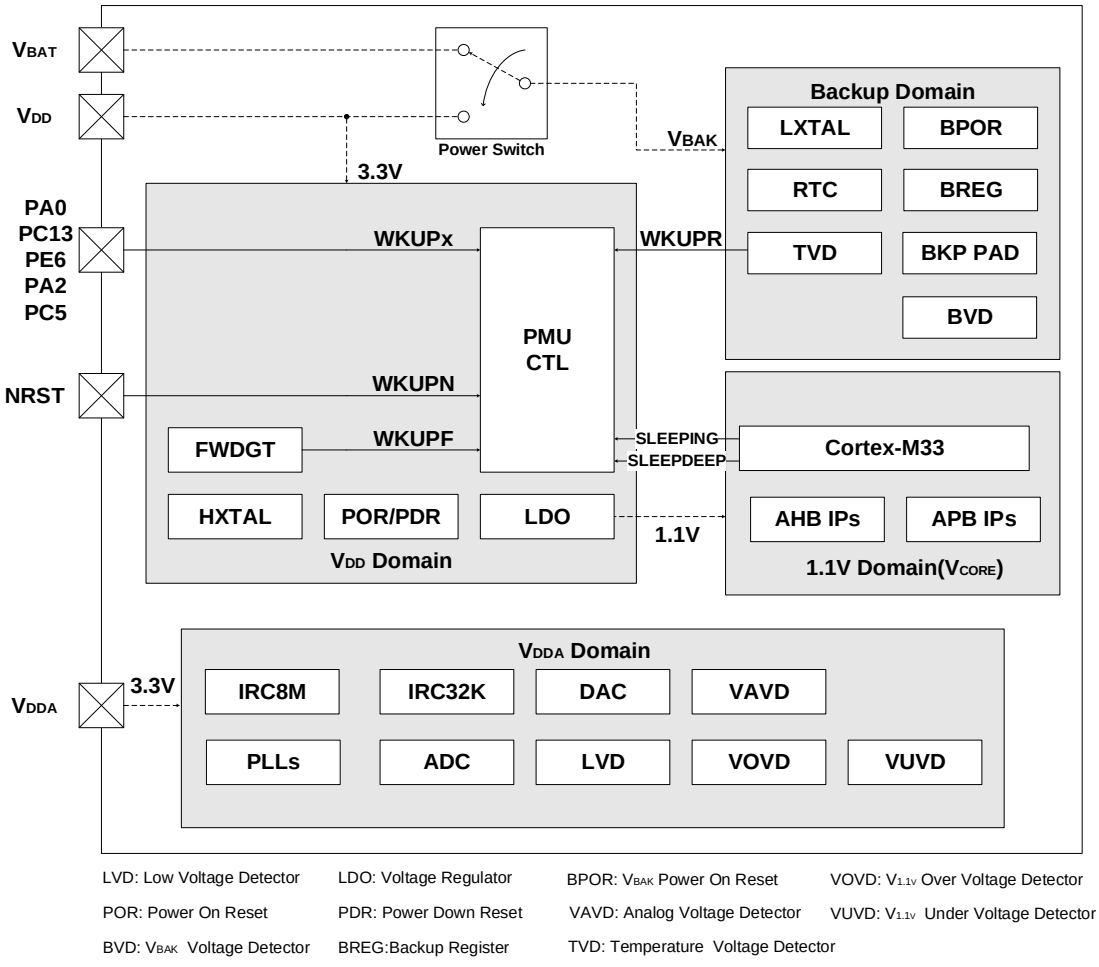
Type	Part Numbers
MCU	GD32G533xx series
	GD32G553xx series

2. Hardware design

2.1. Power supply

The operating voltage range for V_{DD} in the GD32G5xx series is 1.71 V to 3.6 V. As shown in ***Figure 2-1. GD32G5xx series Power supply overview***, the GD32G5xx series devices have three power domains, including the V_{DD}/V_{DDA} domain, the 1.1 V domain, and the backup domain. The V_{DD}/V_{DDA} domain is directly powered by the power supply. The GD32G5xx series incorporates an LDO to supply power to the 1.1 V domain. In the backup domain, there is a power switch that, when the V_{DD} power is turned off, can switch the power supply of the backup domain to the V_{BAT} pin, at which point the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. GD32G5xx series Power supply overview



LVD: Low Voltage Detector
LDO: Voltage Regulator
BPOR: V_{BAK} Power On Reset
VOVD: $V_{1.1V}$ Over Voltage Detector
POR: Power On Reset
PDR: Power Down Reset
VAVD: Analog Voltage Detector
VUVD: $V_{1.1V}$ Under Voltage Detector
BVD: V_{BAK} Voltage Detector
BREG:Backup Register
TVD: Temperature Voltage Detector

2.1.1. Backup domain

The Backup domain is powered by the V_{DD} or the battery power source (V_{BAT}) selected by the internal power switch, and the VBAK pin which drives Backup Domain, power supply for RTC unit, LXTAL oscillator, BPOR and BREG(Backup Register), and three BKP PADs, including

PC13 to PC15. In order to ensure the content of the Backup domain registers and the RTC supply, when V_{DD} supply is shut down, VBAT pin can be connected to an optional standby voltage supplied by a battery or by another source. The power switch is controlled by the power down reset circuit in the V_{DD} / V_{DDA} domain. If no external battery is used in the application, it is recommended to connect VBAT pin externally to VDD pin with a 100nF external ceramic decoupling capacitor.

The Backup domain reset sources includes the Backup domain power-on-reset (BPOR) and the Backup Domain software reset. The BPOR signal forces the device to stay in the reset mode until V_{BAK} is completely powered up. Also the application software can trigger the Backup domain software reset by setting the BKPRST bit in the RCU_BDCTL register to reset the Backup domain.

The clock source of the Real Time Clock (RTC) circuit can be derived from the Internal 32KHz RC oscillator (IRC32K) or the Low Speed Crystal oscillator (LXTAL), or HXTAL clock divided by 32. When V_{DD} is shut down, only LXTAL is valid for RTC. Before entering the power saving mode by executing the WFI/WFE instruction, the Cortex®-M33 can setup the RTC register with an expected alarm time and enable the alarm function and according EXTI lines to achieve the RTC alarm event. After entering the power saving mode for a certain amount of time, the RTC alarm will wake up the device when the time match event occurs.

When the Backup domain is supplied by V_{DD} (V_{BAK} pin is connected to V_{DD}), the following functions are available:

- PC13 can be used as GPIO or RTC function pin.
- PC14 and PC15 can be used as either GPIO or LXTAL Crystal oscillator pins.

When the Backup domain is supplied by V_{BAT} (V_{BAK} pin is connected to V_{BAT}), the following functions are available:

- PC13 can be used as RTC function pin.
- PC14 and PC15 can be used as LXTAL Crystal oscillator pins only.

Note: Since PC13, PC14, PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2MHz when they are in output mode(maximum load: 30pF).

The external V_{BAT} battery can be charged by the V_{DD} through an internal resistor. The charging resistor can be selected by configuring the VCRSEL bit in PMU_CTL2 register. A 5 kOhms resistor or a 1.5 kOhms resistor can be selected for external VBAT battery charing. The external VBAT battery charing is enabled by setting the VCEN bit in PMU_CTL2 register. When in BKP only mode, the V_{BAT} battery charing is disabled by hardware.

Note: In BKP only mode, the V_{DD} loses power and the backup domain is powered by the VBAT pin.

2.1.2. V_{DD} / V_{DDA} domain

The V_{DD} / V_{DDA} power domain includes two parts: V_{DD} domain and V_{DDA} domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two should not exceed 300mV (the internal V_{DDA} and V_{DD} of the chip are connected through a back-to-back diode). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and the corresponding V_{SSA} is connected to V_{SS} through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

The operating voltage range of V_{DDA} can vary due to the specific use scenarios of peripherals such as ADC, DAC, and VREF. For details, refer to ***Table 2-1. VDD / VDDA Operating voltage range***.

Table 2-1. V_{DD} / V_{DDA} Operating voltage range

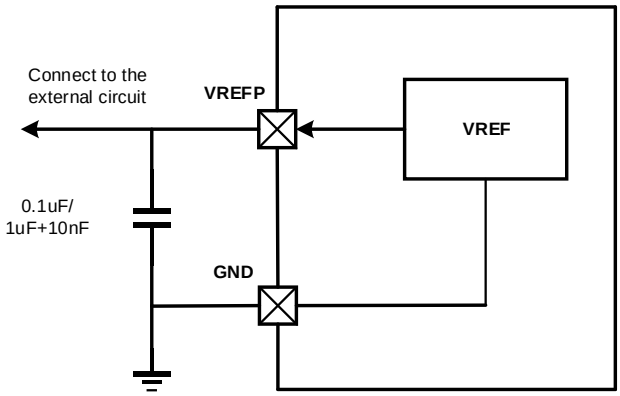
Symbol	Description	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	—	1.71	3.6	V
V_{DDA}	Analog supply voltage	ADC used,f_{ADCMAX} = 50 MHz	1.71	3.6	V
		ADC used,f_{ADCMAX} = 80 MHz	2.4		
		DAC output buffer OFF, DAC_OUT Pin not connected (internal connection only)	1.71		
		DAC work in other mode	1.8		
		VREFBUF used	VREFP + 0.3		

To improve the conversion accuracy of the ADC, independent power supply for V_{DDA} can achieve better characteristics for the analog circuit.

2.1.3. VREF

The GD32G5xx integrates a VREFP pin specifically for the independent power supply of the ADC, which can use an external reference voltage or be directly connected to the VDDA pin. In addition, the GD32G5xx also integrates a VREF module. When this module is enabled, it can be configured to provide a reference voltage out, which can be used as a reference source for on-chip analog circuits. This reference voltage is also output externally through the VREFP pin. When using an accurate internal reference voltage, it is recommended to parallel a bypass capacitor of 0.1 uF (or 1 uF in parallel with 10 nF) at the output, and in the software, it should be enabled before the ADC, as shown in ***Figure 2-2. VREF Connection***

Figure 2-2. VREF Connection

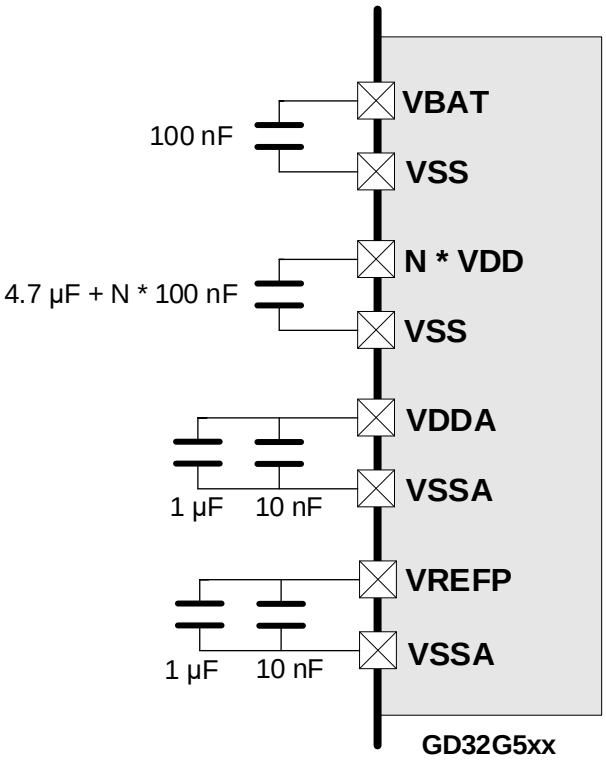


2.1.4. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The V_{DD} pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one V_{DD} needs to be connected to GND with a capacitor of not less than 4.7uF, and other V_{DD} pins are connected to 100nF).
- The V_{DDA} pin must be connected with an external capacitor (10nF + 1uF ceramic capacitor is recommended).
- The V_{REFP} pin can be generated internally or directly connected to V_{DDA}, and a 10nF + 1uF ceramic capacitor should be connected between the V_{REFP} pin and ground.

Figure 2-3. GD32G5xx Recommended Power Supply Design



Note：

1、 All decoupling capacitors must be placed close to the corresponding VDD, VDDA, VBAT, VREFP pins of the chip.

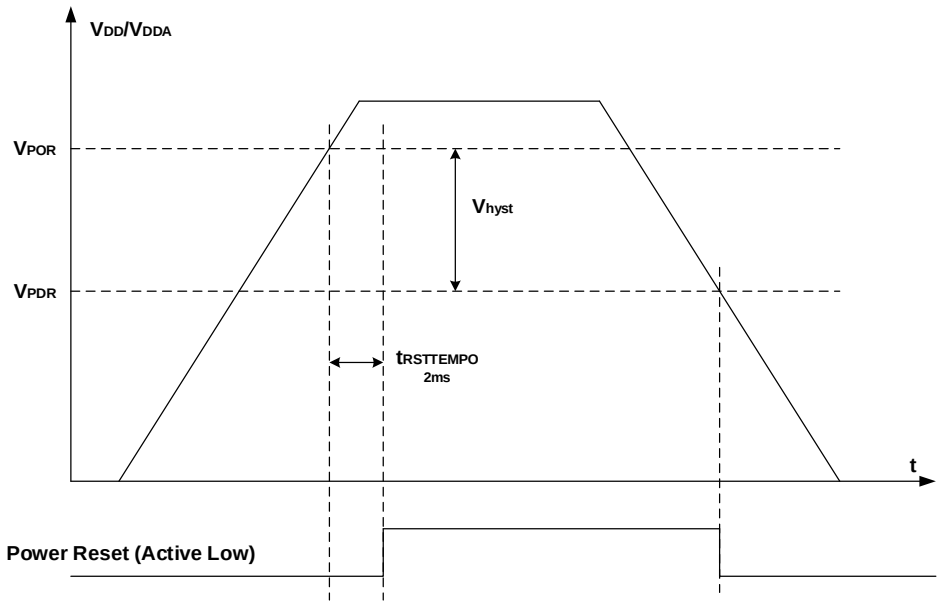
2、 When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.

2.1.5. Reset and power management

GD32G5x3 reset control includes the control of three kinds of reset: power reset, system reset and backup domain reset. The power reset, known as a cold reset, resets the full system except the backup domain. The system reset resets the processor core and peripheral IP components except for the SW-DP controller and the backup domain. The backup domain reset resets the backup domain. These resets can be triggered by an external signal, internal events and the reset generators. More information about these resets will be described in the following sections.

The POR / PDR circuit is implemented to detect V_{DD} / V_{DDA} and generate the power reset signal which resets the whole chip except the Backup domain when the supply voltage is lower than the specified threshold. ***Figure 2-4. Waveform of the POR/PDR*** shows the relationship between the supply voltage and the power reset signal. V_{POR} indicates the threshold of power on reset, with a typical value of 1.63V, while V_{PDR} means the threshold of power down reset, with a typical value of 1.61V. The hysteresis voltage (V_{hyst}) is around 20 mV.

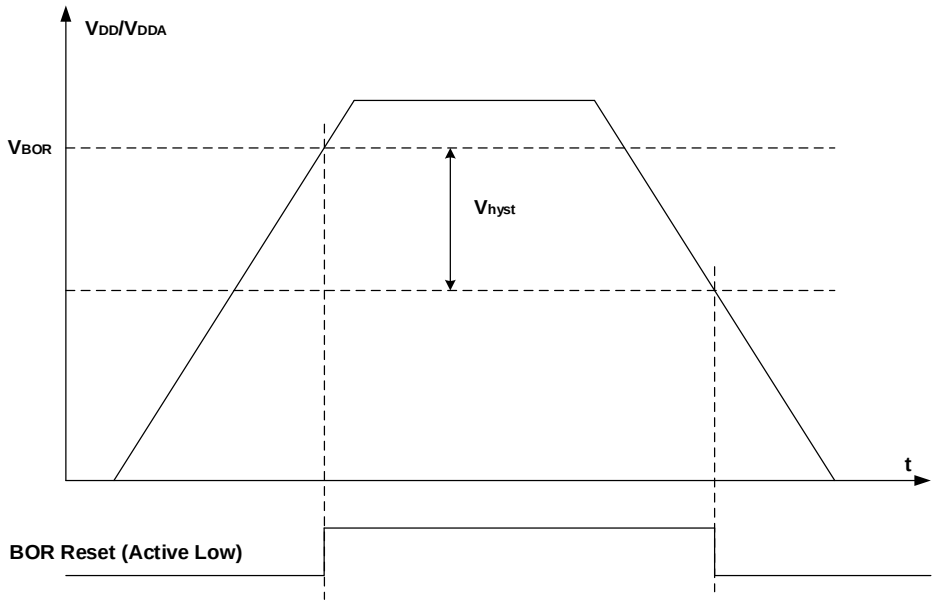
Figure 2-4. Waveform of the POR/PDR



The BOR circuit is used to detect V_{DD}/V_{DDA} and generate the power reset signal which resets the whole chip except the Backup domain when the BOR_TH bits in option bytes is not 0b11 and the supply voltage is lower than the specified threshold which defined in the BOR_TH

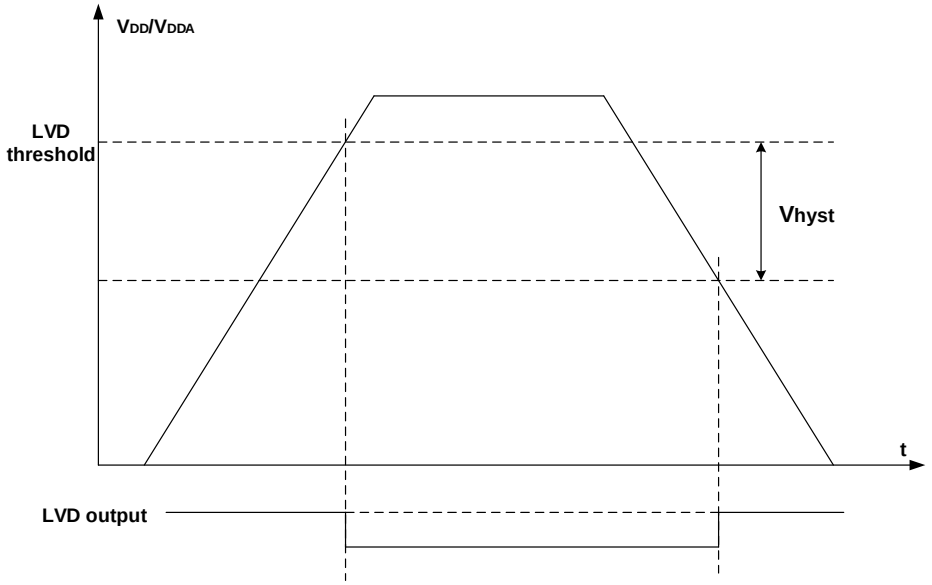
bits in option bytes. Notice that the POR/PDR circuit is always implemented regardless of BOR_TH bits in option bytes is 0b11 or not. ***Figure 2-5. Waveform of the BOR*** shows the relationship between the supply voltage and the BOR reset signal. V_{BOR}, which defined in the BOR_TH bits in option bytes, indicates the threshold of BOR on reset.The Vhyst is 100mV.

Figure 2-5. Waveform of the BOR



The LVD is used to detect whether the V_{DD}/V_{DDA} supply voltage is lower than a programmed threshold selected by the LVDT[2:0] bits in the Power control register(PMU_CTL0). The LVD is enabled by setting the LVDEN bit, and LVDF bit, which in PMU_CS, indicates if V_{DD}/V_{DDA} is higher or lower than the LVD threshold. This event is internally connected to the EXTI line 16 and can generate an interrupt if it is enabled through the EXTI registers. ***Figure 2-6. Waveform of the LVD threshold*** shows the relationship between the LVD threshold and the LVD output (LVD interrupt signal depends on EXTI line 16 rising or falling edge configuration). The following figure shows the relationship between the supply voltage and the LVD signal.

Figure 2-6. Waveform of the LVD threshold



The MCU reset source can be searched by the register RCU_RSTSCK. This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register:

Figure 2-7. The RCU_RSTSCK register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPRSTF	WWDGTRSTF	FWDGTRSTF	SWRSTF	PORRSTF	EPRSTF	BORRSTF	RSTFC	OBLRST	Reserved						
r	r	r	r	r	r	r	rw	r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														IRC32KSTB	IRC32KEN
														r	rw

MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20μs. To prevent a false trigger reset, the NRST pin is recommended to place a capacitor (typically 100nF).

Figure 2-8. System Reset Circuit

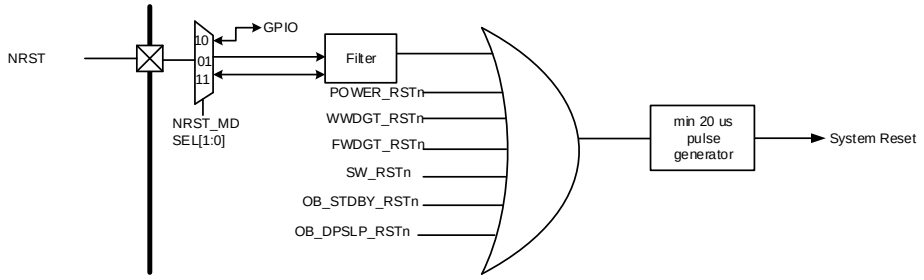
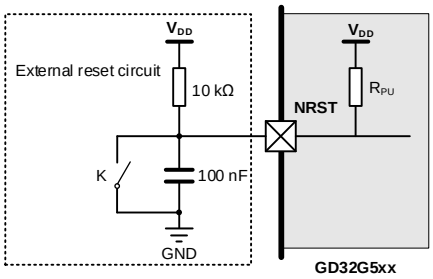


Figure 2-9. Recommend External Reset Circuit



Note:

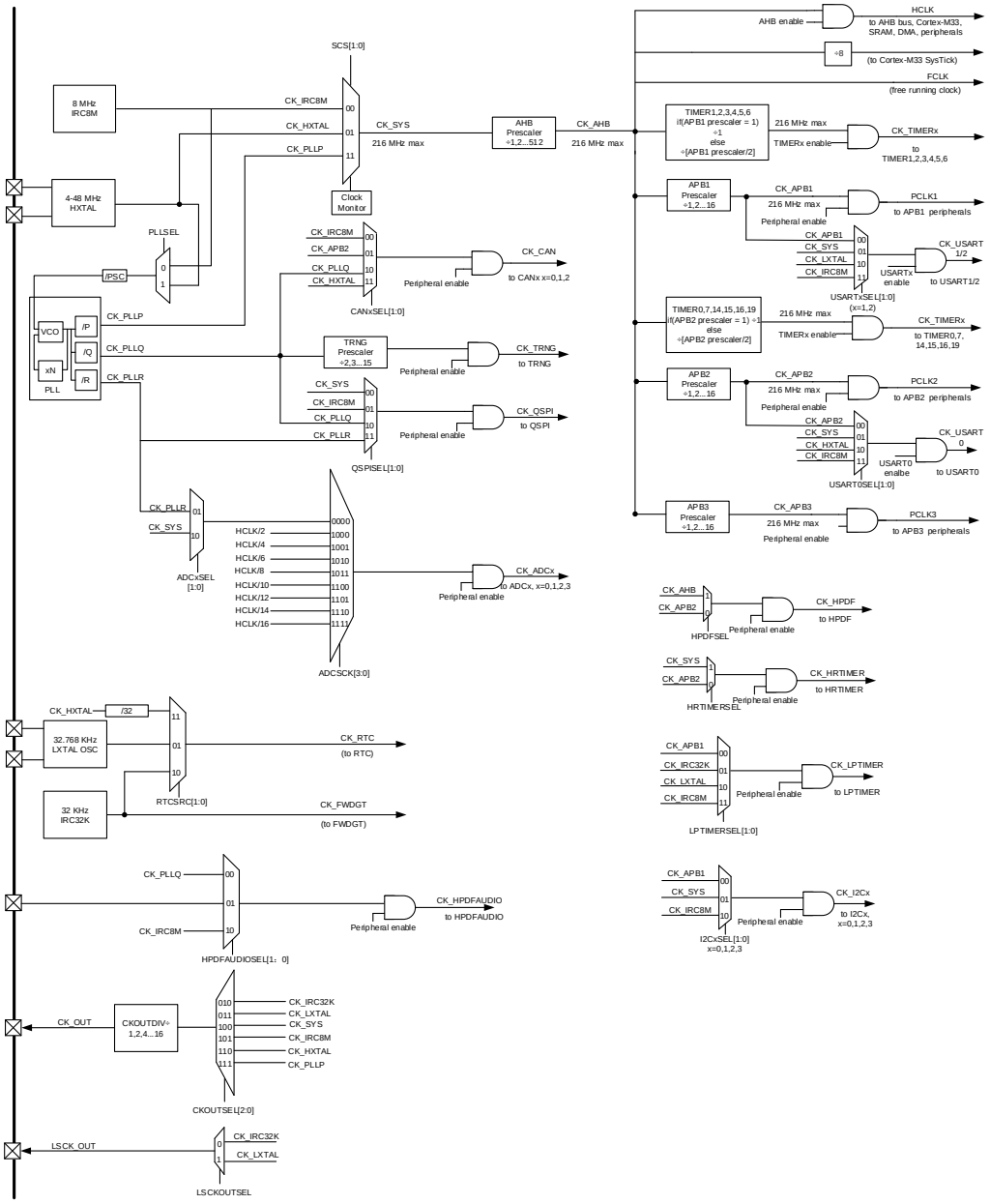
1. Internal pull-up resistance R_{PU} = 40 kΩ. You are advised to use an external pull-up resistance of 10 kΩ to ensure that voltage interference does not cause chip abnormalities.
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

2.2. Clock

GD32G5xx series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

- 4 - 48 MHz external high-speed crystal oscillator (HXTAL)
- Internal 8 MHz RC oscillator（IRC8M）
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- Internal 32 kHz RC oscillator（IRC32K）
- PLL clock source can be selected from HXTAL、IRC8M
- HXTAL clock monitor
- LXTAL clock monitor

Figure 2-10. GD32G5xx Clock Tree



Note: The clocks of the AHB, APB and Cortex®-M33 are derived from the system clock (CK_SYS) which can source from the IRC8M, HXTAL or PLL. The maximum operating frequency of the system clock (CK_SYS) can be up to 216 MHz.

2.2.1. External high-speed crystal oscillator clock (HXTAL)

The high speed external crystal oscillator (HXTAL), which has a frequency from 4 to 48 MHz, produces a highly accurate clock source for use as the system clock. A crystal with a specific frequency must be connected and located close to the two HXTAL pins. The external resistance and capacitance connected to the crystal must be adjusted according to the selected oscillator. The details are shown in ***Figure 2-11. HXTAL External Crystal Circuit***.

HXTAL can also use a bypass input mode to input a clock source (such as a 1 – 48 MHz active crystal oscillator). The details are shown in ***Figure 2-12. HXTAL External Clock Circuit***. When bypassing to an external circuit, the signal is connected to the OSC_IN pin, and the OSC_OUT pin is left floating. In the software, the bypass function for HXTAL needs to be enabled (set the HXTALBPS and HXTALEN bits to '1' in the control register RCU_CTL).

Figure 2-11. HXTAL External Crystal Circuit

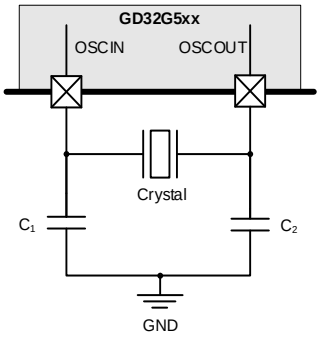
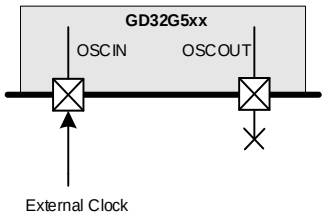


Figure 2-12. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSCIN, and OSCOUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.
3. C_S is the parasitic capacitance on the PCB board traces and MCU pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal oscillator > external passive crystal > internal crystal oscillator.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}.

7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSCOUT and OSCIN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.2.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL is an external low-speed crystal or ceramic resonator with a frequency of 32.768kHz. It provides a low-power and high-precision clock source for real-time clock circuits. The LXTAL oscillator can be turned on and off by setting the LXTALEN bit in the backup domain control register (RCU_BDCTL). The LXTALSTB bit in the backup domain control register RCU_BDCTL is used to indicate whether the LXTAL clock is stable. If the corresponding interrupt enable bit LXTALSTBIE in the interrupt register RCU_INT is set to '1', an interrupt will be generated after LXTAL stabilizes. ***Figure 2-13. LXTAL External Crystal Circuit*** shows the connection method for external low-speed crystals or ceramic resonators.

The external clock bypass mode can be selected by setting the LXTALBPS and LXTALEN to 1 'of the backup domain control register RCU_BDCTL. CK_LXTAL is consistent with the external clock signal connected to the OSC32IN pin. ***Figure 2-14. LXTAL External Clock Circuit*** shows the connection method for the external bypass mode.

Figure 2-13. LXTAL External Crystal Circuit

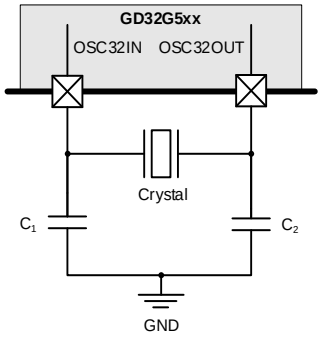
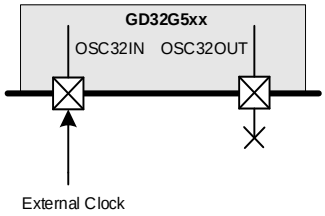


Figure 2-14. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32IN, and OSC32OUT

remains floating.

2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF ~ 7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. When the RTC selects IRC32K as the clock source and uses V_{BAT} external independent power supply, if the MCU loses power at this time, the RTC will stop counting. After re powering on, the RTC will continue to accumulate timing based on the previous count value. If the application needs to use V_{BAT} to power the RTC, and the RTC can still clock normally, the RTC must choose LXTAL as the clock source.
4. MCU can set the driving capacity of LXTAL. If during actual debugging, it is found that external low-speed crystals are difficult to vibrate, try adjusting the driving capacity of LXTAL to high.
5. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSCOUT and OSCIN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.2.3. Clock Output Capability (CKOUT)

GD32G5xx series can output clock signals ranging from 32KHz to 216MHz. By setting the CK_OUT clock source selection field CKOUT0SEL in the clock configuration register 0 (RCU_CFG0), different clock signals can be selected. The corresponding GPIO pin should be configured as an alternate function I/O (AFIO) mode to output the selected clock signal. ***Table 2-2. Clock output source select*** shows the available clock sources that can be output.

Table 2-2. Clock output source select

Clock source selection bits	Clock source
000	NO CLK
010	CK_IRC32K
011	CK_LXTAL
100	CK_SYS
101	CK_IRC8M
110	CK_HXTAL
111	CK_PLLP

The CK_OUT frequency can be reduced by a configurable binary divider, controlled by the CKOUTDIV[2:0] bits, in the configuration register 0(RCU_CFG0).

The CK_LXTAL and CK_IRC32K clock signals also can be output on LSCK_OUT pin, even in Deepsleep mode and Standby mode， which seleted by LSCKOUTSEL in the backup domain control register (RCU_BDCTL). The details are shown in ***Table 2-3. Low-speed clock output source select***.

Table 2-3. Low-speed clock output source select

Clock source selection bits	Clock source
0	CK_IRC32K
1	LXTAL

2.2.4. HXTAL Clock Monitor（CKM）

The HXTAL clock monitor function is enabled by the HXTAL clock monitor enable bit, CKMEN, in the control register (RCU_CTL). This function should be enabled after the HXTAL start-up delay and disabled when the HXTAL is stopped. Once the HXTAL failure is detected, the HXTAL will be automatically disabled. The HXTAL clock stuck interrupt flag, CKMIF, in the clock interrupt register, RCU_INT, will be set and the HXTAL failure event will be generated. This failure interrupt is connected to the non-maskable Interrupt, NMI, of the Cortex®-M33. If the HXTAL is selected as the clock source of CK_SYS, PLL and CK_RTC, the HXTAL failure will force the CK_SYS source to IRC8M, the PLL will be disabled automatically. If the HXTAL is selected as the clock source of RTC, the HXTAL failure will reset the RTC clock selection.

2.2.5. LXTAL clock monitor（LCKM）

A clock monitor on LXTAL can be activated by software writing the LCKMEN, in the control register, RCU_CTL. LCKMEN can not be enabled before LXTAL and IRC32K are enabled and ready.

A 4-bits plus one counter will work at IRC32K domain when LCKMEN enable. If the LXTAL clock has stuck at 0 / 1 error or slow down about 20KHz, the counter will overflow. The LXTAL clock failure will been found.

2.3. Startup Configuration

The GD32G5x3 series provide three kinds of boot sources which can be selected by the BOOT0 pin and boot configuration bits nBOOT1, nSWBT0 and nBOOT0 in the user option byte. The details are shown in ***Table 2-4. Boot modes***.

The value on the BOOT0 pin is latched on the 4th rising edge of CK_SYS after a reset. It is up to the user to set the boot mode configuration after a power-on reset or a system reset to select the required boot source. Once the pin has been sampled, it is free and can be used for other purposes.

Table 2-4. Boot modes

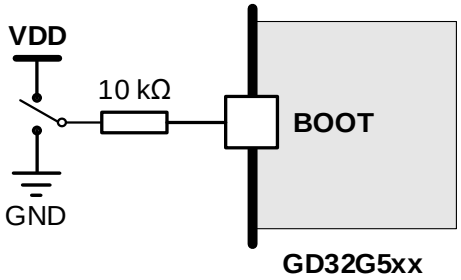
Selected boot area	Boot mode configuration				
	BOOTLK	nBOOT1 bit	BOOT0 pin	nSWBT0 bit	nBOOT0 bit
Main Flash memory	1	X	X	X	X
Main Flash memory	0	X	0	1	X
Main Flash memory	0	X	X	0	1
System memory	0	1	1	1	X
System memory	0	1	X	0	0
Embedded SRAM0	0	0	1	1	X
Embedded SRAM0	0	0	X	0	0

After power-on sequence or a system reset, the Arm® Cortex®-M33 processor fetches the top-of-stack value from address 0x0000 0000 and the base address of boot code from 0x0000 0004 in sequence. Then, it starts executing code from the base address of boot code.

According to the selected boot source, either the main flash memory (original memory space beginning at 0x0800 0000) or the system memory (original memory space beginning at 0x1FFF D000) is aliased in the boot memory space which begins at the address 0x0000 0000. When the on-chip SRAM whose memory space is beginning at 0x2000 0000 is selected as the boot source, in the application initialization code, you have to relocate the vector table in SRAM using the NVIC exception table and offset register.

The embedded boot loader is located in the System memory, which is used to reprogram the Flash memory. The boot loader can be activated through certain interfaces refer to the boot mode chapter of datasheet。For recommended BOOT circuit design, please refer to ***Figure 2-15. Recommend BOOT Circuit Design***.

Figure 2-15. Recommend BOOT Circuit Design



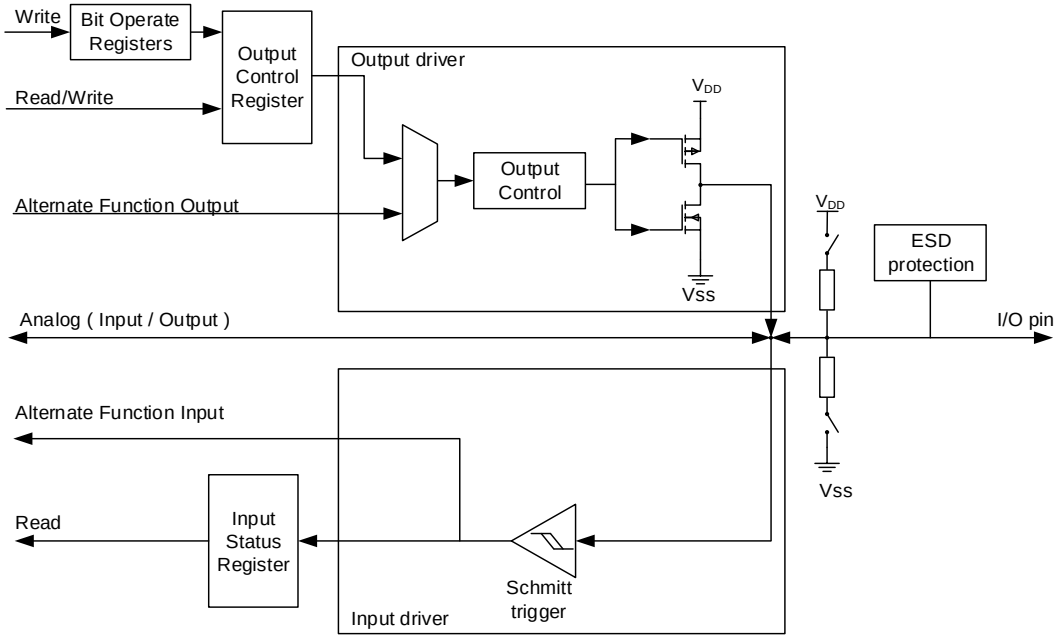
Note: After the MCU is running, if the BOOT state is changed, it will take effect after the system is reset. MCU.

2.4. Typical Peripheral Modules

2.4.1. GPIO Circuit

GD32G5xx can support up to 107 universal I/O pins（GPIO），including PA0 ~ PA15，PB0 ~ PB15，PC0 ~ PC15，PD0 ~ PD15，PE0 ~ PE15，PF0 ~ PF15，PG0 ~ PG10.Each on-chip device uses it to implement logical input / output functions. Each GPIO port has relevant control and configuration registers to meet the specific application requirements. The external interrupt of the GPIO pin of the on-chip device is controlled and configured by the register of the EXTI module. The basic structure of the GPIO port is shown in ***Figure 2-16. Basic structure of standard IO***:

Figure 2-16. Basic structure of standard IO



Note:

1. The IO port is divided into 5V tolerant and non-5V tolerant. When using, pay attention to distinguish the IO port withstand voltage, refer to the datasheet for details.
2. When the 5V-tolerant IO port is configured as an open drain output or input mode, a 5V voltage can be connected. When configured as a push-pull output mode, it is prohibited to connect a 5V voltage.
3. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
4. The three IO ports of PC13, PC14, PC15 have weak drive capability and limited output current capability(about 3mA). When configured in output mode, their working speed cannot exceed 2MHz(Maximum load is 30pF).

5. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.
6. Non-5V tolerance I/O, external voltage over V_{DD}, may generate perfusion current.
7. PG10 can function as a reset pin (NRST) or as a GPIO, depending on the NRST MODE bit in the user option byte. Input/output reset: Default power-on reset or reset after option byte loading, NRST MODE = 3; Reset input only: Reset after option byte loading, NRST MODE = 1; PG10 mode: After option byte loading, NRST MODE = 2.

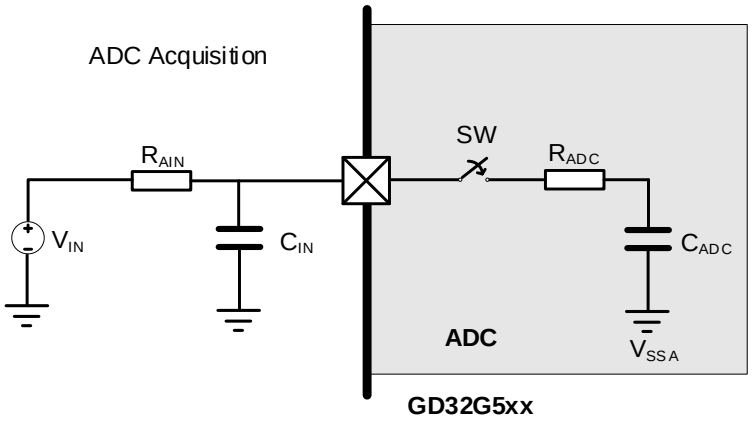
2.4.2. ADC Circuit

A 12-bit successive approximation analog-to-digital converter module(ADC) is integrated on the MCU chip. ADC0 has 14 external channels, 5 internal channels (temperature sensor, the battery voltage, DAC0_OUT0, DAC0_OUT1, VREFINT inputs channel), ADC1 has 16 external channels, 3 internal channels (DAC1_OUT0, DAC1_OUT1, VREFINT inputs channel), ADC2 has 15 external channels, 5 internal channels (VREFINT inputs channel, DAC2_OUT0, DAC2_OUT1, high-precision temperature sensor, the battery voltage), ADC3 has 18 external channels, 3 internal channels (DAC3_OUT0, DAC3_OUT1, VREFINT inputs channel). After sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit(LSB) alignment or the most significant(MSB) bit alignment. An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin, as shown in ***Figure 2-17. ADC Acquisition Circuit Design***:

Figure 2-17. ADC Acquisition Circuit Design



To achieve better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, select a larger value for the sampling period, and also try to minimize the input impedance in the external circuit design. If necessary, use an operational amplifier (op-amp) follower to reduce the input impedance. When f_{ADC} = 40 MHz, the

relationship between input impedance and sampling period is as shown in ***Table 2-5. Relationship between Sampling Period and External Input Impedance at fADC = 40MHz.***

Table 2-5. Relationship between Sampling Period and External Input Impedance at f_{ADC} = 40MHz.

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (kΩ)
3	0.075	0.55
15	0.375	4.65
28	0.7	9.15
55	1.375	18.43
84	2.1	28.46
112	2.8	38.1
144	3.6	49.17
480	12	N/A

Note:
When using ADC1 to sample external signals in the WLCSP81 package, if PC4 outputs a toggling signal, it may affect the accuracy of ADC1. Therefore, when using ADC1 and PC4 is also outputting a toggling signal, it is recommended to use a capacitor, such as 10nF, connected in parallel to PC4 and GND. This can eliminate the impact on the accuracy of ADC1.

2.4.3. Internal temperature sensor calibration

The GD32G5xx series MCU integrates an internal temperature sensor (ADC0_IN14) and a high-precision temperature sensor (ADC2_CH18). The output voltage of the temperature sensor varies linearly with temperature. To ensure accurate temperature measurement, it is necessary to provide the ADC with an accurate, low-drift reference voltage VREFP.

The output voltage of the temperature sensor varies linearly with temperature. Due to the diversity of chip production processes, the deviation of the temperature change curve may vary between chips (up to 45 °C difference). Internal temperature sensors are more suitable for detecting temperature changes than for measuring absolute temperature. If precise temperature measurement is required, an external temperature sensor should be used to calibrate this offset error.

Using temperature sensors：

1. Configure the conversion sequence and sampling time of the temperature sensor channel (ADC1_CH14) to ts_temp us.
2. Set the TSVEN1 bit in the ADC_CTL1 register to enable the temperature sensor.
3. Set the ADCON bit of the ADC_CTL1 register, or trigger ADC conversion externally.
4. Read and calculate the temperature sensor data Vtemperature from the ADC data register, and calculate the actual temperature using the following formula:

$$Temperature(°C) = \{(V_{25} - V_{temperature}) / Avg\_Slope\} + 25$$

V_{25}: $V_{temperature}$ value at 25°C, the typical value please refer to the datasheet.

Avg_Slope: Average Slope for curve between Temperature vs. $V_{temperature}$, the typical value please refer to the datasheet.

Using high-precision temperature sensors:

1. Configure the ADC clock(not greater than 5MHz).
2. Configure the conversion sequence (ADC2_IN18) and the sampling time(t_{s_temp} μs) for the channel.
3. Enable the temperature sensor by setting the TSVEN2 bit in the ADC control register 1 (ADC_CTL1).
4. Start the ADC conversion by setting the ADCON bit or by the triggers.
5. Read the temperature data($V_{temperature}$) in the ADC data register, and get the temperature with the following equation.

$$Temperature\ (°C) = \{(V_{temperature} - V_{25}) / Avg\_Slope\} + 25$$

V_{25}: $V_{temperature}$ value at 25°C, the typical value please refer to the datasheet.

Avg_Slope: Average Slope for curve between Temperature vs. $V_{temperature}$, the typical value please refer to the datasheet.

Note:

1. After the high precision temperature sensor is enabled, it is necessary to wait for at least 3 ADC sampling cycles before the ADC conversion code value is considered valid, and the first 3 conversion data should be discarded.
2. The sampling accuracy of high precision temperature sensor can be improved by means of hardware on chip over sampling or software averaging.

2.4.4. DAC Circuit

GD32G5xx series MCU integrates four DACs, each with two channels, and each DAC's two channels can work independently or concurrently.

The channels 0 and 1 of DAC0, as well as channels 0 and 1 of DAC1, can be output through GPIO, while other DACs can output to other internal circuits of the chip, such as comparators CMP, ADC, etc. Before enabling the DAC module, the GPIO pin (DAC output I/O) should be configured in analog mode.

For reducing output impedance and driving external loads without an external operational amplifier, an output buffer is integrated inside each DAC module.

The output buffer, which is turned on by default to reduce the output impedance and improve the driving capability, can be turned off by setting the MODEx bits in the DAC_MDCR register.

Note: DAC2 and DAC3 don’t have output buffer.

The DAC conversion can be triggered by software or rising edge of external trigger source. The DAC external trigger is enabled by setting the DTENx bits in the DAC_CTL0 register. The DAC external triggers are selected by the DTSELx bits in the DAC_CTL0 register, which is shown as ***Table 2-6. DAC triggers and outputs summary***.

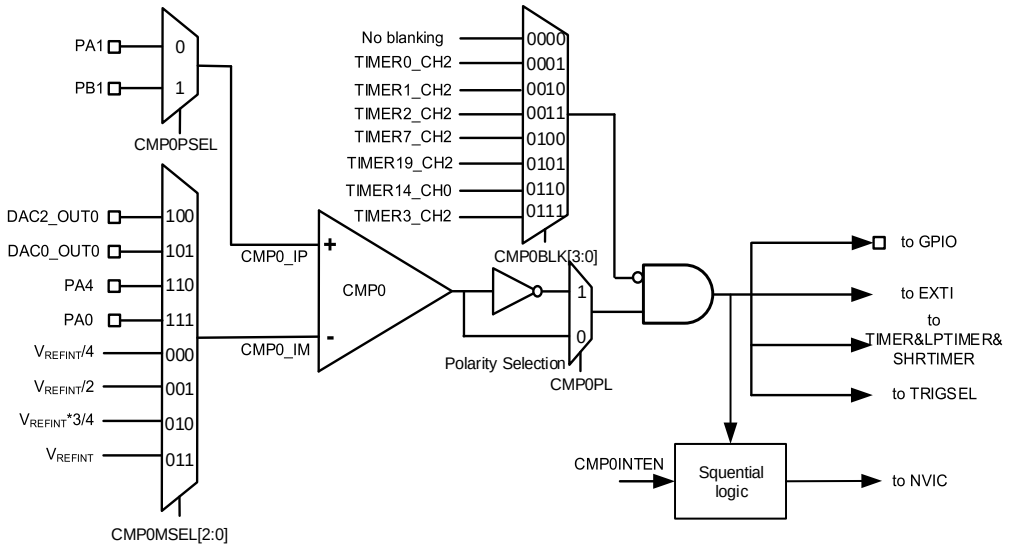
Table 2-6. DAC triggers and outputs summary

	DAC0		DAC1		DAC2		DAC3	
Unit	**Unit0**	**Unit1**	**Unit0**	**Unit1**	**Unit0**	**Unit1**	**Unit0**	**Unit1**
DAC outputs connected to I / Os	PA4	PA5	PA6	PA7	/	/	/	/
DAC output buffer	●	●	●	●	/	/	/	/
DAC trigger signals from TRIGSEL	●		●		●		●	
DAC software trigger	●		●		●		●	

2.4.5. CMP Circuit

GD32G5xx series of MCUs integrates eight rail-to-rail comparators (CMP). Each comparator can be configured with various input and output sources. Taking CMP0 as an example, ***Figure 2-18. CMP block diagram*** illustrates its internal structure.

Figure 2-18. CMP block diagram



These I / Os must be configured in analog mode in the GPIOs registers before they are selected as CMP inputs, ***Table 2-7. CMP inputs and outputs summary*** details the inputs and outputs of the CMP.

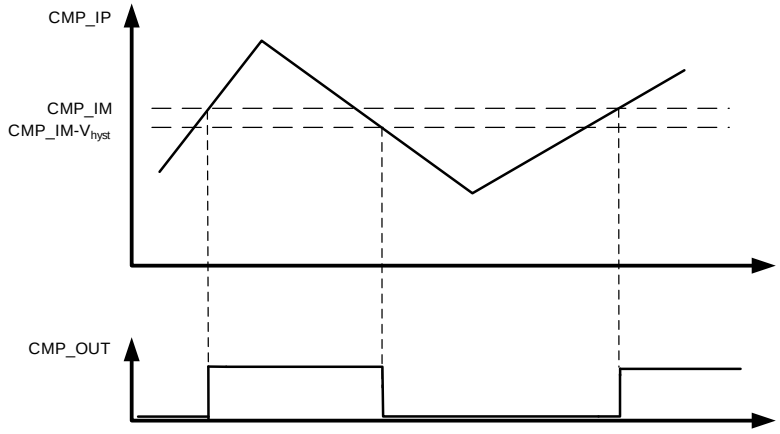
Table 2-7. CMP inputs and outputs summary

	CMP0	CMP1	CMP2	CMP3	CMP4	CMP5	CMP6	CMP7
CMP non inverting inputs connected to I/Os	PA1 PB1	PA7 PA3	PA0 PC1	PB0 PE7	PB13 PD12	PB11 PD11	PB14 PD14	PC2 PE9
CMP inverting inputs connected to I/Os	PA4 PA0	PA5 PA2	PF1 PC0	PE8 PB2	PB10 PD13	PD10 PB15	PD15 PB12	PD8 PD9
CMP inverting inputs connected to internal signals	V_{REFINT}/4, V_{REFINT}/2, V_{REFINT}*3/4, V_{REFINT}, DAC2_OUT0 DAC0_OUT0	V_{REFINT}/4, V_{REFINT}/2, V_{REFINT}*3/4, V_{REFINT}, DAC2_OUT1 DAC0_OUT1	V_{REFINT}/4, V_{REFINT}/2, V_{REFINT}*3/4, V_{REFINT}, DAC2_OUT0 DAC0_OUT0	V_{REFINT}/4, V_{REFINT}/2, V_{REFINT}*3/4, V_{REFINT}, DAC2_OUT1 DAC0_OUT0	V_{REFINT}/4, V_{REFINT}/2, V_{REFINT}*3/4, V_{REFINT}, DAC3_OUT0 DAC0_OUT1	V_{REFINT}/4, V_{REFINT}/2, V_{REFINT}*3/4, V_{REFINT}, DAC3_OUT1 DAC1_OUT0	V_{REFINT}/4, V_{REFINT}/2, V_{REFINT}*3/4, V_{REFINT}, DAC3_OUT0 DAC1_OUT0	V_{REFINT}/4, V_{REFINT}/2, V_{REFINT}*3/4, V_{REFINT}, DAC3_OUT1 DAC1_OUT1
CMP outputs connected to I/Os	PA0 PA6 PA11 PB8 PF4	PA2 PA7 PA12 PB9	PB7 PB15 PC2	PB1 PB6 PB14	PA9 PC7	PC6 PA10	PC8 PA8	PA13 PA14
CMP outputs connected to EXTI	●							
CMP outputs connected to TRIGSEL	●							
CMP outputs connected to NVIC	●							
CMP outputs connected to internal signals	TIMER0, TIMER1, TIMER2, TIMER3, TIMER4, TIMER7, TIMER19, LPTIMER, HRTIMER							

	CMP0	CMP1	CMP2	CMP3	CMP4	CMP5	CMP6	CMP7
CMP outputs connected to internal signals	BREAK0(TIMER0, TIMER7, TIMER14, TIMER15, TIMER16, TIMER19)							
	BREAK1(TIMER0, TIMER7, TIMER19)							

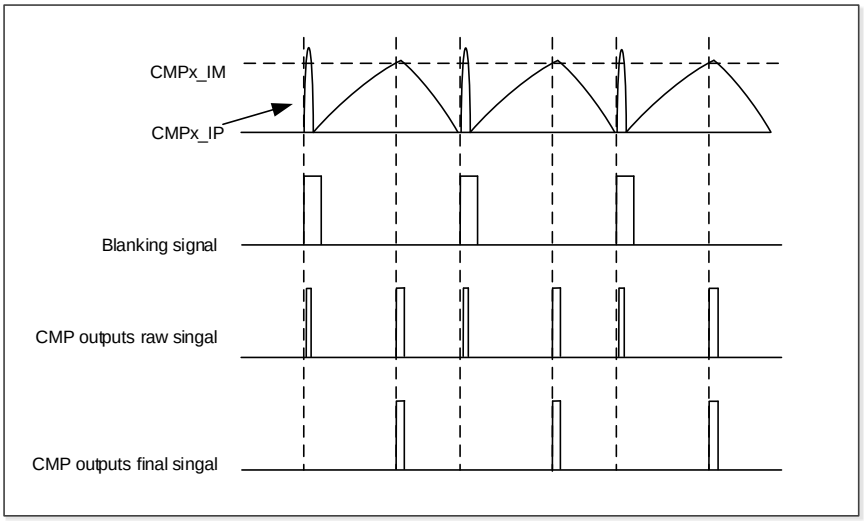
In order to avoid spurious output transitions that caused by the noise signal, a programmable hysteresis is designed to force the hysteresis value by configuring CMPx_CS register. This function could be shut down if it is unnecessary. ***Figure 2-19. CMP hysteresis*** illustrates the relevant details.

Figure 2-19. CMP hysteresis



CMP output blanking function can be used to avoid interference of short pulses in the input signal to CMP output signal. If the CMPxBLK[2:0] bits in the CMPx_CS register are setting to an available value, the CMP output final signal is obtained by ANDing the complementary signal of the selected blanking signal with the raw output of the comparator.***Figure 2-20. The CMP outputs signal blanking*** shows CMP output blanking function.

Figure 2-20. The CMP outputs signal blanking



For more detailed information on the functions and usage of the CMP peripheral, please refer to the《GD32G533_553_User_Manual》、《AN198 CMP usage in GD32G5 Series》.

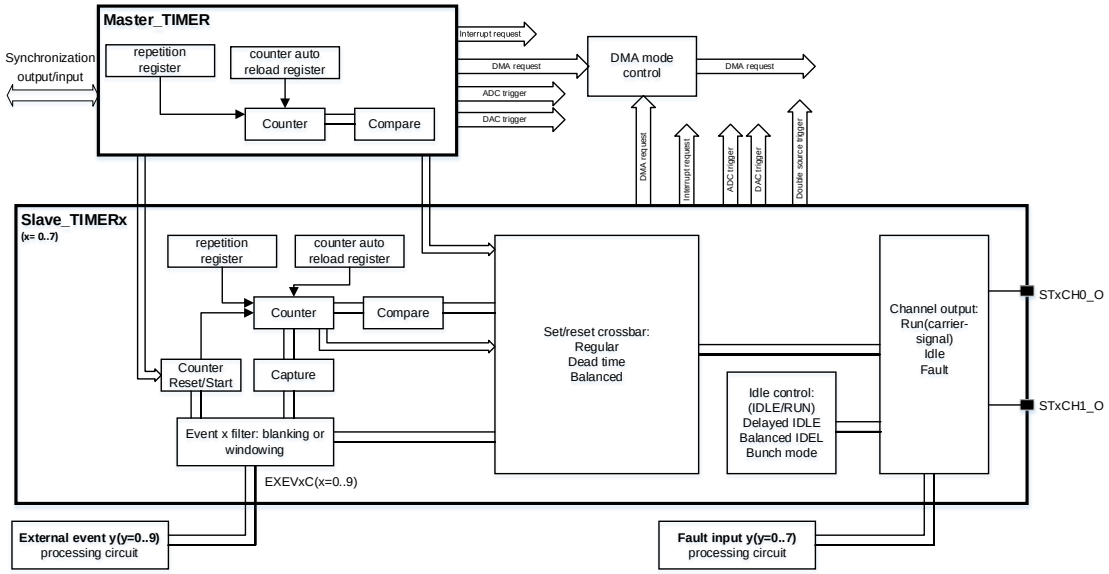
2.4.6. HRTIMER

HRTIMER has a high-resolution counting clock(Master_TIMER，Slave_TIMERx (x=0..7)) and can be used for high-precision timing. It can generate 16 high resolution and flexible digital signals to control motor or be used for power management applications. The 16 digital signals can be output independently or coupled into 8 pairs of complementary signals, and can be controlled by any timer unit.

It has a flexible capture function and can be used to capture timing the input signal. It has multiple internal signals connected to the ADC and DAC. It can be used for control and monitoring purposes.It can handle various fault input for safe purposes.

Figrue 2-21. HRTIMER block diagram provides the internal details and configuration of the HRTIMER.

Figrue 2-21. HRTIMER block diagram



The clock source of Master_TIMER is the HRTIMER_CK from module RCU. The DLL is used to produce a high resolution clock HRTIMER_HPCK ($f_{HRTIMER\_HPCK}$ = 32 *$f_{HRTIMER\_CK}$).

The prescaler (PSC) can divide the high resolution clock (HRTIMER_HPCK) to the counter clock (HRTIMER_PSCCK) by factor 2CNTCKDIV[2:0] which is controlled by CNTCKDIV[2:0] bit-field in HRTIMER_MTCTL0 register. The frequency relationship between them can be expressed below:

$$f_{HRTIMER\_PSCCK} = f_{HRTIMER\_HPCK} / 2^{CNTCKDIV[2:0]}$$

Table 2-8. Resolution with fHRTIMER_CK = 216MHz shows the various resolutions when the $f_{HRTIMER\_CK}$ is 216MHz.

Table 2-8. Resolution with $f_{HRTIMER\_CK}$ = 216MHz

CNTCKDIV[2:0]	$f_{HRTIMER\_PSCCK}$	Resolution
3'b000	216*32MHz = 6.912GHz	144.68ps
3'b001	216*16MHz = 3.456GHz	289.35ps
3'b010	216*8MHz = 1.728GHz	578.70ps
3'b011	216*4MHz = 864MHz	1.16ns
3'b100	216*2MHz = 432MHz	2.31ns
3'b101	216*1MHz = 216MHz	4.63ns
3'b110	216/2MHz = 108MHz	9.26ns
3'b111	216/4MHz = 54MHz	18.52ns

HRTIMER includes a variety of functions:

When HALFM bit in HRTIMER_MTCTL0 is set 1, the half mode is enabled. This mode forces the value of compare 0 active register to be half of the counter-reload value, but the value of HRTIMER_MTCMP0V register is not updated with the HRTIMER_MTCAR / 2 value. It is mainly used to generate a square wave with a fixed duty cycle of 50%.

The variable frequency half mode is complementary to the half mode, The output signal frequency is adjustable while the 180° phase shift is guaranteed.

Alternate mode helps achieve an alternate topology that complements the half mode. The compare value registers are automatically recalculated when the HRTIMER_MTCAR value is updated. alternate mode is selected by ALTM[1:0] bits in HRTIMER_MTCTL0 and HRTIMER_STxCTL0. It can perform triple interleaving (120°) and quadruple interleaving (90°).

Capture feature not only allows the Slave_TIMERx to perform measurements such as pulse interval, frequency, period, duty cycle and so on, but also to update compare 1 and compare 3 values in delayed mode.

The bunch mode controller allows to have the CHyOPRE (y=0,1) alternatively in IDLE and RUN state by hardware. This mode is enabled with BMEN bit in the HRTIMER_BMCTL register and usually used in light load situations.

HRTIMER can be configured to synchronize external resources and act as a master unit. The bit-field SYNOSRC[1:0] in HRTIMER_MTCTL0 register can be configured to selecte the source to be sent to the synchronization output. HRTIMER can wait for a trigger to be synchronized as a slaver. The bit-field SYNISRC[1:0] in HRTIMER_MTCTL0 register can be configured to select the synchronization input source.

The HRTIMER allows to have the embedded DACs updated synchronously with the timer updates. The update events from the Master_TIMER and Slave_TIMERx can generate DAC update triggers on HRTIMER_DACTRIGy(y=0..2).

Double source trigger is easy to implement ramp compensation techniques and hysteresis control. In this mode, the DAC outputs a sawtooth signal that gradually decreases, with the period of the sawtooth wave synchronized with the period of the PWM wave.

The immediately update mode of HRTIMER is available for compare 0 reset event and compare 2 reset event, and this mode is enabled by setting IMUPDxV bit in HRTIMER_STxCTL1 register. The output PWM waveform is updated immediately without waiting for the end of the current period when the immediate update mode is enabled. In the following situation, the PWM waveform is changed immediately.

For more detailed information on the peripheral functions and usage of HRTIMER, please refer to the《GD32G533_553 User Manual》and《AN203 GD32G5xx HRTimer Gudie App Note》.

2.5. Power Saving Modes

There are three methods for reducing chip power consumption through internal control: slowing down the system clock (HCLK, PCLK1, PCLK2, and PCLK3), and turning off the clocks of unused peripherals.

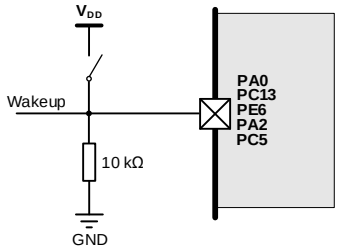
Additionally, the GD32G5xx series has three low power modes to achieve even lower power consumption. These modes are Sleep mode, Deep Sleep mode, and Standby mode.

Table 2-9. Power domain summary

Mode	Sleep	Deep-sleep	Standby
Description	Only CPU clock is off	1. All clocks in the 1.1V domain are off 2. Disable IRC8M / HXTAL and PLLs	1. The 1.1V domain is power off 2. Disable IRC8M / HXTAL and PLLs
LDO Status	On	On or in low power mode	Off
Configuration	SLEEPDEEP = 0	SLEEPDEEP = 1, STBMOD = 0	SLEEPDEEP = 1 STBMOD = 1, WURST=1
Entry	WFI or WFE	WFI or WFE	WFI or WFE
Wakeup	Any interrupt for WFI Any event (or interrupt when SEVONPEND is 1) for WFE	Any interrupt from EXTI lines for WFI Any event(or interrupt when SEVONPEND is 1) from EXTI for WFE	1. NRST pin 2. WKUP pins 3. FWDGT reset 4. RTC 5. LCKMD
Wakeup Latency	None	IRC8M wakeup time,LDO wakeup time added if LDO is in low power mode	Power on sequence

Among these, the mode with the lowest power consumption is Standby mode. This low power mode also requires the longest wake-up time. Waking up from Standby mode can be achieved through a rising edge on the WKUP pin, and this can be configured by setting the WUPENx bit in the PMU_CS register. For the corresponding WKUP wake-up pin reference circuit design, please see ***Figure 2-22. Recommend Standby external wake-up pin circuit design*** is shown as follows.

Figure 2-22. Recommend Standby external wake-up pin circuit design



Note:

1. In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.
2. In many application designs, to ensure that the WKUP pin does not receive excessive external current, a current-limiting resistor is often added in series with the WKUP pin. Because the WKUP pin is configured to wake up on the rising edge and is internally set to input pull-down mode, this will cause the WKUP signal to be divided. Therefore, it is recommended that the series resistor should not exceed 1kΩ.

2.6. Download the debug circuit

The GD32G5xx series supports both JTAG and SWD debugging interfaces, with SWD being the default. It is possible to switch to JTAG mode by modifying the efuse settings, and it also supports secure JTAG. However, once switched to JTAG, it is not possible to revert back to SWD mode. The JTAG interface standard is a 20-pin interface, with 5 signal pins, while the SWD interface standard is a 5-pin interface, with 2 signal pins.

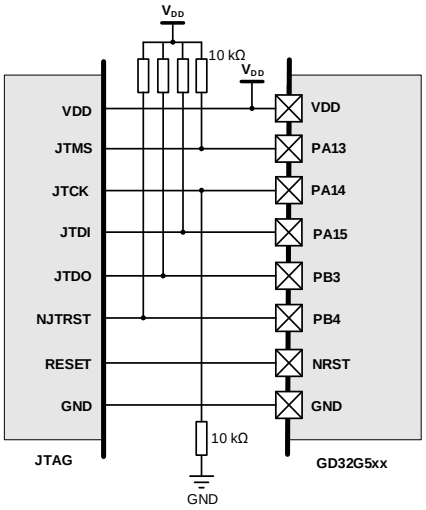
Note: After reset, the debug related ports are in input pull-up / pull-down mode, where:

PA15: JTDI in pull-up mode
PA14: JTCK / SWCLK in pull-down mode
PA13: JTMS / SWDIO in pull-up mode
PB4: NJTRST in pull-up mode
PB3: JTDO in floating mode

Tsble 2-10. JTAG download debug interface assignment

Alternate function	GPIO port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-23. Recommend JTAG wiring reference design



Note: After reset, the debug related ports are in input pull-up / pull-down mode, where:

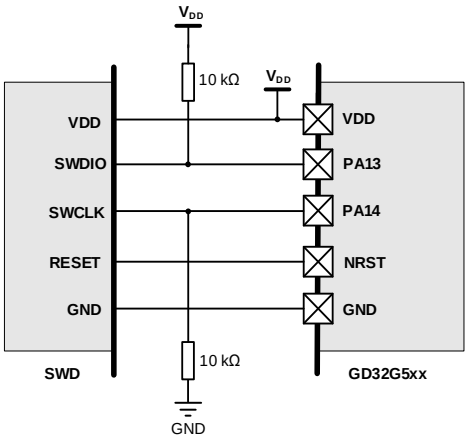
PA13: SWDIO in pull-up mode

PA14: SWCLK in pull-down mode

Table 2-11. SWD download debug interface assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-24. Recommend SWD Wiring Reference Design

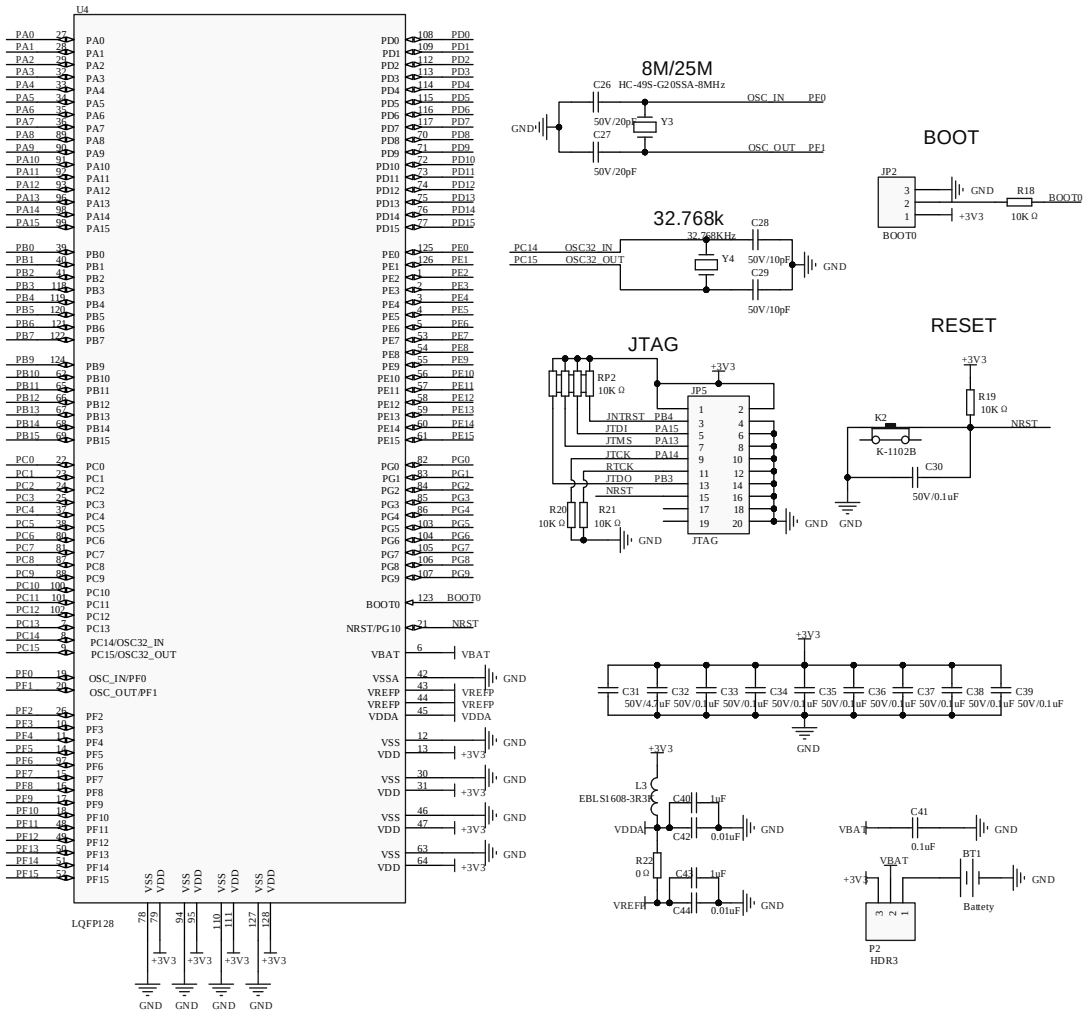


There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15 cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100 Ω ~ 1 kΩ resistor.

2.7. Reference Schematic Design

Figure 2-25. GD32H7xx Recommend Reference Schematic Design



3. PCB Layout Design

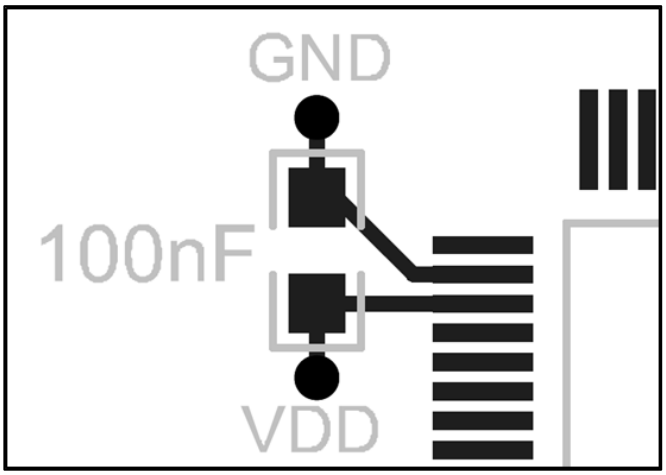
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32G5xx series power supply has VDD, VDDA, VREFP and other power supply pins. Ceramic MLCC can be used for the 100nF decoupling capacitor, and the position should be as close to the power pin as possible. The power cable should be routed through the capacitor before reaching the MCU power pin. It is recommended to lay out a Layout in the form of Via near the capacitor PAD.

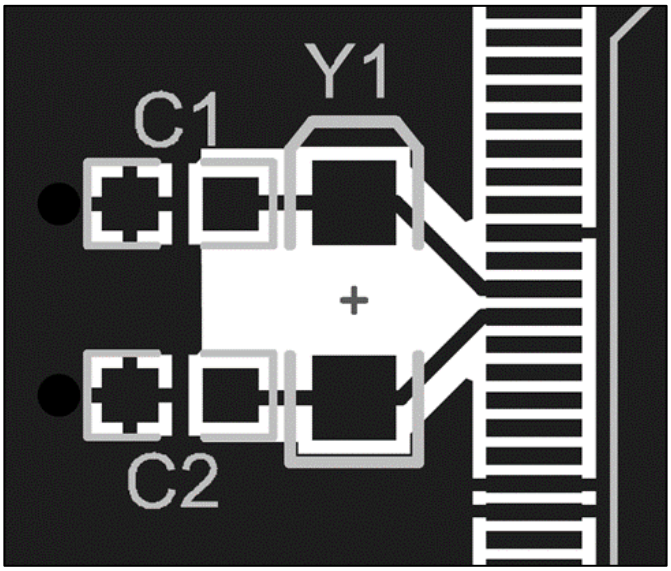
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32G5xx series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



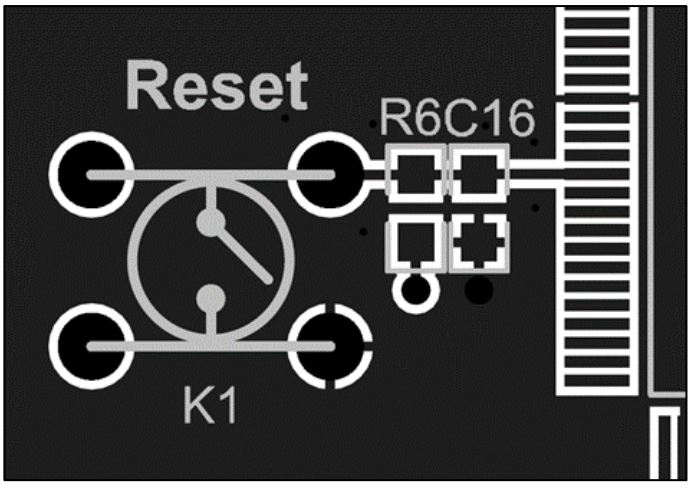
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

For the NRST trace layout on the PCB, please refer to ***Figure 3-3. Recommend NRST Trace Layout Design*** is shown as follows.

Figure 3-3. Recommend NRST Trace Layout Design



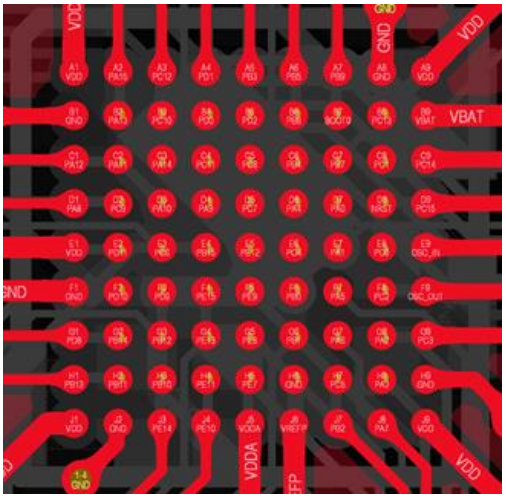
Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better to wrap the NRST traces for better shielding effect.

3.4. Fan-out for WLCSP Package

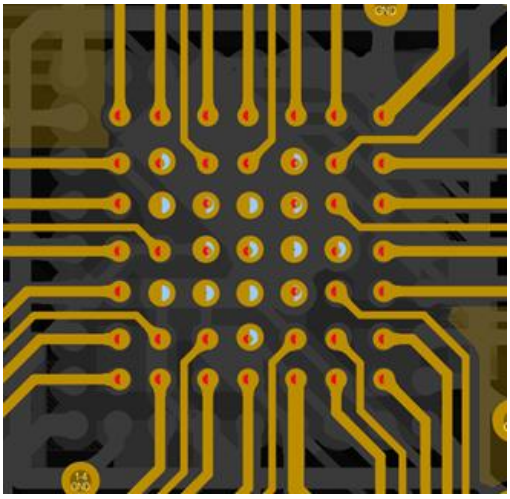
For certain models in the GD32G5xx series MCUs that use the WLCSP81 package, the following routing rules and fan-out methods are recommended：

1、 It is recommended to use a four-layer board or higher for the WLCSP81 package.
2、 Use a rule setting with a 3-mil line width and spacing.
3、 Use 4/8 mil vias. For fan-out, utilize blind and buried vias within some pads. The fan-out after these steps is illustrated in ***Figure 3-4. Fan-out for WLCSP Package***.

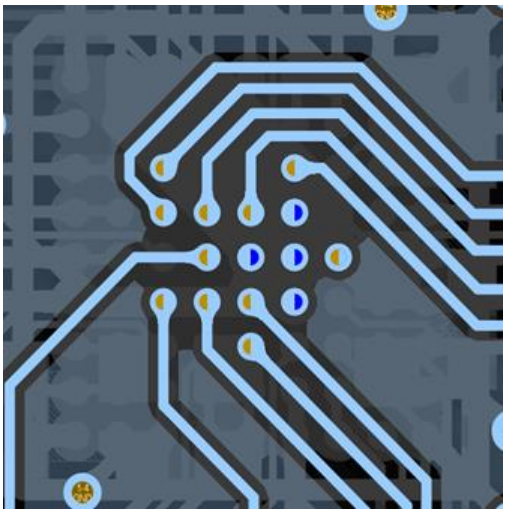
Figure 3-4. Fan-out for WLCSP Package



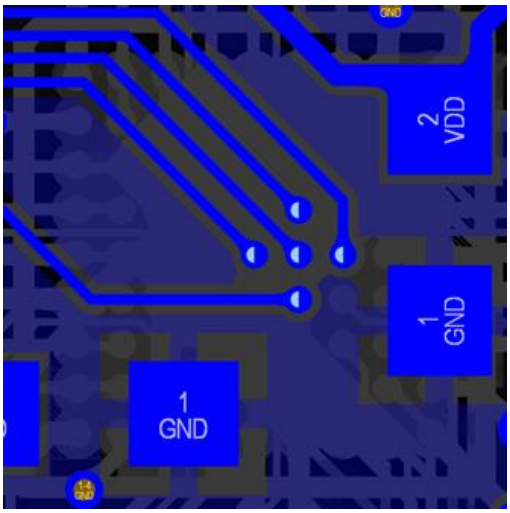
Top Layer



Layer 2



Layer 3



Bottom Layer

4. Package Description

The GD32H7xx series comes in five packaging forms, LQFP128、WLCSP81、LQFP64、LQFP64 and QFN48.

Table 4-1. Package Description

Ordering code	Package
GD32G553QxT6	LQFP128（14x14, 0.4 pitch）
GD32G533QxT6	
GD32G553MEY6	WLCSP81（4x4, 0.4 pitch）
GD32G533MEY6	
GD32G553RET6	LQFP64（10x10, 0.5 pitch）
GD32G533RxT6	
GD32G553CET6	LQFP48(7x7, 0.5 pitch)
GD32G533CxT6	
GD32G553CEU6	QFN48(7x7, 0.5 pitch)
GD32G533CxU6	

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Sep.15, 2024

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