GigaDevice Semiconductor Inc.

GD32E231xx
ARM® Cortex®-M23 32-bit MCU

Datasheet

Revision 1.3

(Sep. 2024)

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1 General description

The GD32E231xx device belongs to the value line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M23 core. The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor delivers high energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier and a 17-cycle divider.

The GD32E231xx device incorporates the ARM® Cortex®-M23 32-bit processor core operating at up to 72 MHz frequency with Flash accesses 0~2 wait states to obtain maximum efficiency. It provides up to 64 KB embedded Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC and one comparator, two OP-AMP, up to five general 16-bit timers, a basic timer, a PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs, an USART, and an I2S.

The device operates from a 1.8 to 3.6 V power supply and available in –40 to +85 °C temperature range for grade 6 devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32E231xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

2 Device overview

2.1 Device information

Table 2-1. GD32E231xx devices features and peripheral list

Part Number		GD32E231K8Q6	GD32E231T8O6
FLASH (KB)		64	64
SRAM (KB)		8	8
Timers	**General timer(16-bit)**	5 (2,13-16)	5 (2,13-16)
	Advanced timer(16-bit)	1 (0)	1 (0)
	SysTick	1	1
	Basic timer(16-bit)	1 (5)	1 (5)
	Watchdog	2	2
	RTC	1	1
Connectivity	**USART**	1 (0)	1 (0)
	I2C	2 (0-1)	2 (0-1)
	SPI/I2S	2/1 (0-1)/(0)	2/1 (0-1)/(0)
GPIO		25	26
CMP		1	1
OP-AMP		1	2
EXTI		15	15
ADC	**Units**	1	1
	Channels (External)	10	10
	Channels (Internal)	2	2
Package		QFN32	QFN36

2.2   Block diagram

Figure 2-1. GD32E231xx block diagram
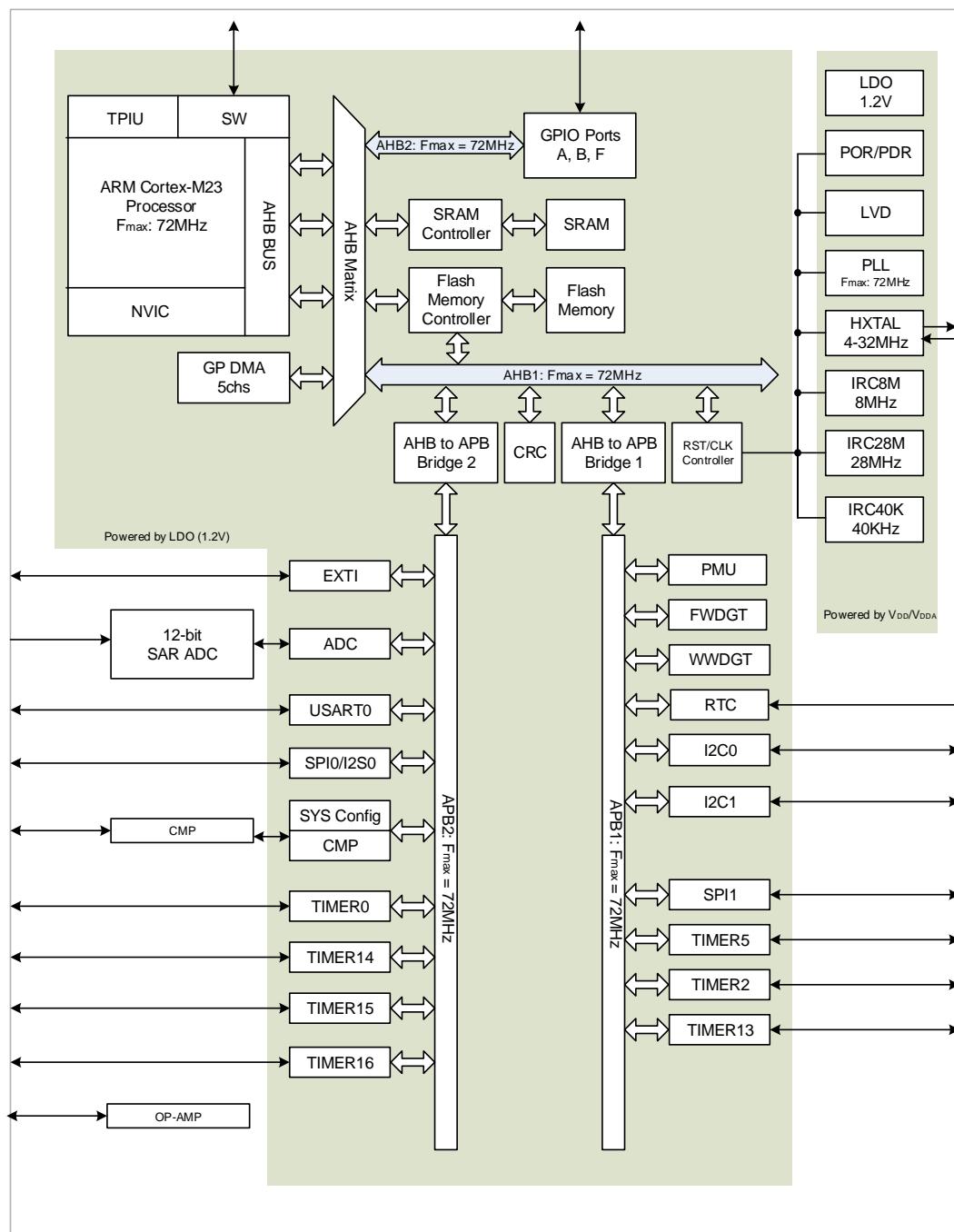
2.3   Pinouts and pin assignment

Figure 2-2. GD32E231T8O6 QFN36 pinouts
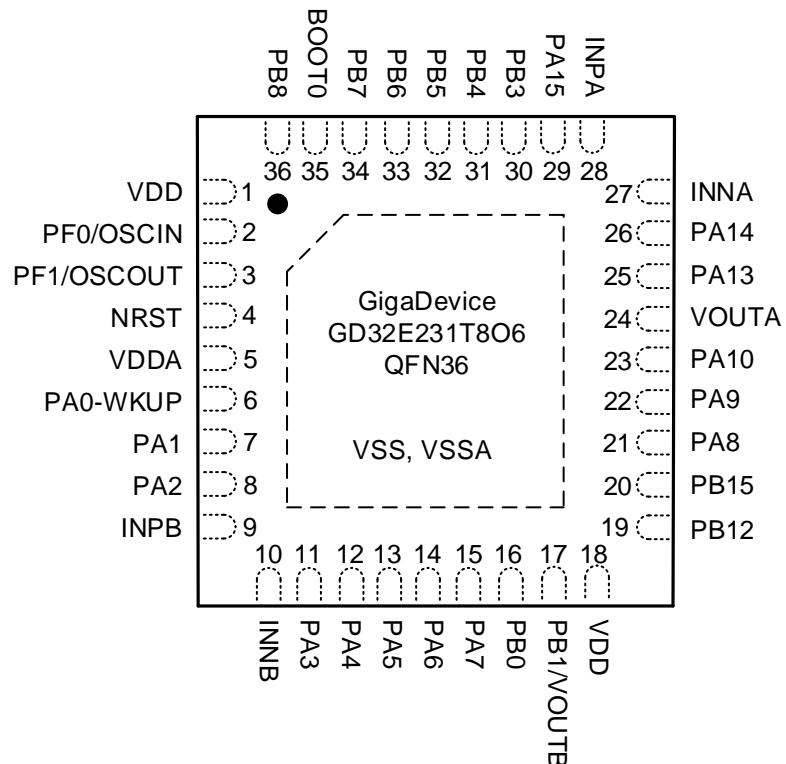
Figure 2-3. GD32E231K8Q6 QFN32 pinouts
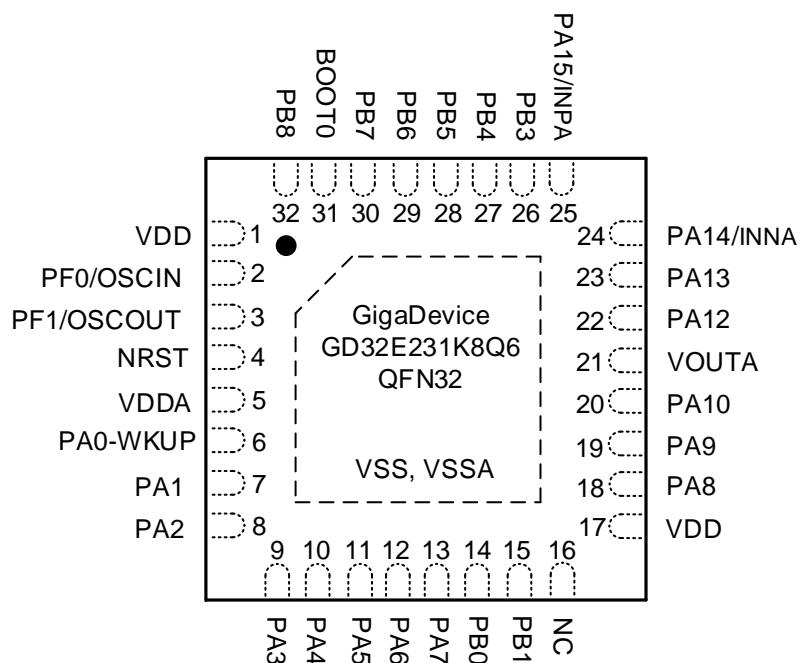
2.4 Memory map

Table 2-2. GD32E231xx memory map

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex M23 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x60000000 - 0x9FFFFFFF	Reserved
Peripherals	AHB1	0x5004 0000 - 0x5FFF FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	Reserved
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	Reserved
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4002 4400 - 0x47FF FFFF	Reserved
		0x4002 4000 - 0x4002 43FF	Reserved
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0400 - 0x4002 0FFF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB2	0x4001 8000 - 0x4001 FFFF	Reserved
		0x4001 5C00 - 0x4001 7FFF	Reserved
		0x4001 5800 - 0x4001 5BFF	DBG
		0x4001 4C00 - 0x4001 57FF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0/I2S0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 0800 - 0x4001 23FF	Reserved

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG + CMP
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	Reserved
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6400 - 0x4000 6FFF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4800 - 0x4000 53FF	Reserved
		0x4000 4400 - 0x4000 47FF	Reserved
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1400 - 0x4000 1FFF	Reserved
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0800 - 0x4000 0FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	Reserved
SRAM		0x2000 2000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 1FFF	SRAM
Code		0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option bytes
		0x1FFF EC00 - 0x1FFF F7FF	System memory
		0x0801 0000 - 0x1FFF EBFF	Reserved
		0x0800 0000 - 0x0800 FFFF	Main Flash memory
		0x0001 0000 - 0x07FF FFFF	Reserved

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x00000000 - 0x0000FFFF	Aliased to Flash or system memory

2.5 Clock tree

Figure 2-4. GD32E231xx clock tree
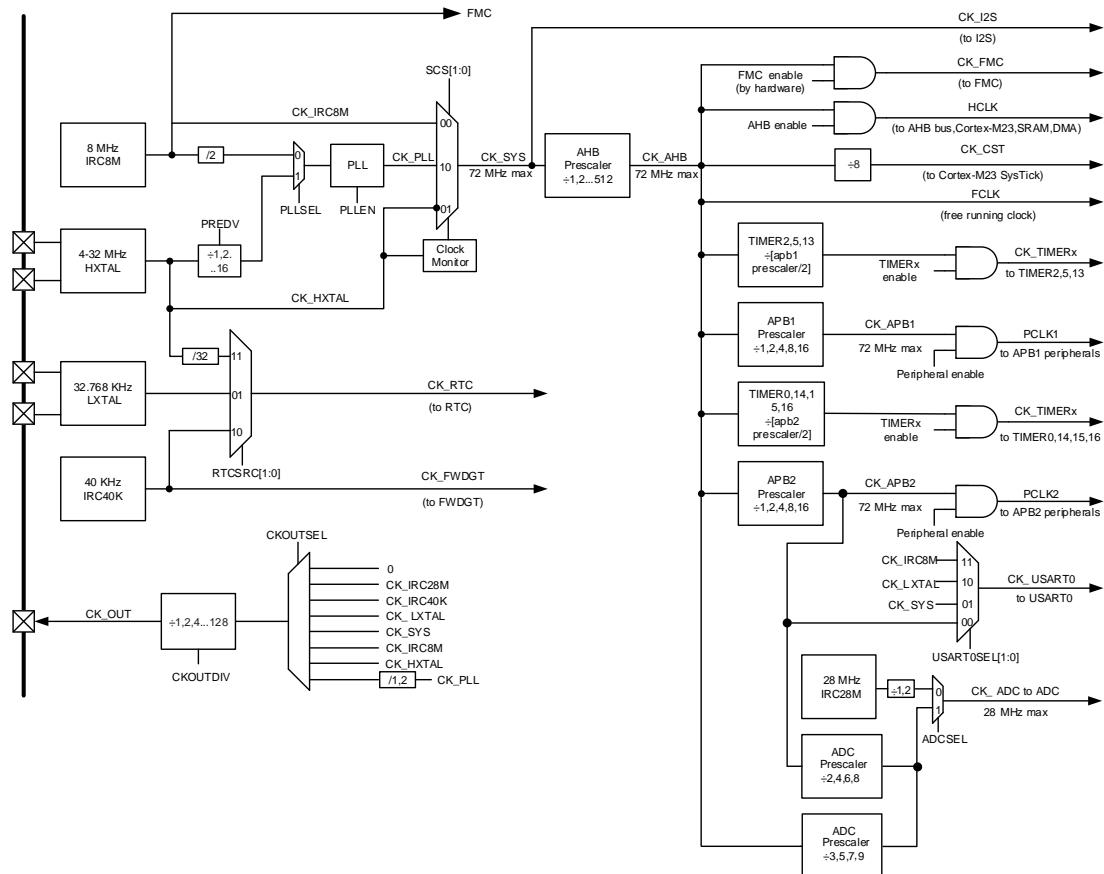
Note:

If the APB prescaler is 1, the timer clock frequencies are set to AHB frequency divide by 1.
Otherwise, they are set to the AHB frequency divide by half of APB prescaler.

Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillator

IRC40K: Internal 40K RC oscillator

IRC28M: Internal 28M RC oscillator

2.6   Pin definitions

2.6.1   GD32E231T8O6 QFN36 pin definitions

Table 2-3. GD32E231T8O6 QFN36 pin definitions

GD32E231T8O6 QFN36				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VDD	1	P		Default: VDD
PF0/OSCIN	2	I/O	5VT	Default: PF0 Alternate: I2C0_SDA Additional: OSCIN
PF1/OSCOUT	3	I/O	5VT	Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT
NRST	4	I/O		Default: NRST
VDDA	5	P		Default: VDDA
PA0-WKUP	6	I/O		Default: PA0 Alternate: CMP_OUT, I2C1_SCL Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: I2C1_SDA, EVENTOUT, TIMER14_CH0_ON Additional: ADC_IN1, CMP_IP
PA2	8	I/O		Default: PA2 Alternate: TIMER14_CH0 Additional: ADC_IN2, CMP_IM7
INPB	9	I		Default: OPA_INPB
INNB	10	I		Default: OPA_INNB
PA3	11	I/O		Default: PA3 Alternate: TIMER14_CH1 Additional: ADC_IN3
PA4	12	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, TIMER13_CH0, SPI1_NSS Additional: ADC_IN4, CMP_IM4
PA5	13	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5, CMP_IM5
PA6	14	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: ADC_IN6
PA7	15	I/O		Default: PA7

Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
				Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	16	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, EVENTOUT Additional: ADC_IN8
PB1/VOUTB	17	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK Additional: ADC_IN9, OPA_VOUTB
VDD	18	P		Default: VDD
PB12	19	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, TIMER0_BRKIN, I2C1_SMBA, EVENTOUT
PB15	20	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN, WKUP6
PA8	21	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, EVENTOUT
PA9	22	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL, CK_OUT
PA10	23	I/O	5VT	Default: PA10 Alternate: USART0_RX,TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
VOUTA	24	O		Default: OPA_VOUTA
PA13	25	I/O	5VT	Default: PA13/SWDIO Alternate: SWDIO, IFRP_OUT, SPI1_MISO
PA14	26	I/O	5VT	Default: PA14/SWCLK Alternate: SWCLK, SPI1_MOSI
INNA	27	I		Default: OPA_INNA
INPA	28	I		Default: OPA_INPA
PA15	29	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, I2S0_WS, SPI1_NSS, EVENTOUT
PB3	30	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT
PB4	31	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT, I2C0_TXFRAME, TIMER16_BRKIN
PB5	32	I/O	5VT	Default: PB5

Table header: **GD32E231T8O6 QFN36**

GD32E231T8O6 QFN36				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1
				Additional: WKUP5
PB6	33	I/O	5VT	Default: PB6
				Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	34	I/O	5VT	Default: PB7
				Alternate:I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	35	I		Default: BOOT0
PB8	36	I/O	5VT	Default: PB8
				Alternate: I2C0_SCL, TIMER15_CH0

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2 GD32E231K8Q6 QFN32 pin definitions

Table 2-4. GD32E231K8Q6 QFN32 pin definitions

GD32E231K8Q6 QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VDD	1	P		Default: VDD
PF0/OSCIN	2	I/O	5VT	Default: PF0
				Alternate: I2C0_SDA
				Additional: OSCIN
PF1/OSCOUT	3	I/O	5VT	Default: PF1
				Alternate: I2C0_SCL
				Additional: OSCOUT
NRST	4	I/O		Default: NRST
VDDA	5	P		Default: VDDA
PA0-WKUP	6	I/O		Default: PA0
				Alternate: CMP_OUT, I2C1_SCL
				Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1
				Alternate: I2C1_SDA, EVENTOUT, TIMER14_CH0_ON
				Additional: ADC_IN1, CMP_IP
PA2	8	I/O		Default: PA2
				Alternate: TIMER14_CH0
				Additional: ADC_IN2, CMP_IM7
PA3	9	I/O		Default: PA3
				Alternate: TIMER14_CH1
				Additional: ADC_IN3
PA4	10	I/O		Default: PA4
				Alternate: SPI0_NSS, I2S0_WS, TIMER13_CH0,

GD32E231K8Q6 QFN32				
Pin Name	**Pins**	**Pin Type**[1]	**I/O Level**[2]	**Functions description**
				SPI1_NSS
				Additional: ADC_IN4, CMP_IM4
PA5	11	I/O		Default: PA5
				Alternate: SPI0_SCK, I2S0_CK
				Additional: ADC_IN5, CMP_IM5
PA6	12	I/O		Default: PA6
				Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT
				Additional: ADC_IN6
PA7	13	I/O		Default: PA7
				Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT
				Additional: ADC_IN7
PB0	14	I/O		Default: PB0
				Alternate: TIMER2_CH2, TIMER0_CH1_ON, EVENTOUT
				Additional: ADC_IN8
PB1	15	I/O		Default: PB1
				Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK
				Additional: ADC_IN9
NC	16	O		Default: Not connected
VDD	17	P		Default: VDD
PA8	18	I/O	5VT	Default: PA8
				Alternate: USART0_CK, TIMER0_CH0, CK_OUT, EVENTOUT
PA9	19	I/O	5VT	Default: PA9
				Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL, CK_OUT
PA10	20	I/O	5VT	Default: PA10
				Alternate: USART0_RX,TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
VOUTA	21	O		Default: OPA_VOUTA
PA12	22	I/O	5VT	Default: PA12
				Alternate: USART0_RTS/USART0_DE, TIMER0_ETI, EVENTOUT, I2C0_TXFRAME, I2C1_SDA
PA13	23	I/O	5VT	Default: PA13/SWDIO
				Alternate: SWDIO, IFRP_OUT, SPI1_MISO
PA14/INNA	24	I/O	5VT	Default: PA14/SWCLK
				Alternate: SWCLK, SPI1_MOSI
				Additional: OPA_INNA
PA15/INPA	25	I/O	5VT	Default: PA15

GD32E231K8Q6 QFN32				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: SPI0_NSS, I2S0_WS, SPI1_NSS, EVENTOUT Additional: OPA_INPA
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT, I2C0_TXFRAME, TIMER16_BRKIN
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional: WKUP5
PB6	29	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	30	I/O	5VT	Default: PB7 Alternate:I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	31	I		Default: BOOT0
PB8	32	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0

Notes:

(1)   Type: I = input, O = output, P = power.

(2)   I/O Level: 5VT = 5 V tolerant.

2.6.3   GD32E231xx pin alternate functions

Table 2-5. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0					I2C1_SCL			CMP_OUT
PA1	EVENTOUT				I2C1_SDA	TIMER14_CH0_ON		
PA2	TIMER14_CH0							
PA3	TIMER14_CH1							
PA4	SPI0_NSS/I2S0_WS				TIMER13_CH0	SPI1_NSS		
PA5	SPI0_SCK/I2S0_CK							
PA6	SPI0_MISO/I2S0_MCK	TIMER2_CH0	TIMER0_BRKIN			TIMER15_CH0	EVENTOUT	CMP_OUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA7	SPI0_MOSI/ I2S0_SD	TIMER2_CH1	TIMER0_CH0_ON		TIMER13_CH0	TIMER16_CH0	EVENT OUT	
PA8	CK_OUT	USART0_CK	TIMER0_CH0	EVENT OUT				
PA9	TIMER14_BRKIN	USART0_TX	TIMER0_CH1		I2C0_SCL	CK_OUT		
PA10	TIMER16_BRKIN	USART0_RX	TIMER0_CH2		I2C0_SDA			
PA12	EVENTOUT	USART0_RTS/USART0_DE	TIMER0_ETI		I2C0_TXFRAME	I2C1_SDA		
PA13	SWDIO	IFRP_OUT					SPI1_MISO	
PA14	SWCLK						SPI1_MOSI	
PA15	SPI0_NSS/I2S0_WS			EVENT OUT			SPI1_NSS	

Table 2-6. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	EVENTOUT	TIMER2_CH2	TIMER0_CH1_ON					
PB1	TIMER13_CH0	TIMER2_CH3	TIMER0_CH2_ON				SPI1_SCK	
PB3	SPI0_SCK/I2S0_CK	EVENTOUT						
PB4	SPI0_MISO/I2S0_MCK	TIMER2_CH0	EVENTOUT		I2C0_TXFRAME		TIMER16_BRKIN	
PB5	SPI0_MOSI/I2S0_SD	TIMER2_CH1	TIMER15_BRKIN	I2C0_SMBA				
PB6	USART0_TX	I2C0_SCL	TIMER15_CH0_ON					
PB7	USART0_RX	I2C0_SDA	TIMER16_CH0_ON					
PB8		I2C0_SCL	TIMER15_CH0					
PB12	SPI1_NSS	EVENTOUT	TIMER0_BRKIN		I2C1_SMBA			
PB15	SPI1_MOSI	TIMER14_CH1	TIMER0_CH2_ON	TIMER14_CH0_ON				

Table 2-7. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PF0		I2C0_SDA					
PF1		I2C0_SCL					

3   Functional description

3.1   ARM® Cortex®-M23 core

The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M23 processor core

- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Ultra-low power, energy-efficient operation
- Excellent code density
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M23 processor is based on the ARMv8-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M23:

- Internal Bus Matrix connected with AHB master, Serial Wire Debug Port and Single-cycle IO port
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit(BPU)
- Data Watchpoint
- Serial Wire Debug Port

3.2   Embedded memory

- Up to 64 Kbytes of Flash memory
- Up to 8 Kbytes of SRAM with hardware parity checking

64 Kbytes of inner Flash and 8 Kbytes of inner SRAM at most is available for storing programs and data, and Flash is accessed (read) at CPU clock speed with 0~2 wait states. *Table 2-2. GD32E231xx memory map* shows the memory map of the GD32E231xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3   Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator

- Internal 28 MHz RC oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 1.8 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 72 MHz/72 MHz/72 MHz. See *Figure 2-4. GD32E231xx clock tree* for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.71 V and down to 1.67 V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:
- V_{DD} range: 1.8 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 1.8 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAK} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4 Boot modes

At startup, boot pins are used to select one of three boot options:
- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10).

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance

between the CPU operating time, speed and power consumption.

■ **Sleep mode**

In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

■ **Deep-sleep mode**

In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC tamper and timestamp, CMP output, LVD output and USART wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

■ **Standby mode**

In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6 Analog to digital converter (ADC)

■ 12-bit SAR ADC's conversion rate is up to 2 MSPS
■ 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
■ Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
■ Input voltage range: V_{SSA} to V_{DDA}
■ Temperature sensor

One 12-bit 2 MSPS multi-channel ADC is integrated in the device. It has a total of 12 multiplexed channels: up to 10 external channels, 1 channel for internal temperature sensor (V_{SENSE}) and 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between V_{SSA} and V_{DDA}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timer (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7 DMA

■ 5 channels DMA controller

■ Peripherals supported: Timers, ADC, SPIs, I2Cs, USART0 and I2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.8 General-purpose inputs/outputs (GPIOs)

■ Up to 26 fast GPIOs, all mappable on 15 external interrupt lines (line0 ~ line10, line12 ~ line15)

■ Analog input/output configurable

■ Alternate function input/output configurable

There are up to 26 general purpose I/O pins (GPIO) in GD32E231xx, named PA0 ~ PA10, PA12 ~ PA15 and PB0 ~ PB1, PB3 ~ PB8, PB15, PF0 ~ PF1 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull open-drain or analog), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.9 Timers and PWM generation

■ One 16-bit advanced timer (TIMER0), up to five 16-bit general timers (TIMER2, TIMER13 ~ TIMER16), and one 16-bit basic timer (TIMER5)

■ Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input

■ 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match

■ Encoder interface controller with two inputs using quadrature decoder

■ 24-bit SysTick timer down counter

■ 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 3 independent channels can be used for input capture, output compare, PWM generation (edge- or center- aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER2 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload up counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 can also be used as a simple 16-bit time base.

The GD32E231xx have two watchdog peripherals, free watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:
- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.10   Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.
- Calendar with subsecond, second, minute, hour, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.954

ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.11 Inter-integrated circuit (I2C)

■ Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
■ Provide arbitration function, optional PEC (packet error checking) generation and checking
■ Supports 7-bit and 10-bit addressing mode and general call addressing mode
■ Supports SAM_V mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.12 Serial peripheral interface (SPI)

■ Up to two SPI interfaces with a frequency of up to 18 MHz
■ Support both master and slave mode
■ Hardware CRC calculation and transmit automatic CRC error checking
■ Separate transmit and receive 32-bit FIFO with DMA capability (only in SPI1)
■ Data frame size can be 4 to 16 bits (only in SPI1)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Specially, SPI1 has separate transmit and receive 32-bit FIFO with DMA capability and its data frame size can be 4 to 16 bits.

3.13 Universal synchronous asynchronous receiver transmitter (USART)

■ Up to one USART with operating frequency up to 4.5 MBits/s
■ Supports both asynchronous and clocked synchronous serial communication modes
■ IrDA SIR encoder and decoder support
■ LIN break generation and detection
■ ISO 7816-3 compliant smart card interface

The USART (USART0) is used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.14 Inter-IC sound (I2S)

■ One I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI0
■ Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32E231xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI0. The audio sampling frequency from 8 KHz to 192 KHz is supported with less than 0.5% accuracy error.

3.15 Comparators (CMP)

■ One fast rail-to-rail low-power comparators with software configurable
■ Programmable reference voltage (internal or external I/O)

One Comparator (CMP) is implemented within the devices. It can wake up from deep-sleep mode to generate interrupts and breaks for the timers and also can be combined as a window comparator. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

3.16 Operational amplifier (OP-AMP)

■ Two 6.5MHz, rail-to-rail I/O CMOS operational amplifiers

- Low offset voltage: 1mV (typ)
- High gain: 104dB (typ)
- Low I_B: 5pA (typ)
- Low supply voltage: + 2.7 V to + 3.6V

Two operational amplifier (OP-AMP) are low noise, low voltage and low power operational amplifiers with high gain-bandwidth product of 6.5MHz and slew rate of 5V/μs. The maximum input offset voltage is only 3.5mV and the input common mode range extends beyond the supply rails.

3.17 Debug mode

- Serial wire debug port

Debug capabilities can be accessed by a debug tool via Serial Wire (SW - Debug Port).

3.18 Package and operation temperature

- QFN36 (GD32E231T8O6), QFN32 (GD32E231K8Q6).
- Operation temperature range: -40°C to +85°C (industrial level) for grade 6 devices.

4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings[1][4]

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range[2]	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin[3]	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V
$|\Delta V_{DDx}|$	Variations between different VDD power pins	—	50	mV
$|V_{SSX} - V_{SS}|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±25	mA
T_A	Operating temperature range	-40	+85	°C
P_D	Power dissipation at T_A = 85°C of QFN32	—	939	mW
	Power dissipation at T_A = 85°C of QFN36	—	845	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Guaranteed by design, not tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) V_{IN} maximum value cannot exceed 5.5 V.
(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

4.2 Operating conditions characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
V_{DD}	Supply voltage	—	1.8	3.3	3.6	V
V_{DDA}	Analog supply voltage ADC not used	—	1.8	3.3	3.6	V
	Analog supply voltage ADC used		2.4	3.3	3.6	

(1) Based on characterization, not tested in production.

Figure 4-1. Recommended power supply decoupling capacitors[1][2]
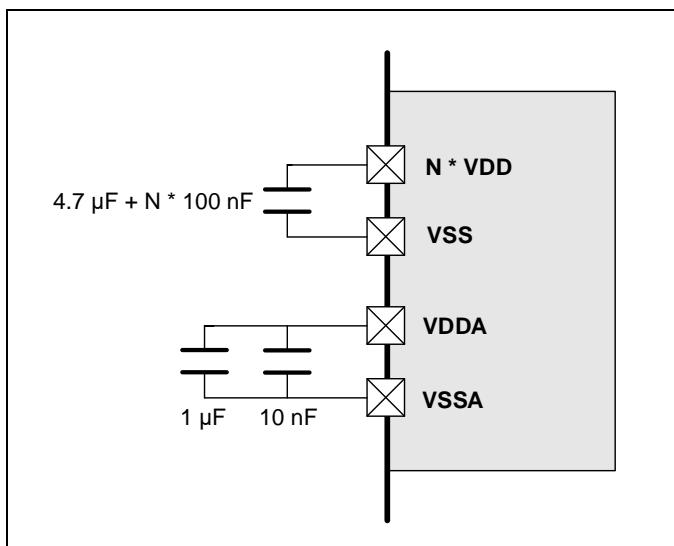
(1) More details refer to *AN074 GD32E23x Hardware Development Guide*.
(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK1}	AHB1 clock frequency	—	0	72	MHz
f_{HCLK2}	AHB2 clock frequency	—	0	72	MHz
f_{APB1}	APB1 clock frequency	—	0	72	MHz
f_{APB2}	APB2 clock frequency	—	0	72	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down[1]

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	μs /V
	V_{DD} fall time rate		20	∞	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions[1]

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	432	μs
		Clock source from IRC8M	76	

(1) Based on characterization, not tested in production.
(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.
(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics[1][2]

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	3.5	μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode（LDO On）	17.1	
	Wakeup from Deep-sleep mode（LDO in low power mode）	17.1	
$t_{Standby}$	Wakeup from Standby mode	77.5	

(1) Based on characterization, not tested in production.
(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: $V_{DD} = V_{DDA} = 3.3$ V, IRC8M = System clock = 8 MHz.

4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics[2][3][4][5]

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$I_{DD}+I_{DDA}$	Supply current (Run mode)	$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals enabled	—	8.7	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals disabled	—	5.8	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals enabled	—	6.6	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals disabled	—	4.6	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals enabled	—	5.5	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals disabled	—	4.0	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals enabled	—	4.4	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals disabled	—	3.4	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals enabled	—	3.6	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals disabled	—	3.0	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals enabled	—	3.1	—	mA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals disabled	-—	2.4	-—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals enabled	—	1.3	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals disabled	—	1.1	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 2 MHz, System clock = 2 MHz, All peripherals enabled	-—	1.1	-—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 2 MHz, System clock = 2 MHz, All peripherals disabled	—	1.0	—	mA
	Supply current (Sleep mode)	$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, CPU clock off, System clock = 72 MHz, All peripherals enabled	—	7.8	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, CPU clock off, System clock = 72 MHz, All peripherals disabled	—	4.2	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, CPU clock off, System clock = 48 MHz, All peripherals enabled	-—	6.0	-—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, CPU clock off, System clock = 48 MHz, All peripherals disabled	—	3.5	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, CPU clock off, System clock = 36 MHz, All peripherals enabled	—	5.0	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, CPU clock off, System clock = 36 MHz, All peripherals disabled	-—	3.2	-—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, CPU clock off, System clock = 24 MHz, All peripherals enabled	—	4.0	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, CPU clock off, System clock = 24 MHz, All peripherals disabled	—	2.9	—	mA
		$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 8 MHz, CPU clock off, System clock = 16 MHz, All peripherals enabled	-—	3.5	-—	mA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 16 MHz, All peripherals disabled	—	2.6	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 8 MHz, All peripherals enabled	—	2.7	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 8 MHz, All peripherals disabled	-—	2.3	-—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 4 MHz, CPU clock off, System clock = 4 MHz, All peripherals enabled	—	1.1	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 4 MHz, CPU clock off, System clock = 4 MHz, All peripherals disabled	—	0.9	—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 2 MHz, CPU clock off, System clock = 2 MHz, All peripherals enabled	-—	0.9	-—	mA
		$V_{DD} = V_{DDA}$ = 3.3 V, HXTAL = 2 MHz, CPU clock off, System clock = 2 MHz, All peripherals disabled	—	0.8	—	mA
	Supply current (Deep-sleep mode)	$V_{DD} = V_{DDA}$ = 3.3 V, LDO in normal power and normal driver mode, IRC40K off, RTC off	—	438.8	—	μA
		$V_{DD} = V_{DDA}$ = 3.3 V, LDO in normal power and low driver mode, IRC40K off, RTC off	—	425.4	—	μA
	Supply current (Standby mode)	$V_{DD} = V_{DDA}$ = 3.3 V, LXTAL off, IRC40K on, RTC on	—	417.8	—	μA
		$V_{DD} = V_{DDA}$ = 3.3 V, LXTAL off, IRC40K on, RTC off	—	417.3	—	μA
		$V_{DD} = V_{DDA}$ = 3.3 V, LXTAL off, IRC40K off, RTC off, VDDA Monitor on	—	416.9	—	μA
		$V_{DD} = V_{DDA}$ = 3.3 V, LXTAL off, IRC40K off, RTC off, VDDA Monitor off	—	416.8	—	μA

(1) Based on characterization, not tested in production.

(2) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(3) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

(4) When analog peripheral blocks such as ADCs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

(5) All GPIOs are configured as analog mode except standby mode.

Figure 4-2. Typical supply current consumption in Run mode
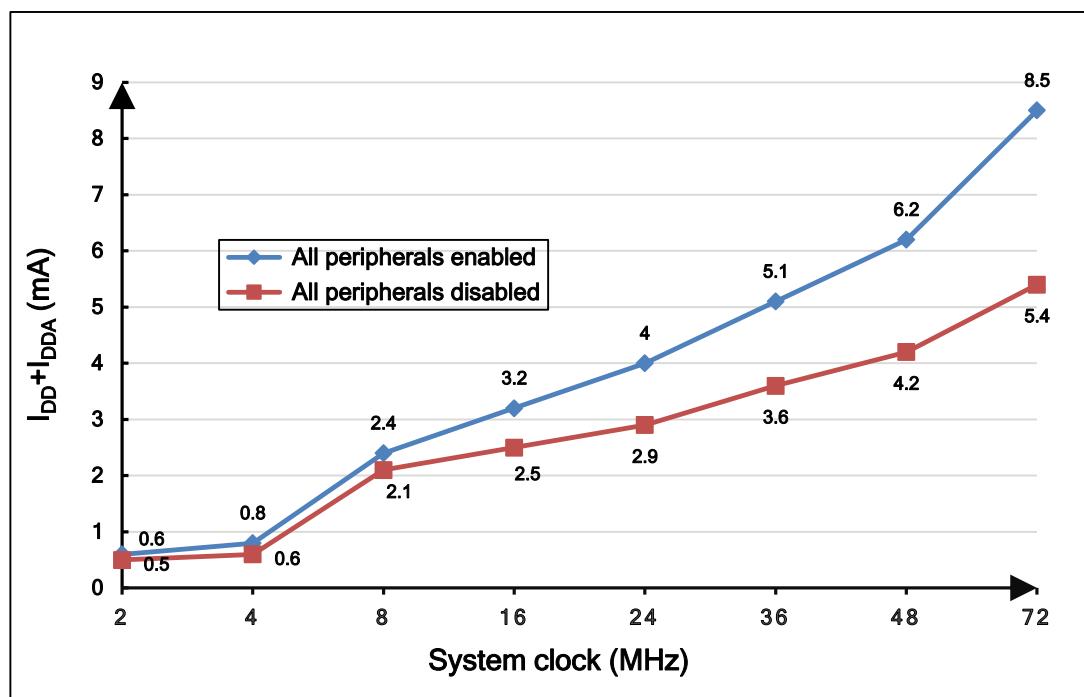
Figure 4-3. Typical supply current consumption in Sleep mode
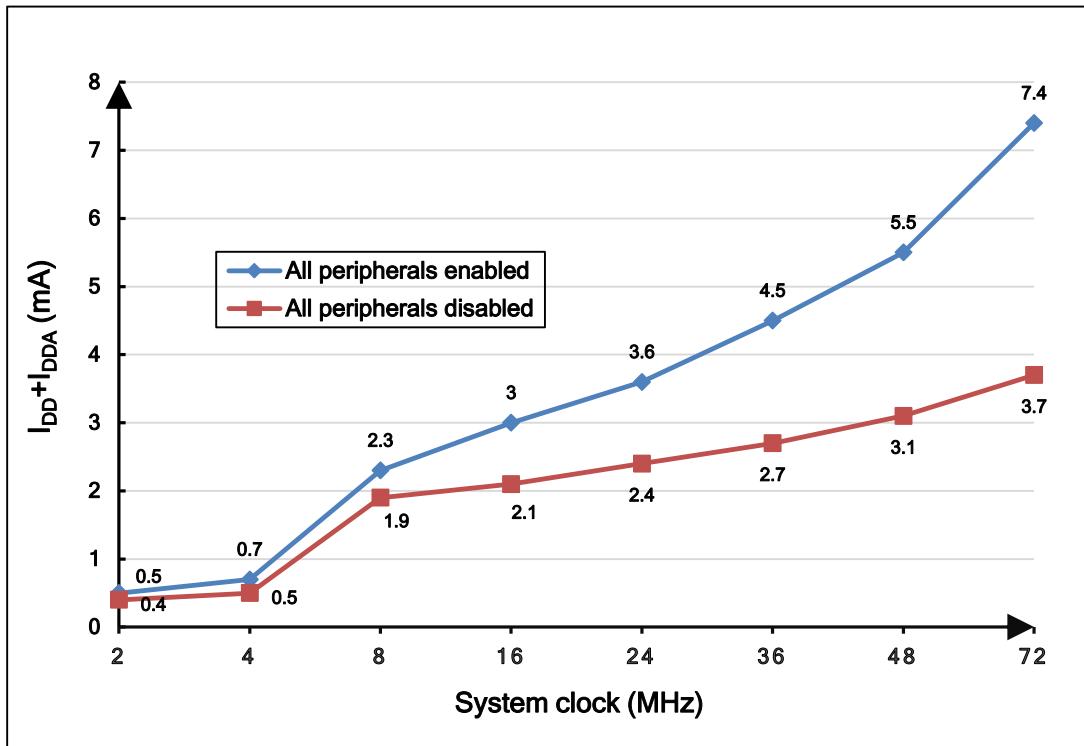
Table 4-8. Peripheral current consumption characteristics[1]

Peripherials[4]		Typical consumption	Unit
APB1	PMU	1.44	mA
	I2C1	1.38	
	I2C0	1.38	
	SPI1	1.37	
	WWDGT	1.32	
	TIMER13	1.36	
	TIMER5	0.17	
	TIMER2	0.23	
APB2	DBGMCU	1.3	
	TIMER16	1.42	
	TIMER15	1.42	
	TIMER14	1.49	
	USART0	1.63	
	SPI0	1.38	
	TIMER0	1.68	
	ADC[2]	0.95	
	CFG & CMP[3]	1.27	
AHB	GPIOF	1.31	
	GPIOC	1.31	
	GPIOB	1.34	
	GPIOA	1.34	
	CRC	0.16	
	DMA	0.15	

(1)   Based on characterization, not tested in production.

(2) f_{ADCCLK} = IRC28M, ADCON bit is set to 1.

(3)   CMP enabled by setting CMPEN bit in CMP_CS，CMP mode is set to High Speed.

(4)   If there is no other description, then V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, system clock = f_{HCLK} = 72 MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, f_{ADCCLK} = f_{APB2}/2.

4.4   EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in *__Table 4-9. EMS characteristics__*, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-9. EMS characteristics[1]

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3A
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on VDD and VSS pins	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

(1)   Based on characterization, not tested in production.

EMI (Electromagnetic Interference) emission test result is given in the **_Table 4-10. EMI characteristics_**[1], The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-10. EMI characteristics[1]

Symbol	Parameter	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}] 8/72 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-1.51	dBμV
			30 MHz to 130 MHz	3.02	
			130 MHz to 1 GHz	7.47	

(1)   Based on characterization, not tested in production.

4.5 Power supply supervisor characteristics

Table 4-11. Power supply supervisor characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}[1]	Low Voltage Detector Threshold	LVDT[2:0] = 000, rising edge	—	2.11	—	V
		LVDT[2:0] = 000, falling edge	—	2.01	—	V
		LVDT[2:0] = 001, rising edge	—	2.25	—	V
		LVDT[2:0] = 001, falling edge	—	2.16	—	V
		LVDT[2:0] = 010, rising edge	—	2.39	—	V
		LVDT[2:0] = 010, falling edge	—	2.29	—	V
		LVDT[2:0] = 011, rising edge	—	2.52	—	V
		LVDT[2:0] = 011, falling edge	—	2.43	—	V
		LVDT[2:0] = 100, rising edge	—	2.66	—	V
		LVDT[2:0] = 100, falling edge	—	2.57	—	V
		LVDT[2:0] = 101, rising edge	—	2.80	—	V
		LVDT[2:0] = 101, falling edge	—	2.71	—	V
		LVDT[2:0] = 110, rising edge	—	2.95	—	V
		LVDT[2:0] = 110, falling edge	—	2.84	—	V
		LVDT[2:0] = 111, rising edge	—	3.08	—	V
		LVDT[2:0] = 111, falling edge	—	2.98	—	V
$V_{LVDhyst}$[2]	LVD hysteresis	—	—	100	—	mV
V_{POR}[1]	Power on reset threshold		—	1.71	—	V
V_{PDR}[1]	Power down reset threshold	—	—	1.67	—	V
$V_{PDRhyst}$[2]	PDR hysteresis		—	40	—	mV
$t_{RSTTEMPO}$[2]	Reset temporization		—	2	—	ms

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up

(LU) test is based on the two measurement methods.

Table 4-12. ESD characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = 25\ °C$; JS-001-2017	—	—	6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = 25\ °C$; JS-002-2014	—	—	2000	V

(1)　Based on characterization, not tested in production.

Table 4-13. Static latch-up characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	$T_A = 25\ °C$; JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

(1)　Based on characterization, not tested in production.

4.7　External clock characteristics

Table 4-14. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}[1]	Crystal or ceramic frequency	$V_{DD} = 3.3\ V$	4	8	32	MHz
R_F[2]	Feedback resistor	$V_{DD} = 3.3\ V$	—	400	—	kΩ
C_{HXTAL}[2] [3]	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$[2]	Crystal or ceramic duty cycle	—	30	50	70	%
g_m[2]	Oscillator transconductance	Startup	—	25	—	mA/ V
$I_{DD(HXTAL)}$[1]	Crystal or ceramic operating current	$V_{DD} = 3.3\ V$	—	1.2	—	mA
$t_{SUHXTAL}$[1]	Crystal or ceramic startup time	$V_{DD} = 3.3\ V$	—	1.8	—	ms

(1)　Based on characterization, not tested in production.

(2)　Guaranteed by design, not tested in production.

(3)　$C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 4-15. High speed external user clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}[1]	External clock source or oscillator frequency	V_{DD} = 3.3 V	1	8	50	MHz
V_{HXTALH}[2]	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}[2]	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	
$t_{H/L(HXTAL)}$ [2]	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$[2]	OSCIN rise or fall time	—	—	—	10	
C_{IN}[2]	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$ [2]	Duty cycle	—	30	50	70	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-16. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}[1]	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}[2][3]	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	10	—	pF
$Ducy_{(LXTAL)}$[2]	Crystal or ceramic duty cycle	—	30	—	70	%
g_m[2]	Oscillator transconductance	Lower driving capability	—	4	—	µA/V
		Medium low driving capability	—	6	—	
		Medium high driving capability	—	12	—	
		Higher driving capability	—	18	—	
$I_{DDLXTAL}$ [1]	Crystal or ceramic operating current	Lower driving capability	—	0.5	—	µA
		Medium low driving capability	—	0.6	—	
		Medium high driving capability	—	1.0	—	
		Higher driving capability	—	1.2	—	
$t_{SULXTAL}$[1][4]	Crystal or ceramic startup time	V_{DD} = 3.3 V	—	1.8	—	s

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S), For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-17. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}[1]	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}[2]	OSC32IN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}[2]	OSC32IN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$[2]	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$[2]	OSC32IN rise or fall time	—	—	—	50	
C_{IN}[2]	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$[2]	Duty cycle	—	30	50	70	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.8 Internal clock characteristics

Table 4-18. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	8	—	MHz
ACC_{IRC8M}[1]	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	—	-0.525 to 0.275[1]	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.0	—	+1.0	
	IRC8M oscillator Frequency accuracy, User trimming step	—	—	0.5	—	%
D_{IRC8M}[2]	IRC8M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDIRC8M}$[1]	IRC8M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{IRC8M} = 8 MHz	—	55	—	µA
$t_{SUIRC8M}$[1]	IRC8M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{IRC8M} = 8 MHz	—	1.5	—	µs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-19. Low speed internal clock (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}[1]	Low Speed Internal oscillator (IRC40K) frequency	$V_{DD} = V_{DDA} = 3.3\ V$	—	40	—	kHz
$I_{DDIRC40K}$[2]	IRC40K oscillator operating current	$V_{DD} = V_{DDA} = 3.3\ V$	—	0.41	—	µA
$t_{SUIRC40K}$[2]	IRC40K oscillator startup time	$V_{DD} = V_{DDA} = 3.3\ V$	—	33	—	µs

(1)   Guaranteed by design, not tested in production.

(2)   Based on characterization, not tested in production.

Table 4-20. High speed internal clock (IRC28M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC28M}	High Speed Internal Oscillator (IRC28M) frequency	$V_{DD} = V_{DDA} = 3.3\ V$	—	28	—	MHz
ACC_{IRC28M}[1]	IRC28M oscillator Frequency accuracy, Factory-trimmed	$V_{DD} = V_{DDA} = 3.3\ V$, $T_A = -40\ °C \sim +85\ °C$	—	-0.975 to 0.782[1]	—	%
		$V_{DD} = V_{DDA} = 3.3\ V$, $T_A = 25\ °C$	-2.0	—	+2.0	
	IRC28M oscillator Frequency accuracy, User trimming step	—	—	0.5	—	%
D_{IRC28M}[2]	IRC28M oscillator duty cycle	$V_{DD} = V_{DDA} = 3.3\ V$	45	50	55	%
$I_{DDAIRC28M}$[1]	IRC28M oscillator operating current	$V_{DD} = V_{DDA} = 3.3\ V$, $f_{IRC28M} = 28\ MHz$	—	121	—	µA
$t_{SUIRC28M}$[1]	IRC28M oscillator startup time	$V_{DD} = V_{DDA} = 3.3\ V$, $f_{IRC28M} = 28\ MHz$	—	1.5	—	µs

(1)   Based on characterization, not tested in production.

(2)   Guaranteed by design, not tested in production.

4.9 PLL characteristics

Table 4-21. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}[1]	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}[2]	PLL output clock frequency	—	16	—	72	MHz
f_{VCO}[2]	PLL VCO output clock frequency	—	—	—	72	MHz
t_{LOCK}[2]	PLL lock time	—	—	—	300	µs
I_{DDA}[1]	Current consumption on V_{DDA}	VCO freq = 72 MHz	—	260	—	µA
$Jitter_{PLL}$[3]	Cycle to cycle Jitter（rms）	System clock	—	50	—	ps
	Cycle to cycle Jitter（peak to peak）		—	500	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Value given with main PLL running.

4.10 Memory characteristics

Table 4-22. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}[1]	Number of guaranteed program /erase cycles before failure (Endurance)	—	100	—	—	kcycles
t_{RET}[1]	Data retention time	—	10	—	—	years
t_{PROG}[2]	Word programming time	T_A = -40 °C ~ +85 °C	37	—	42	µs
t_{ERASE}[2]	Page erase time		3.2	—	4	ms
t_{MERASE}[2]	Mass erase time		8	—	10	ms

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.11 NRST pin characteristics

Table 4-23. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$[1]	NRST Input low level voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	-0.5	—	0.35 V_{DD}	V
$V_{IH(NRST)}$[1]	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}[1]	Schmidt trigger Voltage hysteresis		—	400	—	mV
R_{pu}[2]	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit
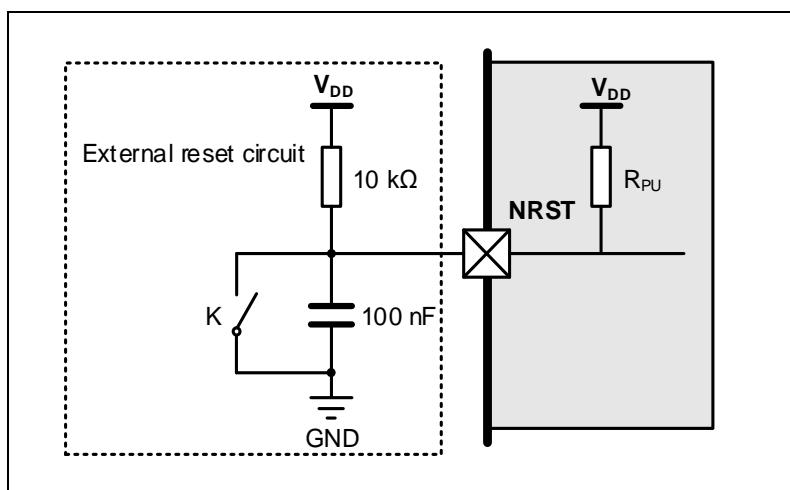
(1)   Unless the voltage on NRST pin go below VIL(NRST) level, the device would not generate a reliable reset.

4.12   GPIO characteristics

Table 4-24. I/O port DC characteristics[(1)(3)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
	5V-tolerant IO Low level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
V_{IH}	Standard IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
	5 V-tolerant IO High level input voltage	1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.8 V	—	—	0.20	V
		V_{DD} = 2.5 V	—	—	0.20	
		V_{DD} = 3.3 V	—	—	0.10	
		V_{DD} = 3.6 V	—	—	0.10	
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.8 V	—	—	—	V
		V_{DD} = 2.5 V	—	—	0.50	
		V_{DD} = 3.3 V	—	—	0.40	
		V_{DD} = 3.6 V	—	—	0.40	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.8 V	1.50	—	—	V
		V_{DD} = 2.5 V	2.30	—	—	
		V_{DD} = 3.3 V	3.10	—	—	
		V_{DD} = 3.6 V	3.40	—	—	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.8 V	—	—	—	V
		V_{DD} = 2.5 V	1.90	—	—	
		V_{DD} = 3.3 V	2.80	—	—	
		V_{DD} = 3.6 V	3.10	—	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}[2]	Internal pull-up resistor	—	—	40	—	kΩ
R_{PD}[2]	Internal pull-down resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

Table 4-25. I/O port AC characteristics[1][2]

GPIOx_OSPD[1:0] bit value[3]	Parameter	Conditions	Max	Unit
GPIOx_OSPD0->OSPDy[1:0] = X0 （IO_Speed = 2 MHz）	Maximum frequency[4]	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	4	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	3	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	2	
GPIOx_OSPD0->OSPDy[1:0] = 01 （IO_Speed = 10 MHz）	Maximum frequency[4]	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	24	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	16	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	14	
GPIOx_OSPD0->OSPDy[1:0] = 11 （IO_Speed = 50 MHz）	Maximum frequency[4]	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	72	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	72	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	72	

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all test results given for T_A = 25 °C.

(3) The I/O speed is configured using the GPIOx_OSPD0->OSPDy [1:0] bits. Refer to the GD32E23x user manual which is selected to set the GPIO port output speed.

(4) The maximum frequency is defined in Figure 4-5, and maximum frequency cannot exceed 72 MHz.

Figure 4-5. I/O port AC characteristics definition

If $(t_r + t_f) \leqslant$ 2/3 T, then maximum frequency is achieved .
The duty cycle is （45%-55%） when loaded by 50 pF
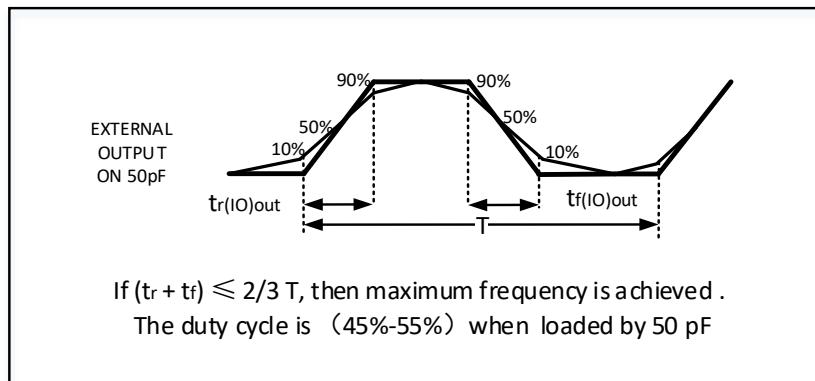
4.13   ADC characteristics

Table 4-26. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}[1]	Operating voltage	—	2.4	3.3	3.6	V
V_{IN}[1]	ADC input voltage range	—	0	—	V_{DDA}	V
f_{ADC}[1]	ADC clock	—	0.1	—	28	MHz
f_S[1]	Sampling rate	12-bit	0.007	—	2	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		10-bit	0.008	—	2.3	MSPS
		8-bit	0.01	—	2.8	
		6-bit	0.011	—	3.5	
V_{AIN}[1]	Analog input voltage	10 external; 2 internal	0	—	V_{DDA}	V
R_{AIN}[2]	External input impedance	See **Equation 1**	—	—	219.86	kΩ
R_{ADC}[2]	Input sampling switch resistance	—	—	—	0.5	kΩ
C_{ADC}[2]	Input sampling capacitance	No pin/pad capacitance included	—	—	4	pF
t_{CAL}[2]	Calibration time	f_{ADC} = 28 MHz	—	4.68	—	µs
t_s[2]	Sampling time	f_{ADC} = 28 MHz	0.05	—	8.55	µs
t_{CONV}[2]	Total conversion time(including sampling time)	12-bit	—	14	—	1/ f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}[2]	Startup time	—	—	—	1	µs

(1)   Based on characterization, not tested in production.

(2)   Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula $R_{AIN} < \dfrac{T_s}{f_{ADC}*C_{ADC}*\ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-27. ADC R_{AIN} max for f_{ADC} = 28 MHz[1]

T_s(cycles)	t_s(µs)	R_{AINmax} (kΩ)
1.5	0.05	0.88
7.5	0.27	6.40
13.5	0.48	11.92
28.5	1.02	25.72
41.5	1.48	37.68
55.5	1.98	50.56
71.5	2.55	65.29
239.5	8.55	219.86

(1)   Based on characterization, not tested in production.

Table 4-28. Internal reference voltage calibration values[2][3]

Symbol	Test conditions	Memory address
V_{REFINT}[1]	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V (± 3.65 mV), Temperature = 25 °C (± 4 °C)	0x1FFFF7C0-0x1FFFF7C4

(1) V_{REFINT} is internally connected to the ADC_IN17 input channel.

(2)   Low bit data is placed at the low bit address, and high bit data is placed at the high bit address.

(3)   Chip temperature calibration error is less than ±10mV.

Table 4-29. ADC dynamic accuracy at f$_{ADC}$ = 14 MHz[1]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f$_{ADC}$ = 14 MHz	—	10.2	—	bits
SNDR	Signal-to-noise and distortion ratio	V$_{DDA}$ = V$_{REFP}$ = 3.3 V	—	63.16	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	64.20	—	
THD	Total harmonic distortion	Temperature = 25 °C	—	-71.17	—	

(1) Based on characterization, not tested in production.

Table 4-30. ADC static accuracy at f$_{ADC}$ = 14 MHz[1]

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f$_{ADC}$ = 14 MHz	±1	—	LSB
DNL	Differential linearity error	V$_{DDA}$ = V$_{REFP}$ = 3.3 V	±1.5	—	
INL	Integral linearity error		±3	—	

(1) Based on characterization, not tested in production.

4.14 Temperature sensor characteristics

Table 4-31. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T$_L$[1]	V$_{SENSE}$ linearity with temperature	—	±1.5	—	°C
Avg_Slope[1]	Average slope	—	4.3	—	mV/°C
V$_{25}$[1]	Voltage at 25 °C	—	1.45	—	V
t$_{S\_temp}$[2]	ADC sampling time when reading the temperature	—	17.1	—	µs

(4) Based on characterization, not tested in production.
(5) Shortest sampling time can be determined in the application by multiple iterations.

4.15 Comparators characteristics

Table 4-32. CMP characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V$_{DDA}$	Operating voltage	—	1.8	3.3	3.6	V
V$_{IN}$	Input voltage range	—	0	—	V$_{DDA}$	V
V$_{BG}$	Scaler input voltage	—	—	1.2	—	V
V$_{SC}$	Scaler offset voltage	—	—	—	—	mV
t$_D$	Propagation delay for 200 mV step with 100 mV overdrive	Ultra low power mode	—	0.98	—	µs
		Low power mode	—	0.25	—	µs
		Medium power mode	—	0.12	—	µs
		High speed power mode	—	33	—	ns
	Propagation delay for full range step with 100 mV overdrive	Ultra low power mode	—	—	—	µs
		Low power mode	—	—	—	µs
		Medium power mode	—	—	—	µs
		High speed power mode	—	—	—	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Current consumption	Ultra low power mode	—	2.2	—	µA
		Low power mode	—	3.2	—	
		Medium power mode	—	8.1	—	
		High speed power mode	—	46.9	—	
V_{offset}	Offset error	—	—	±4	—	mV
V_{hyst}	Hysteresis Voltage	No Hysteresis	—	0	—	mV
		Low Hysteresis	—	11	—	
		Medium Hysteresis	—	22	—	
		High Hysteresis	—	43	—	

(1)   Based on characterization, not tested in production.

Figure 4-6. CMP hysteresis
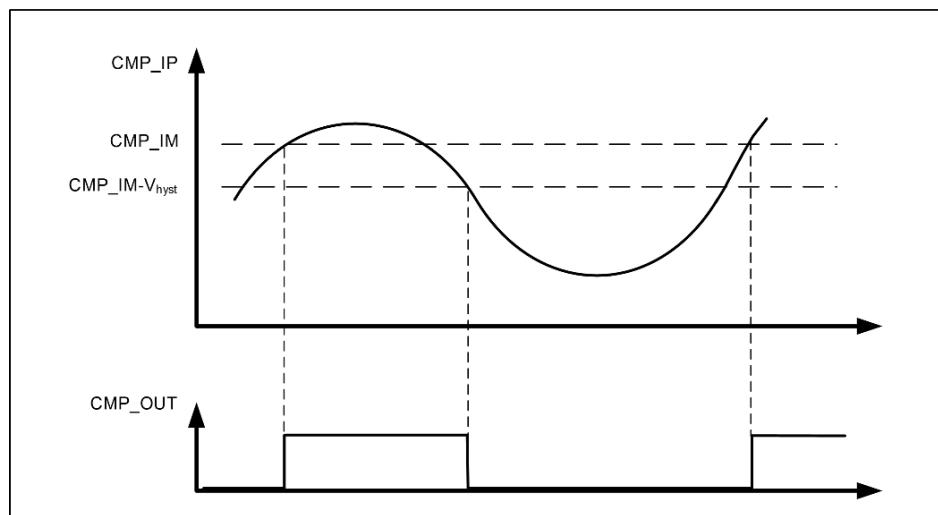
4.16   Operational amplifier characteristics

Table 4-33. OP-AMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage	—	2.7	—	3.6	V
V_{in}	Input voltage range	—	V_{SS} - 0.2	—	V_{DD} + 0.2	V
I_{DD}	Operating current	Io = 0	—	580	750	µA
I_{Load}	Drive current	—	—	—	—	mA
V_{os}	Offset voltage	—	—	1	3.5	mV
T_s	Settling time to 0.1%	Gain = 1, V_{out} = 2V step	—	1	—	µs
	Settling time to 0.1%	Gain = 1, V_{out} = 2V step	—	1.5	—	µs
	Overload Recovery Time	V_{in} *Gain > V_{DD}	—	0.2	—	µs
SR	Slew rate	Gain = 1	—	5	—	V/µs
CMRR	Common mode rejection	—	58	72	—	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	ratio					
PSRR	Power supply rejection ratio	—	—	25	150	uV/V
GBW	Gain bandwidth	—	—	6.5	—	MHz
A0	Open-loop gain	R_L = 5 kΩ	85	104	—	dB
V_{out}	Output swing from rail	R_L = 5 kΩ	—	100	125	mV
V_{noise}	Input voltage noise	F = 0.1 Hz to 10 Hz	—	5	—	µVpp
e_n	Input voltage noise density	F = 10 kHz	—	15	—	nV/√Hz

4.17 TIMER characteristics

Table 4-34. TIMER characteristics[1]

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 72 MHz	13.9	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}$/2	MHz
		$f_{TIMERxCLK}$ = 72 MHz	0	36	MHz
RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count	—	—	65536 x 65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 72 MHz	—	59.6	s

(1)   Guaranteed by design, not tested in production.

4.18   I2C characteristics

Table 4-35. I2C characteristics[1][2]

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	µs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	µs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0[3]	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	µs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	µs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	µs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	µs

(1)   Guaranteed by design, not tested in production.

(2)   To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz, To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3)   The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-7. I2C bus timing diagram
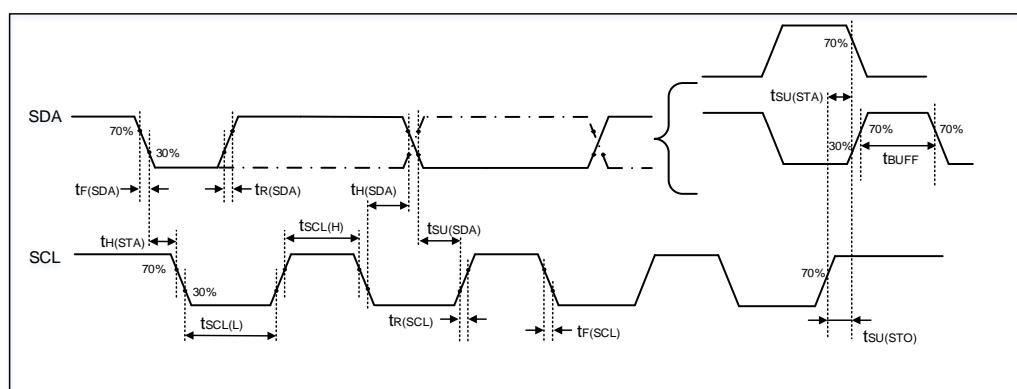
4.19   SPI characteristics

Table 4-36. Standard SPI characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	18	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 72 MHz, presc = 4	25	27	29	ns
$t_{SCK (L)}$	SCK clock low time	Master mode, f_{PCLKx} = 72 MHz, presc = 4	25	27	29	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	2	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	7	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	8	—	ns
$t_{V(SO)}$	Data output valid time	—	—	10	—	ns
$t_{SU(SI)}$	Data input setup time	—	—	10	—	ns
$t_{H(SI)}$	Data input hold time	—	0	—	—	ns

(1)   Based on characterization, not tested in production.

**Figure 4-8. SPI timing diagram - master mode**
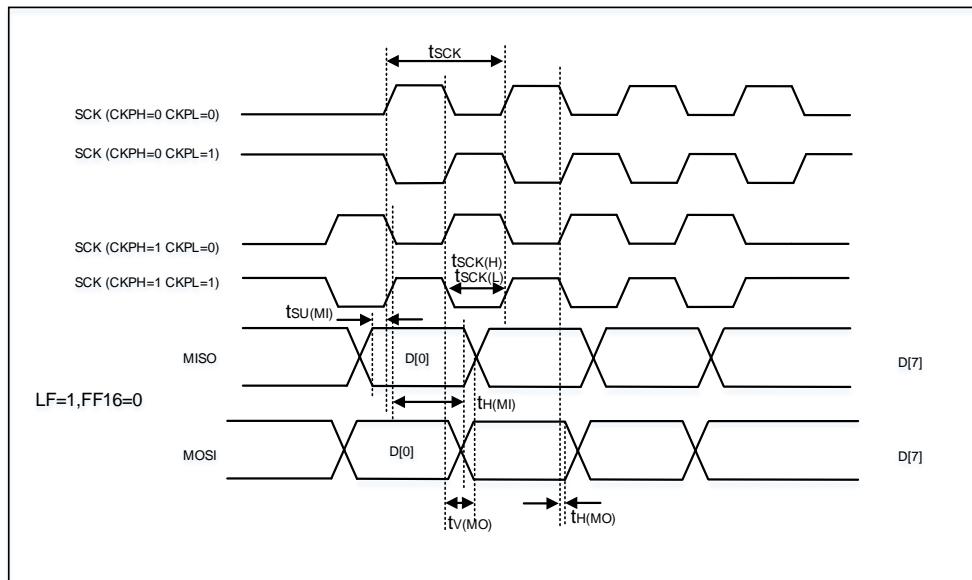
Figure 4-9. SPI timing diagram - slave mode
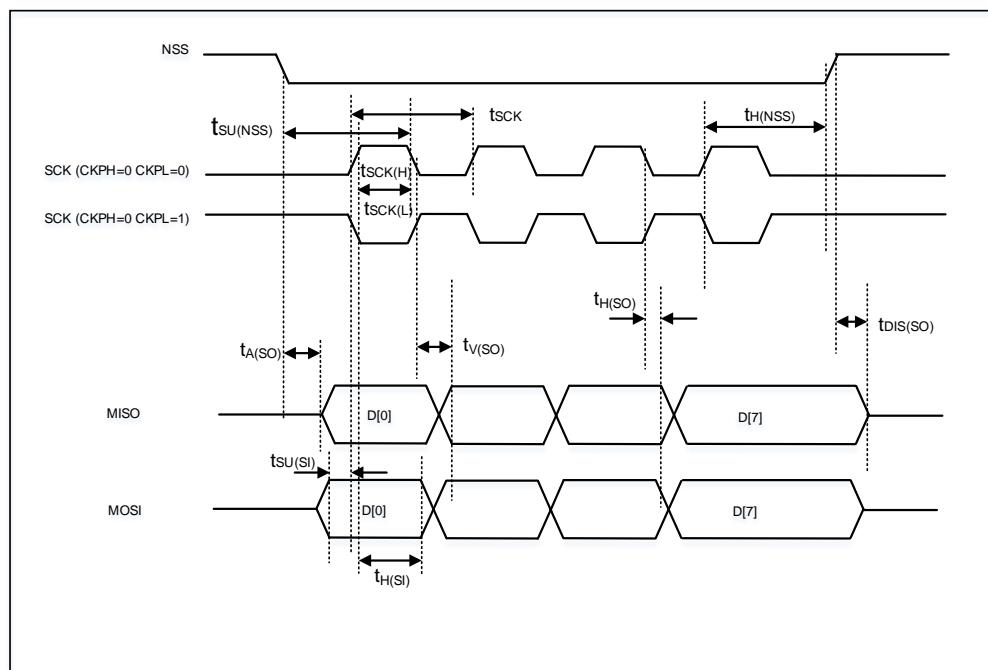
4.20 I2S characteristics

Table 4-37. I2S characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	—	3.12	—	MHz
		Slave mode	—	10	—	
t_H	Clock high time	—	—	160	—	ns
t_L	Clock low time		—	160	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$Ducy_{(sck)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	0	—	—	ns
$t_{SU(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	2	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	2	—	—	ns
$t_{V(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	12	—	ns
$t_{H(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	—	10	—	ns
$t_{V(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	10	—	ns
$t_{H(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	—	7	—	ns

(1) Based on characterization, not tested in production.

**Figure 4-10. I2S timing diagram - master mode**
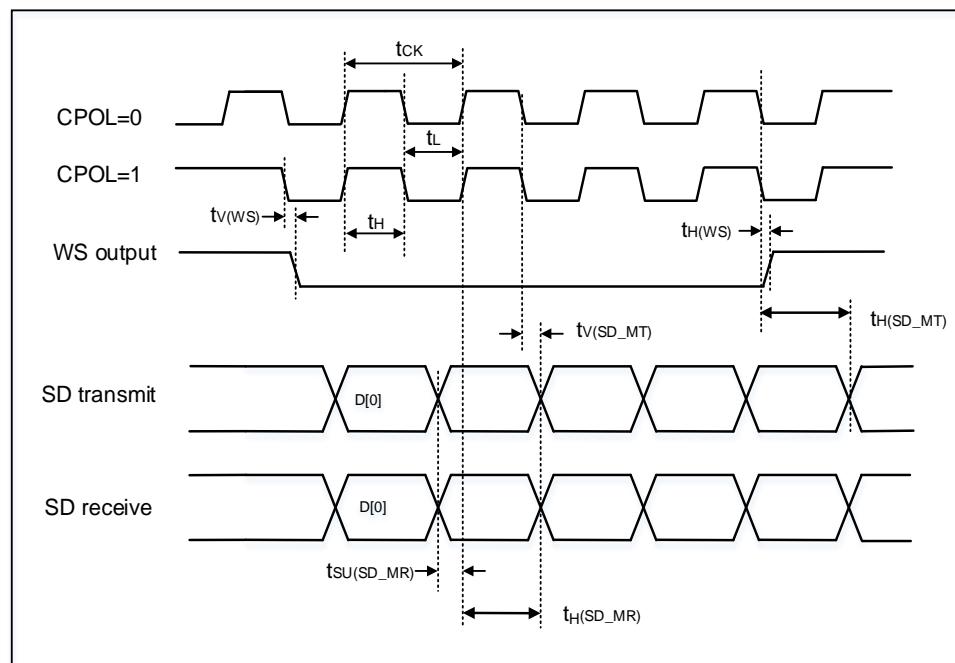
Figure 4-11. I2S timing diagram - slave mode
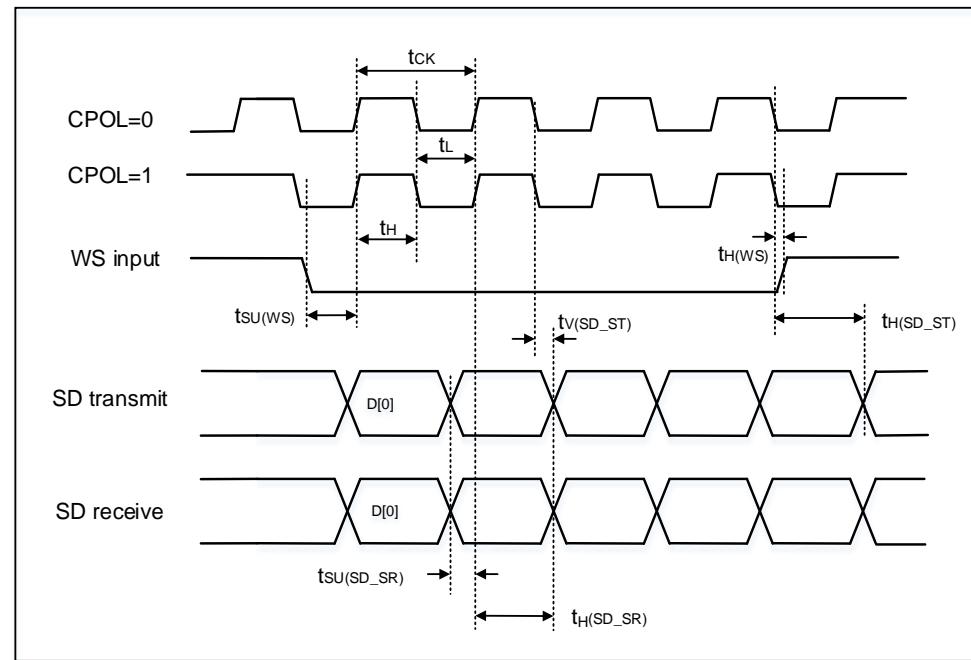
4.21 USART characteristics

Table 4-38. USART characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	36	MHz
$t_{SCK(H)}$	SCK clock high time	—	13.5	—	—	ns
$t_{SCK(L)}$	SCK clock low time	—	13.5	—	—	ns

(1) Guaranteed by design, not tested in production.

4.22 WDGT characteristics

Table 4-39. FWDGT min/max timeout period at 40 kHz (IRC40K)[1]

Prescaler divider	PR[2:0] bits	Min timeout RLD[11:0]= 0x000	Max timeout RLD[11:0]= 0xFFF	Unit
1/4	000	0.025	409.525	
1/8	001	0.025	819.025	
1/16	010	0.025	1638.025	
1/32	011	0.025	3276.025	ms
1/64	100	0.025	6552.025	
1/128	101	0.025	13104.025	
1/256	110 or 111	0.025	26208.025	

(1) Guaranteed by design, not tested in production.

Table 4-40. WWDGT min-max timeout value at 72 MHz (f_{PCLK1})[1]

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	56		3.64	
1/2	01	113	μs	7.28	ms
1/4	10	227		14.56	
1/8	11	455		29.12	

(1) Guaranteed by design, not tested in production.

4.23 Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C.

5 Package information

## 5.1 QFN32 package outline dimensions

Figure 5-1. QFN32 package outline
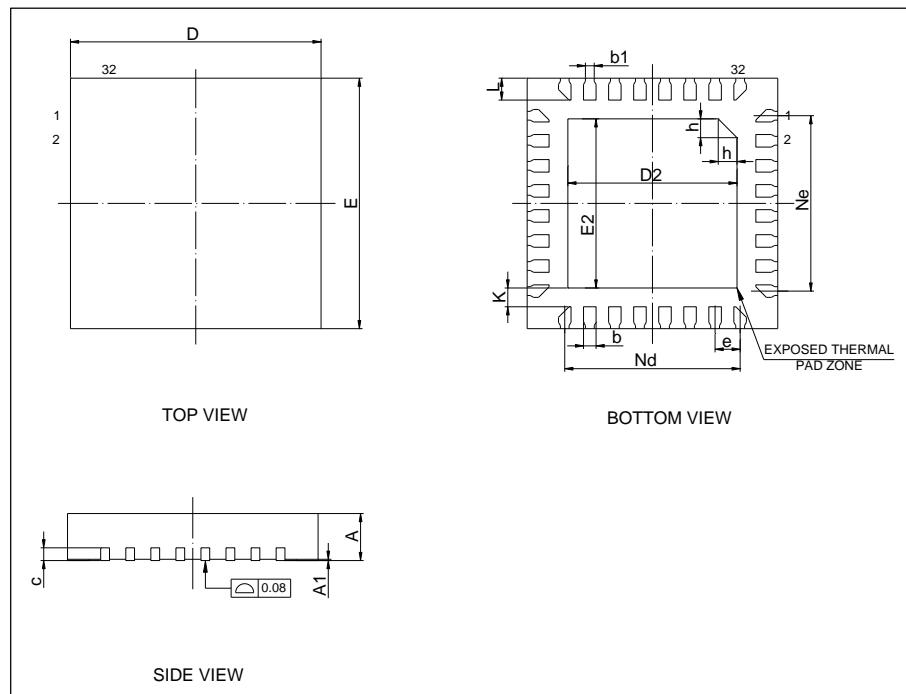
Table 5-1. QFN32 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	—	0.14	—
c	—	0.20	—
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
e	—	0.40	—
h	0.25	0.30	0.35
K	—	0.30	—
L	0.30	0.35	0.40
Nd	—	2.80	—
Ne	—	2.80	—

(Original dimensions are in millimeters)

Figure 5-2. QFN32 recommended footprint
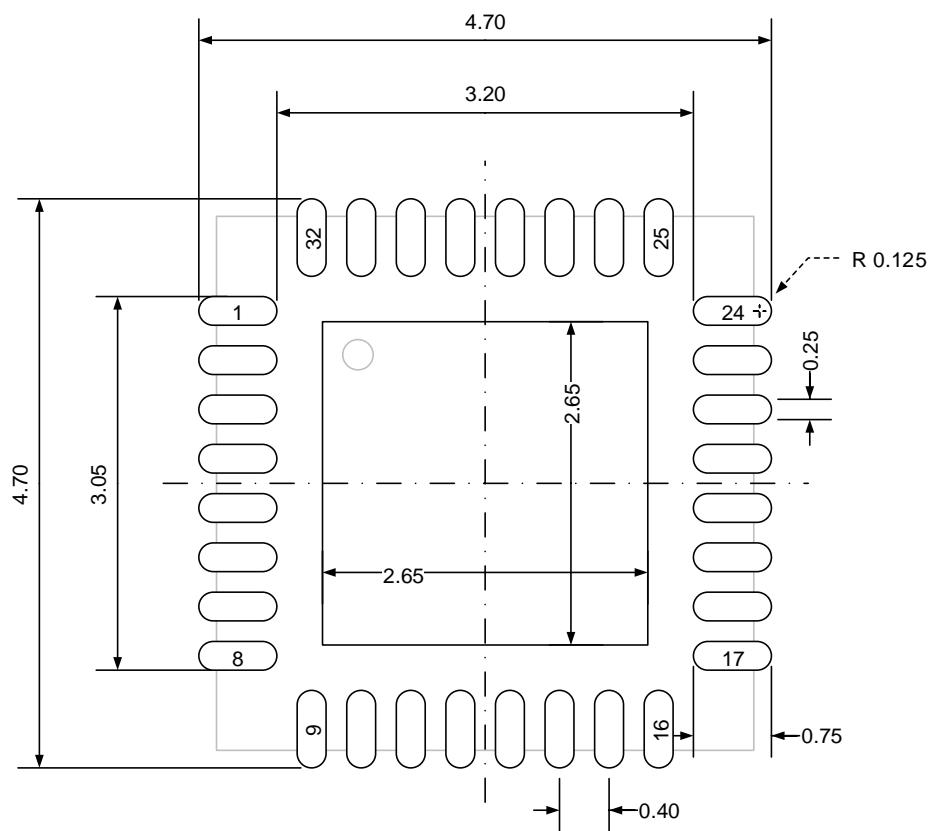
(Original dimensions are in millimeters)

5.2 QFN36 package outline dimensions

Figure 5-3. QFN36 package outline

TOP VIEW

BOTTOM VIEW

SIDE VIEW
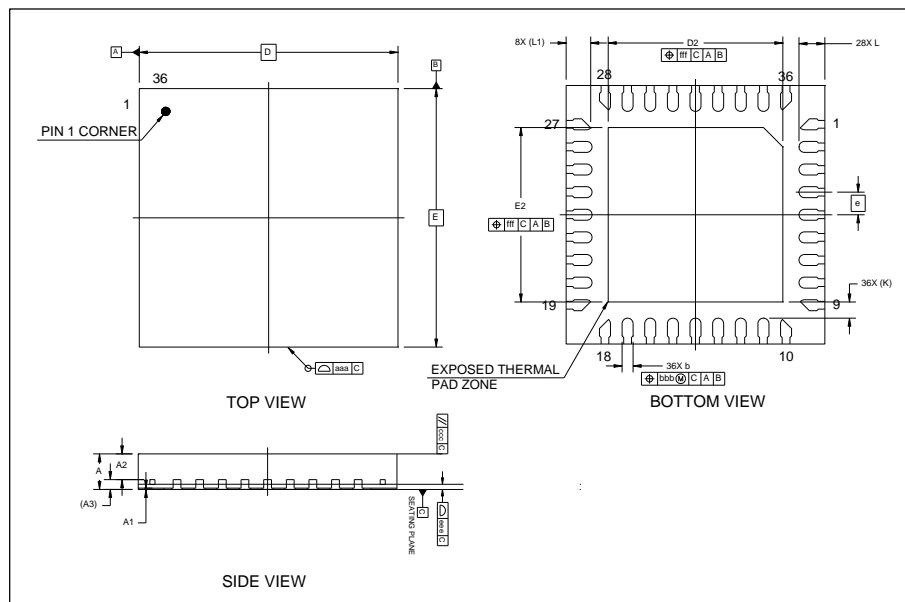
Table 5-2. QFN36 package dimensions

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A2	—	0.40	—
A3	—	0.152	—
b	0.12	0.17	0.22
D	—	4.00	—
D2	2.60	2.70	2.80
E	—	4.00	—
E2	2.60	2.70	2.80
e	—	0.35	—
K	—	0.27	—
L	0.30	0.40	0.50
L1	—	0.38	—
aaa	—	0.10	—
bbb	—	0.07	—
ccc	—	0.10	—
eee	—	0.08	—
fff	—	0.10	—

(Original dimensions are in millimeters)

Figure 5-4. QFN36 recommended footprint
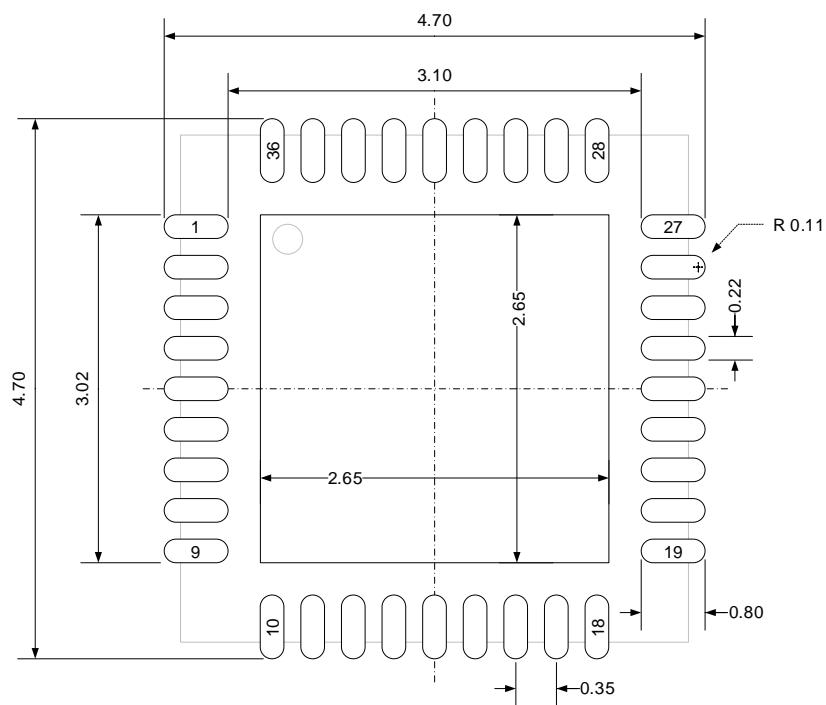
(Original dimensions are in millimeters)

5.3   Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \tag{5-1}$$

$$\theta_{JB}=(T_J-T_B)/P_D \tag{5-2}$$

$$\theta_{JC}=(T_J-T_C)/P_D \tag{5-3}$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-3. Package thermal characteristics[1]

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	QFN32	42.57	°C/W
		QFN36	47.32	
θ_{JB}	Cold plate, 2S2P PCB	QFN32	19.21	°C/W
		QFN36	12.97	
θ_{JC}	Cold plate, 2S2P PCB	QFN32	19.10	°C/W
		QFN36	20.26	
Ψ_{JB}	Natural convection, 2S2P PCB	QFN32	19.18	°C/W

Symbol	Condition	Package	Value	Unit
		QFN36	13.07	
Ψ_{JT}	Natural convection, 2S2P PCB	QFN32	0.62	°C/W
		QFN36	0.75	

(1). Thermal characteristics are based on simulation, and meet JEDEC specification.

6   Ordering information

Table 6-1. Part ordering code for GD32E231xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32E231K8Q6	64	QFN32	Green	Industrial -40 °C to +85 °C
GD32E231T8O6	64	QFN36	Green	Industrial -40 °C to +85 °C

7 Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov.8, 2023
1.1	Update OPA pins name	Nov.24, 2023
1.2	Add GD32E231T8O6 series	Jan.15, 2024
1.3	1. Update GD32E231T8O6 ***Device information*** 2. Update POD information, refer to ***Package information*** 3. Add ***Table 7-2. Internal reference voltage calibration values***[(2)(3)]	Sep.2, 2024

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