

**GigaDevice Semiconductor Inc.**

**GD32F130xx**

**Arm<sup>®</sup> Cortex<sup>®</sup>-M3 32-bit MCU**

**Datasheet**

Revision 3.9

(Dec. 2023)

## Table of Contents

|  |           |
|--|-----------|
| <b>Table of Contents</b> .....                           | <b>1</b>  |
| <b>List of Figures</b> .....                             | <b>4</b>  |
| <b>List of Tables</b> .....                              | <b>5</b>  |
| <b>1. General description</b> .....                      | <b>7</b>  |
| <b>2. Device overview</b> .....                          | <b>8</b>  |
| <b>2.1. Device information</b> .....                     | <b>8</b>  |
| <b>2.2. Block diagram</b> .....                          | <b>9</b>  |
| <b>2.3. Pinouts and pin assignment</b> .....             | <b>10</b> |
| <b>2.4. Memory map</b> .....                             | <b>13</b> |
| <b>2.5. Clock tree</b> .....                             | <b>15</b> |
| <b>2.6. Pin definitions</b> .....                        | <b>16</b> |
| 2.6.1. GD32F130R8 LQFP64 pin definitions .....           | 16        |
| 2.6.2. GD32F130Cx LQFP48 pin definitions .....           | 20        |
| 2.6.3. GD32F130Kx LQFP32 pin definitions .....           | 23        |
| 2.6.4. GD32F130Kx QFN32 pin definitions .....            | 25        |
| 2.6.5. GD32F130Gx QFN28 pin definitions .....            | 29        |
| 2.6.6. GD32F130Fx TSSOP20 pin definitions .....          | 31        |
| 2.6.7. GD32F130xx pin alternate functions .....          | 33        |
| <b>3. Functional description</b> .....                   | <b>37</b> |
| <b>3.1. Arm® Cortex®-M3 core</b> .....                   | <b>37</b> |
| <b>3.2. On-chip memory</b> .....                         | <b>37</b> |
| <b>3.3. Clock, reset and supply management</b> .....     | <b>38</b> |
| <b>3.4. Boot modes</b> .....                             | <b>38</b> |
| <b>3.5. Power saving modes</b> .....                     | <b>39</b> |
| <b>3.6. Analog to digital converter (ADC)</b> .....      | <b>39</b> |
| <b>3.7. DMA</b> .....                                    | <b>40</b> |
| <b>3.8. General-purpose inputs/outputs (GPIOs)</b> ..... | <b>40</b> |
| <b>3.9. Timers and PWM generation</b> .....              | <b>40</b> |
| <b>3.10. Real time clock (RTC)</b> .....                 | <b>41</b> |
| <b>3.11. Inter-integrated circuit (I2C)</b> .....        | <b>42</b> |
| <b>3.12. Serial peripheral interface (SPI)</b> .....     | <b>42</b> |

|       |   |    |
|-------|---|----|
| 3.13. | Universal synchronous asynchronous receiver transmitter (USART) ..... | 42 |
| 3.14. | Debug mode .....  | 43 |
| 3.15. | Package and operation temperature.....                                | 43 |
| 4.    | Electrical characteristics.....                                       | 44 |
| 4.1.  | Absolute maximum ratings.....   | 44 |
| 4.2.  | Operating conditions characteristics.....                             | 44 |
| 4.3.  | Power consumption .....   | 46 |
| 4.4.  | EMC characteristics .....   | 49 |
| 4.5.  | Power supply supervisor characteristics .....                         | 51 |
| 4.6.  | Electrical sensitivity .....  | 52 |
| 4.7.  | External clock characteristics .....                                  | 52 |
| 4.8.  | Internal clock characteristics .....                                  | 54 |
| 4.9.  | PLL characteristics.....  | 55 |
| 4.10. | Memory characteristics .....  | 56 |
| 4.11. | NRST pin characteristics .....  | 56 |
| 4.12. | GPIO characteristics .....  | 57 |
| 4.13. | ADC characteristics .....   | 59 |
| 4.14. | Temperature sensor characteristics.....                               | 59 |
| 4.15. | I2C characteristics .....   | 60 |
| 4.16. | USART characteristics.....  | 61 |
| 4.17. | TIMER characteristics.....  | 61 |
| 4.18. | WDGT characteristics.....   | 61 |
| 4.19. | Parameter conditions.....   | 62 |
| 5.    | Package information.....  | 63 |
| 5.1.  | LQFP64 package outline dimensions.....                                | 63 |
| 5.2.  | LQFP48 package outline dimensions.....                                | 65 |
| 5.3.  | LQFP32 package outline dimensions.....                                | 67 |
| 5.4.  | QFN32 package outline dimensions .....                                | 69 |
| 5.5.  | QFN28 package outline dimensions .....                                | 71 |
| 5.6.  | TSSOP20 package outline dimensions .....                              | 73 |
| 5.7.  | Thermal characteristics .....   | 75 |
| 6.    | Ordering information .....  | 77 |

---

**7. Revision history ..... 78**

## List of Figures

|   |    |
|---|----|
| Figure 2-1. GD32F130xx block diagram .....                                      | 9  |
| Figure 2-2. GD32F130Rx LQFP64 pinouts .....                                     | 10 |
| Figure 2-3. GD32F130Cx LQFP48 pinouts .....                                     | 10 |
| Figure 2-4. GD32F130Kx LQFP32 pinouts .....                                     | 11 |
| Figure 2-5. GD32F130Kx QFN32 pinouts .....                                      | 11 |
| Figure 2-6. GD32F130Gx QFN28 pinouts .....                                      | 12 |
| Figure 2-7. GD32F130Fx TSSOP20 pinouts .....                                    | 12 |
| Figure 2-8. GD32F130xx clock tree .....   | 15 |
| Figure 4-1. Recommended power supply decoupling capacitors <sup>(1)</sup> ..... | 45 |
| Figure 4-2. Typical supply current consumption in Run mode .....                | 49 |
| Figure 4-3. Typical supply current consumption in Sleep mode .....              | 49 |
| Figure 4-4. Recommended external NRST pin circuit <sup>(1)</sup> .....          | 57 |
| Figure 4-5. I2C bus timing diagram .....  | 60 |
| Figure 5-1. LQFP64 package outline .....  | 63 |
| Figure 5-2. LQFP64 recommended footprint .....                                  | 64 |
| Figure 5-3. LQFP48 package outline .....  | 65 |
| Figure 5-4. LQFP48 recommended footprint .....                                  | 66 |
| Figure 5-5. LQFP32 package outline .....  | 67 |
| Figure 5-6. LQFP32 recommended footprint .....                                  | 68 |
| Figure 5-7. QFN32 package outline .....   | 69 |
| Figure 5-8. QFN32 recommended footprint .....                                   | 70 |
| Figure 5-9. QFN28 package outline .....   | 71 |
| Figure 5-10. QFN28 recommended footprint .....                                  | 72 |
| Figure 5-11. TSSOP20 package outline .....                                      | 73 |
| Figure 5-12. TSSOP20 recommended footprint .....                                | 74 |

## List of Tables

|  |    |
|--|----|
| Table 2-1. GD32F130xx devices features and peripheral list .....   | 8  |
| Table 2-2. GD32F130xx memory map .....   | 13 |
| Table 2-3. GD32F130R8 LQFP64 pin definitions .....   | 16 |
| Table 2-4. GD32F130Cx LQFP48 pin definitions .....   | 20 |
| Table 2-5. GD32F130Kx LQFP32 pin definitions .....   | 23 |
| Table 2-6. GD32F130Kx QFN32 pin definitions .....  | 25 |
| Table 2-7. GD32F130Gx QFN28 pin definitions .....  | 29 |
| Table 2-8. GD32F130Fx TSSOP20 pin definitions .....  | 31 |
| Table 2-9. Port A alternate functions summary .....  | 33 |
| Table 2-10. Port B alternate functions summary .....   | 34 |
| Table 2-11. Port C & D & F alternate functions summary .....   | 36 |
| Table 4-1. Absolute maximum ratings <sup>(1)(4)</sup> .....  | 44 |
| Table 4-2. DC operating conditions .....   | 44 |
| Table 4-3. Clock frequency <sup>(1)</sup> .....  | 45 |
| Table 4-4. Operating conditions at Power up/ Power down <sup>(1)</sup> .....                             | 45 |
| Table 4-5. Start-up timings of Operating conditions <sup>(1)(2)(3)</sup> .....                           | 45 |
| Table 4-6. Power saving mode wakeup timings characteristics <sup>(1)(2)</sup> .....                      | 45 |
| Table 4-7. Power consumption characteristics <sup>(2)(3)(4)(5)</sup> .....                               | 46 |
| Table 4-8. EMS characteristics <sup>(1)</sup> .....  | 50 |
| Table 4-9. EMI characteristics <sup>(1)</sup> .....  | 50 |
| Table 4-10. Power supply supervisor characteristics .....  | 51 |
| Table 4-11. ESD characteristics .....  | 52 |
| Table 4-12. Static latch-up characteristics .....  | 52 |
| Table 4-13. High speed crystal oscillator (HXTAL) generated from a crystal/ceramic characteristics ..... | 52 |
| Table 4-14. High speed external clock characteristics (HXTAL in bypass mode) .....                       | 53 |
| Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics .....      | 53 |
| Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode) .....                   | 54 |
| Table 4-17. Internal 8 MHz RC oscillator (IRC8M) characteristics .....                                   | 54 |
| Table 4-18. Internal 40KHz RC oscillator (IRC40K) characteristics .....                                  | 54 |
| Table 4-19. High speed internal clock (IRC14M) characteristics .....                                     | 55 |
| Table 4-20. PLL characteristics .....  | 55 |
| Table 4-21. Flash memory characteristics .....   | 56 |
| Table 4-22. NRST pin characteristics .....   | 56 |
| Table 4-23. I/O port DC characteristics <sup>(1)(3)</sup> .....  | 57 |
| Table 4-24. I/O port AC characteristics <sup>(1)(2)(4)</sup> .....                                       | 58 |
| Table 4-25. ADC characteristics .....  | 59 |
| Table 4-26. ADC $R_{AIN\ max}$ for $f_{ADC} = 14\ MHz$ .....   | 59 |
| Table 4-27. Temperature sensor characteristics <sup>(1)</sup> .....                                      | 59 |
| Table 4-28. I2C characteristics <sup>(1)(2)(3)</sup> .....   | 60 |

|  |    |
|--|----|
| <b>Table 4-29. USART characteristics<sup>(1)</sup></b> .....                                     | 61 |
| <b>Table 4-30. TIMER characteristics<sup>(1)</sup></b> .....                                     | 61 |
| <b>Table 4-31. FWDGT min/max timeout period at 40 kHz (IRC40K)<sup>(1)</sup></b> .....           | 61 |
| <b>Table 4-32. WWDGT min-max timeout value at 48 MHz (f<sub>PCLK1</sub>)<sup>(1)</sup></b> ..... | 62 |
| <b>Table 5-1. LQFP64 package dimensions</b> .....  | 63 |
| <b>Table 5-2. LQFP48 package dimensions</b> .....  | 65 |
| <b>Table 5-3. LQFP32 package dimensions</b> .....  | 67 |
| <b>Table 5-4. QFN32 package dimensions</b> .....   | 69 |
| <b>Table 5-5. QFN28 package dimensions</b> .....   | 71 |
| <b>Table 5-6. TSSOP20 package dimensions</b> .....   | 73 |
| <b>Table 5-7. Package thermal characteristics<sup>(1)</sup></b> .....                            | 75 |
| <b>Table 6-1. Part ordering code for GD32F130xx devices</b> .....                                | 77 |
| <b>Table 7-1. Revision history</b> .....   | 78 |

## 1. General description

The GD32F130xx device belongs to the value line of GD32 MCU family. It is a 32-bit general-purpose microcontroller based on the high performance Arm® Cortex®-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F130xx device incorporates the Arm® Cortex®-M3 32-bit processor core operating at 48 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 64 KB on-chip Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, up to five general 16-bit timers, a general 32-bit timer, a PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs and two USARTs.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F130xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.





## 2. Device overview

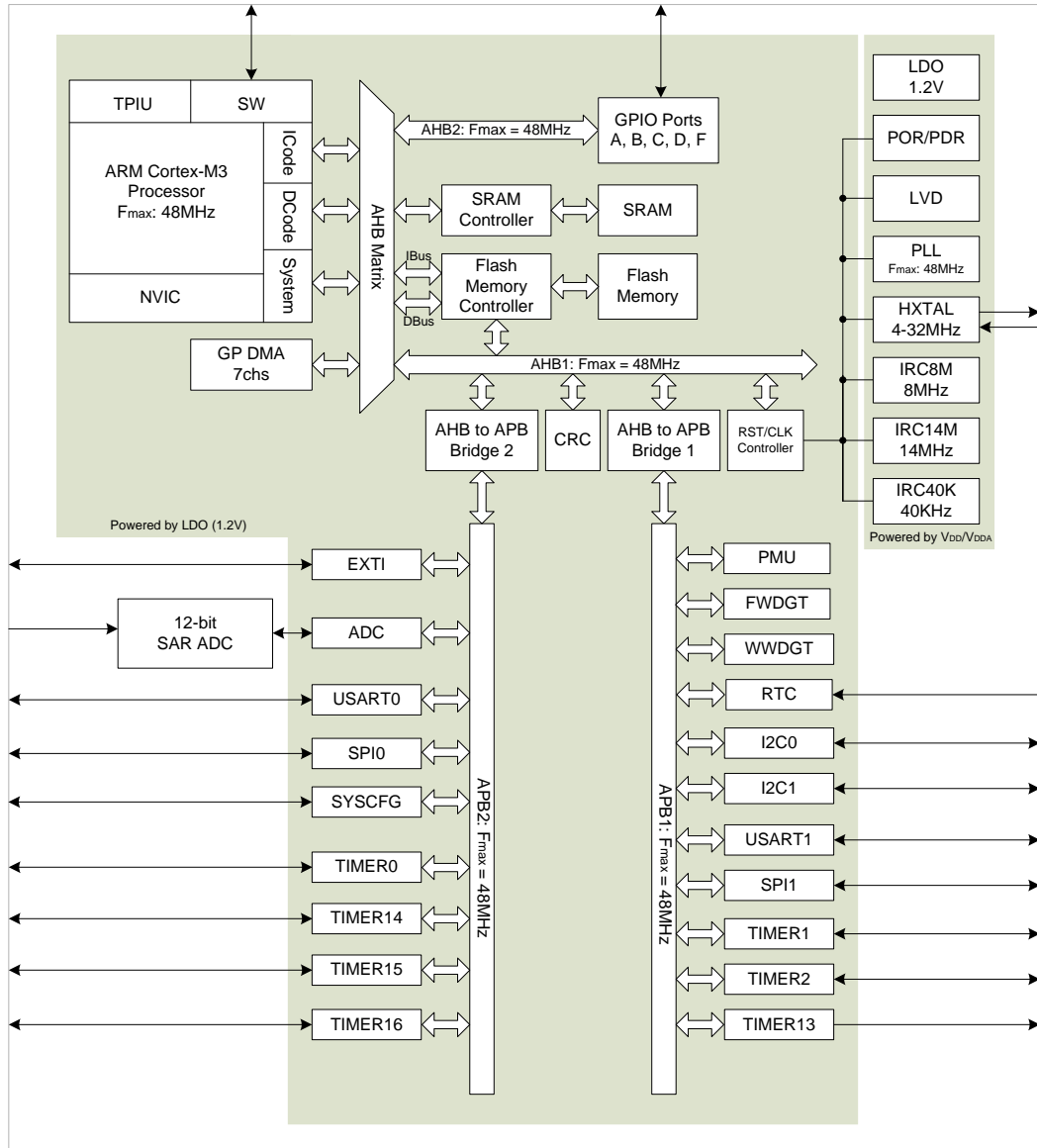
### 2.1. Device information

Table 2-1. GD32F130xx devices features and peripheral list

| Part Number  |                        | GD32F130xx                       |                                  |                                  |                                  |                                  |                               |                                  |                                  |                                  |                                  |                               |                               |                                  |                                  |                               |                               |                         |
|--------------|------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|-------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|-------------------------------|-------------------------------|----------------------------------|----------------------------------|-------------------------------|-------------------------------|-------------------------|
|              |                        | F4                               | F6                               | F8                               | G4                               | G6                               | G8                            | K4                               | K6                               | K8                               | K4                               | K6                            | K8                            | C4                               | C6                               | C8                            | R8                            |                         |
| Flash        | Code area (KB)         | 16                               | 32                               | 32                               | 16                               | 32                               | 32                            | 16                               | 32                               | 32                               | 16                               | 32                            | 32                            | 16                               | 32                               | 32                            | 32                            |                         |
|              | Data area (KB)         | 0                                | 0                                | 32                               | 0                                | 0                                | 32                            | 0                                | 0                                | 32                               | 0                                | 0                             | 32                            | 0                                | 0                                | 32                            | 32                            |                         |
|              | Total (KB)             | 16                               | 32                               | 64                               | 16                               | 32                               | 64                            | 16                               | 32                               | 64                               | 16                               | 32                            | 64                            | 16                               | 32                               | 64                            | 64                            |                         |
| SRAM (KB)    |                        | 4                                | 4                                | 8                                | 4                                | 4                                | 8                             | 4                                | 4                                | 8                                | 4                                | 4                             | 8                             | 4                                | 4                                | 8                             | 8                             |                         |
| Timers       | General timer(32-bit)  | 1<br><small>(1)</small>          | 1<br><small>(1)</small>          | 1<br><small>(1)</small>          | 1<br><small>(1)</small>          | 1<br><small>(1)</small>          | 1<br><small>(1)</small>       | 1<br><small>(1)</small>          | 1<br><small>(1)</small>          | 1<br><small>(1)</small>          | 1<br><small>(1)</small>          | 1<br><small>(1)</small>       | 1<br><small>(1)</small>       | 1<br><small>(1)</small>          | 1<br><small>(1)</small>          | 1<br><small>(1)</small>       | 1<br><small>(1)</small>       |                         |
|              | General timer(16-bit)  | 4<br><small>(2,13,15-16)</small> | 4<br><small>(2,13,15-16)</small> | 4<br><small>(2,13,15-16)</small> | 4<br><small>(2,13,15-16)</small> | 4<br><small>(2,13,15-16)</small> | 5<br><small>(2,13-16)</small> | 4<br><small>(2,13,15-16)</small> | 4<br><small>(2,13,15-16)</small> | 4<br><small>(2,13,15-16)</small> | 4<br><small>(2,13,15-16)</small> | 5<br><small>(2,13-16)</small> | 5<br><small>(2,13-16)</small> | 4<br><small>(2,13,15-16)</small> | 4<br><small>(2,13,15-16)</small> | 5<br><small>(2,13-16)</small> | 5<br><small>(2,13-16)</small> |                         |
|              | Advanced timer(16-bit) | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>       | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>       | 1<br><small>(0)</small>       | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>       | 1<br><small>(0)</small>       | 1<br><small>(0)</small> |
|              | SysTick                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                             | 1                                | 1                                | 1                                | 1                                | 1                             | 1                             | 1                                | 1                                | 1                             | 1                             | 1                       |
|              | Watchdog               | 2                                | 2                                | 2                                | 2                                | 2                                | 2                             | 2                                | 2                                | 2                                | 2                                | 2                             | 2                             | 2                                | 2                                | 2                             | 2                             | 2                       |
|              | RTC                    | 1                                | 1                                | 1                                | 1                                | 1                                | 1                             | 1                                | 1                                | 1                                | 1                                | 1                             | 1                             | 1                                | 1                                | 1                             | 1                             | 1                       |
| Connectivity | USART                  | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>        | 2<br><small>(0-1)</small>        | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>        | 2<br><small>(0-1)</small>     | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>        | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>        | 2<br><small>(0-1)</small>     | 2<br><small>(0-1)</small>     | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>        | 2<br><small>(0-1)</small>     | 2<br><small>(0-1)</small>     |                         |
|              | I2C                    | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>        | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>     | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>     | 2<br><small>(0-1)</small>     | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>     | 2<br><small>(0-1)</small>     |                         |
|              | SPI                    | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>        | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>     | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>     | 2<br><small>(0-1)</small>     | 1<br><small>(0)</small>          | 1<br><small>(0)</small>          | 2<br><small>(0-1)</small>     | 2<br><small>(0-1)</small>     |                         |
| GPIO         |                        | 15                               | 15                               | 15                               | 23                               | 23                               | 23                            | 27                               | 27                               | 27                               | 25                               | 25                            | 25                            | 39                               | 39                               | 39                            | 55                            |                         |
| EXTI         |                        | 16                               | 16                               | 16                               | 16                               | 16                               | 16                            | 16                               | 16                               | 16                               | 16                               | 16                            | 16                            | 16                               | 16                               | 16                            | 16                            |                         |
| ADC          | Units                  | 1                                | 1                                | 1                                | 1                                | 1                                | 1                             | 1                                | 1                                | 1                                | 1                                | 1                             | 1                             | 1                                | 1                                | 1                             | 1                             |                         |
|              | Channels (External)    | 9                                | 9                                | 9                                | 10                               | 10                               | 10                            | 10                               | 10                               | 10                               | 10                               | 10                            | 10                            | 10                               | 10                               | 10                            | 16                            |                         |
|              | Channels (Internal)    | 3                                | 3                                | 3                                | 3                                | 3                                | 3                             | 3                                | 3                                | 3                                | 3                                | 3                             | 3                             | 3                                | 3                                | 3                             | 3                             |                         |
| Package      |                        | TSSOP20                          |                                  |                                  | QFN28                            |                                  |                               | QFN32                            |                                  |                                  | LQFP32                           |                               |                               | LQFP48                           |                                  |                               | LQFP64                        |                         |

## 2.2. Block diagram

Figure 2-1. GD32F130xx block diagram



## 2.3. Pinouts and pin assignment

Figure 2-2. GD32F130Rx LQFP64 pinouts

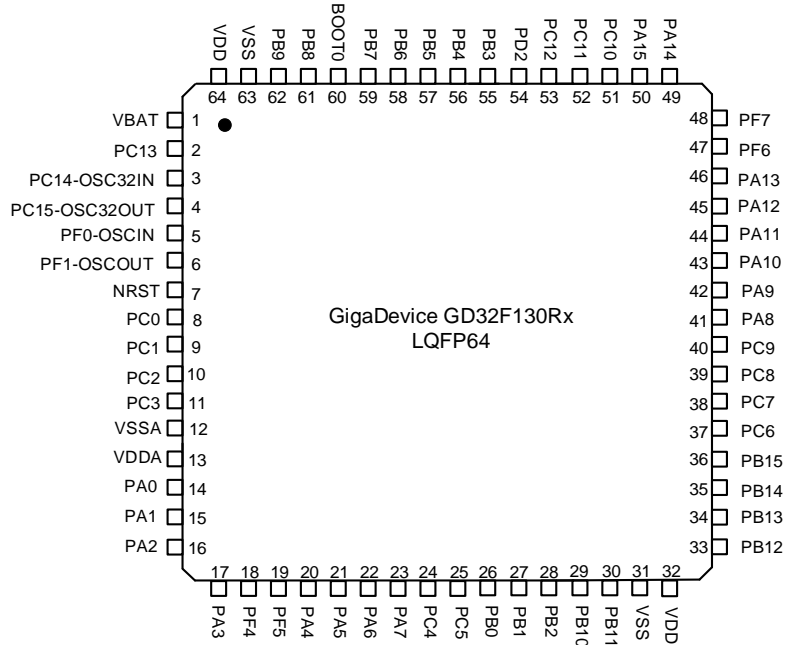


Figure 2-3. GD32F130Cx LQFP48 pinouts

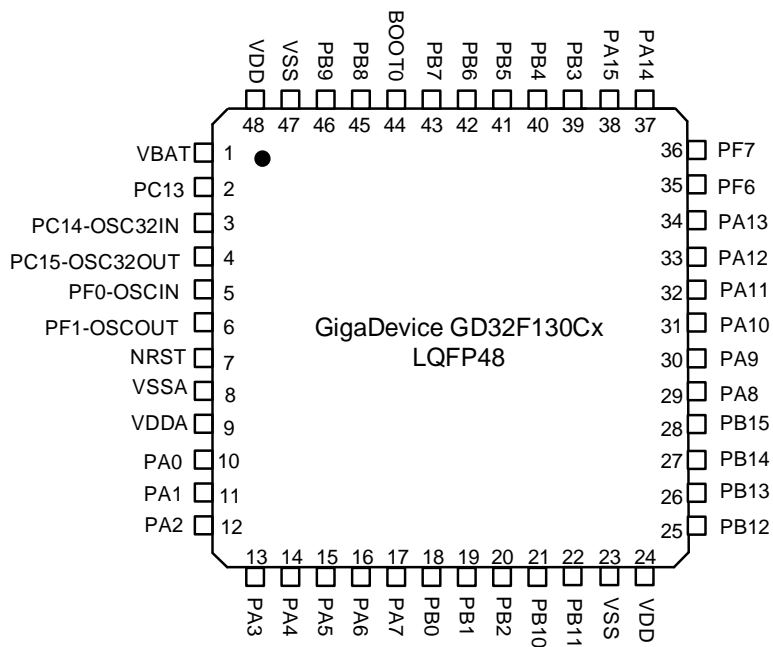


Figure 2-4. GD32F130Kx LQFP32 pinouts

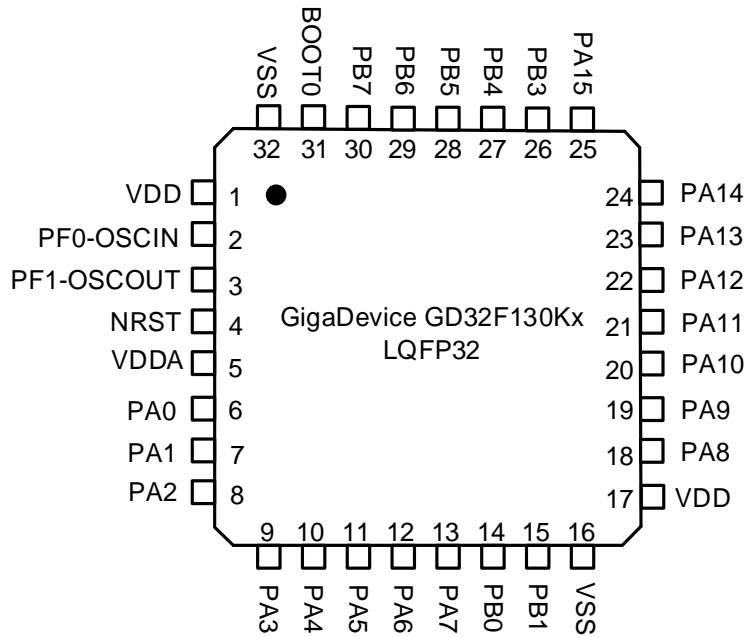


Figure 2-5. GD32F130Kx QFN32 pinouts

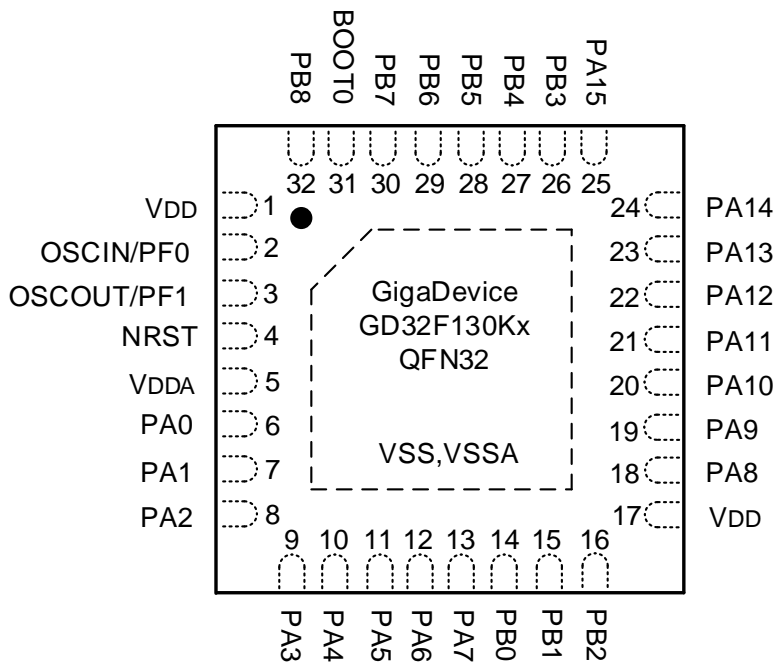


Figure 2-6. GD32F130Gx QFN28 pinouts

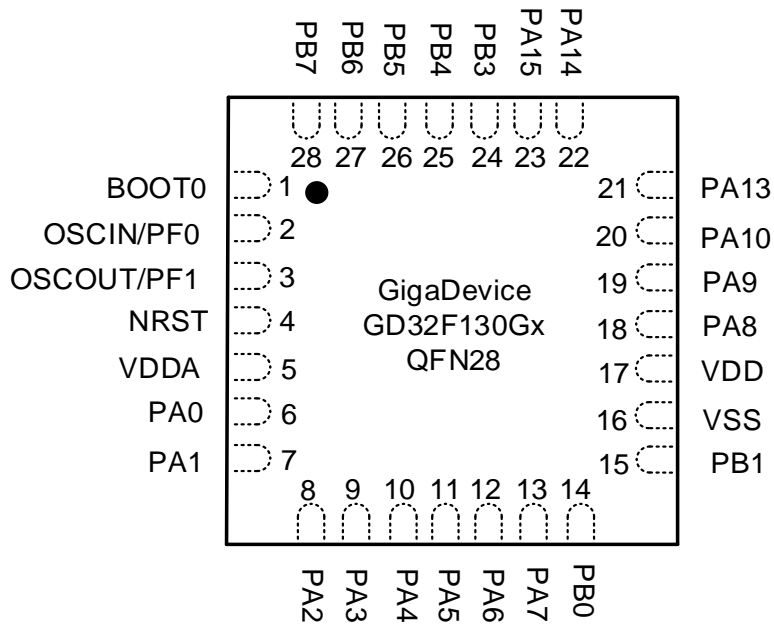
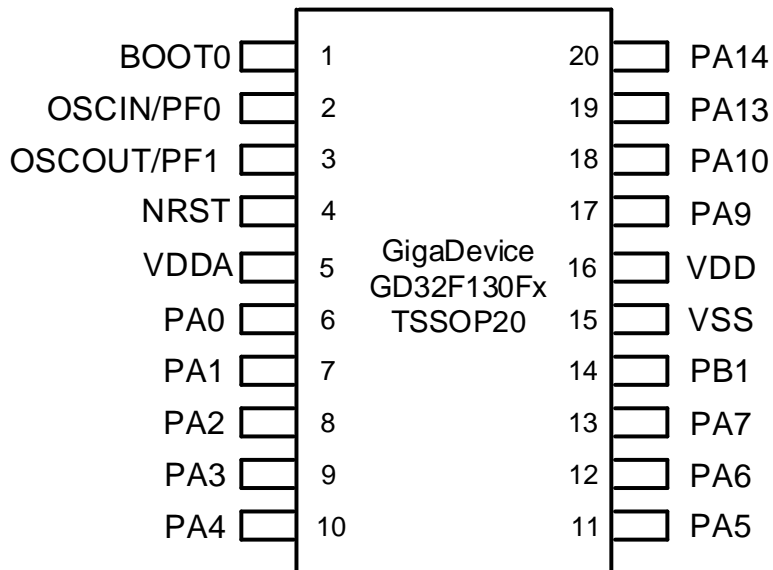


Figure 2-7. GD32F130Fx TSSOP20 pinouts



## 2.4. Memory map

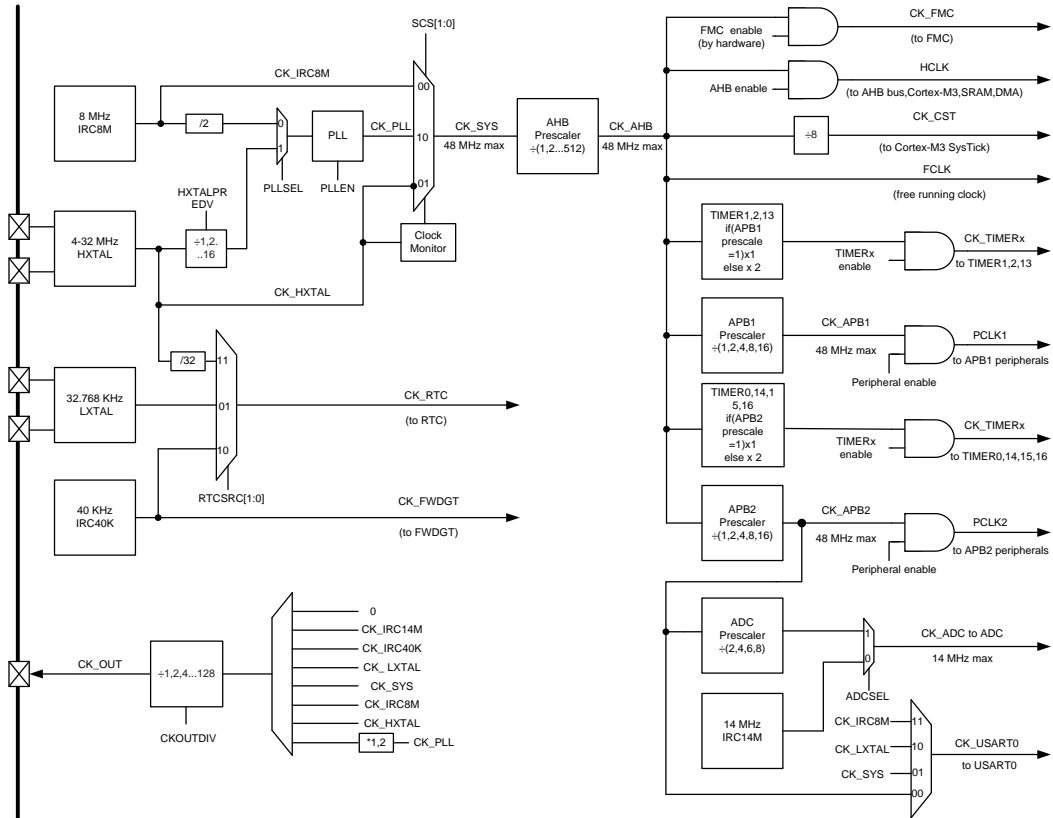
**Table 2-2. GD32F130xx memory map**

| Pre-defined Regions       | Bus  | Address                   | Peripherals                    |
|---------------------------|------|---------------------------|--------------------------------|
|                           |      | 0xE000 0000 - 0xE00F FFFF | Cortex-M3 internal peripherals |
| External Device           |      | 0xA000 0000 - 0xDFFF FFFF | Reserved                       |
| External RAM              |      | 0x6000 0000 - 0x9FFF FFFF | Reserved                       |
| Peripherals               | AHB1 | 0x5000 0000 - 0x5FFF FFFF | Reserved                       |
|                           | AHB2 | 0x4800 1800 - 0x4FFF FFFF | Reserved                       |
|                           |      | 0x4800 1400 - 0x4800 17FF | GPIOF                          |
|                           |      | 0x4800 1000 - 0x4800 13FF | Reserved                       |
|                           |      | 0x4800 0C00 - 0x4800 0FFF | GIPOD                          |
|                           |      | 0x4800 0800 - 0x4800 0BFF | GPIOC                          |
|                           |      | 0x4800 0400 - 0x4800 07FF | GPIOB                          |
|                           |      | 0x4800 0000 - 0x4800 03FF | GPIOA                          |
|                           | AHB1 | 0x4002 4400 - 0x47FF FFFF | Reserved                       |
|                           |      | 0x4002 4000 - 0x4002 43FF | Reserved                       |
|                           |      | 0x4002 3400 - 0x4002 3FFF | Reserved                       |
|                           |      | 0x4002 3000 - 0x4002 33FF | CRC                            |
|                           |      | 0x4002 2400 - 0x4002 2FFF | Reserved                       |
|                           |      | 0x4002 2000 - 0x4002 23FF | FMC                            |
|                           |      | 0x4002 1400 - 0x4002 1FFF | Reserved                       |
|                           |      | 0x4002 1000 - 0x4002 13FF | RCU                            |
|                           |      | 0x4002 0400 - 0x4002 0FFF | Reserved                       |
|                           |      | 0x4002 0000 - 0x4002 03FF | DMA                            |
|                           | APB2 | 0x4001 4C00 - 0x4001 FFFF | Reserved                       |
|                           |      | 0x4001 4800 - 0x4001 4BFF | TIMER16                        |
|                           |      | 0x4001 4400 - 0x4001 47FF | TIMER15                        |
|                           |      | 0x4001 4000 - 0x4001 43FF | TIMER14                        |
|                           |      | 0x4001 3C00 - 0x4001 3FFF | Reserved                       |
|                           |      | 0x4001 3800 - 0x4001 3BFF | USART0                         |
|                           |      | 0x4001 3400 - 0x4001 37FF | Reserved                       |
|                           |      | 0x4001 3000 - 0x4001 33FF | SPI0                           |
|                           |      | 0x4001 2C00 - 0x4001 2FFF | TIMER0                         |
|                           |      | 0x4001 2800 - 0x4001 2BFF | Reserved                       |
|                           |      | 0x4001 2400 - 0x4001 27FF | ADC                            |
|                           |      | 0x4001 0800 - 0x4001 23FF | Reserved                       |
|                           |      | 0x4001 0400 - 0x4001 07FF | EXTI                           |
|                           |      | 0x4001 0000 - 0x4001 03FF | SYSCFG                         |
|                           | APB1 | 0x4000 C400 - 0x4000 FFFF | Reserved                       |
| 0x4000 C000 - 0x4000 C3FF |      | Reserved                  |                                |

| Pre-defined Regions       | Bus    | Address                   | Peripherals                       |
|---------------------------|--------|---------------------------|-----------------------------------|
|                           |        | 0x4000 7C00 - 0x4000 BFFF | Reserved                          |
|                           |        | 0x4000 7800 - 0x4000 7BFF | Reserved                          |
|                           |        | 0x4000 7400 - 0x4000 77FF | Reserved                          |
|                           |        | 0x4000 7000 - 0x4000 73FF | PMU                               |
|                           |        | 0x4000 6400 - 0x4000 6FFF | Reserved                          |
|                           |        | 0x4000 6000 - 0x4000 63FF | Reserved                          |
|                           |        | 0x4000 5C00 - 0x4000 5FFF | Reserved                          |
|                           |        | 0x4000 5800 - 0x4000 5BFF | I2C1                              |
|                           |        | 0x4000 5400 - 0x4000 57FF | I2C0                              |
|                           |        | 0x4000 4800 - 0x4000 53FF | Reserved                          |
|                           |        | 0x4000 4400 - 0x4000 47FF | USART1                            |
|                           |        | 0x4000 4000 - 0x4000 43FF | Reserved                          |
|                           |        | 0x4000 3C00 - 0x4000 3FFF | Reserved                          |
|                           |        | 0x4000 3800 - 0x4000 3BFF | SPI1                              |
|                           |        | 0x4000 3400 - 0x4000 37FF | Reserved                          |
|                           |        | 0x4000 3000 - 0x4000 33FF | FWDGT                             |
|                           |        | 0x4000 2C00 - 0x4000 2FFF | WWDGT                             |
|                           |        | 0x4000 2800 - 0x4000 2BFF | RTC                               |
|                           |        | 0x4000 2400 - 0x4000 27FF | Reserved                          |
|                           |        | 0x4000 2000 - 0x4000 23FF | TIMER13                           |
|                           |        | 0x4000 1400 - 0x4000 1FFF | Reserved                          |
|                           |        | 0x4000 1000 - 0x4000 13FF | Reserved                          |
|                           |        | 0x4000 0800 - 0x4000 0FFF | Reserved                          |
| 0x4000 0400 - 0x4000 07FF | TIMER2 |                           |                                   |
| 0x4000 0000 - 0x4000 03FF | TIMER1 |                           |                                   |
| SRAM                      |        | 0x2000 2000 - 0x3FFF FFFF | Reserved                          |
|                           |        | 0x2000 0000 - 0x2000 1FFF | SRAM                              |
| Code                      |        | 0x1FFF F810 - 0x1FFF FFFF | Reserved                          |
|                           |        | 0x1FFF F800 - 0x1FFF F80F | Option bytes                      |
|                           |        | 0x1FFF EC00 - 0x1FFF F7FF | System memory                     |
|                           |        | 0x0801 0000 - 0x1FFF EBFF | Reserved                          |
|                           |        | 0x0800 0000 - 0x0800 FFFF | Main Flash memory                 |
|                           |        | 0x0000 0000 - 0x07FF FFFF | Aliased to Flash or system memory |

## 2.5. Clock tree

Figure 2-8. GD32F130xx clock tree



**Note:**

If the APB prescaler is 1, the timer clock frequencies are set to AHB frequency divide by 1. Otherwise, they are set to the AHB frequency divide by half of APB prescaler.

**Legend:**

- HXTAL: High speed crystal oscillator
- LXTAL: Low speed crystal oscillator
- IRC8M: Internal 8M RC oscillators
- IRC40K: Internal 40K RC oscillator
- IRC14M: Internal 14M RC oscillators



## 2.6. Pin definitions

### 2.6.1. GD32F130R8 LQFP64 pin definitions

Table 2-3. GD32F130R8 LQFP64 pin definitions

| GD32F130R8 LQFP64 |      |                         |                          |  |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
| VBAT              | 1    | P                       |                          | Default: VBAT  |
| PC13-TAMPER-RTC   | 2    | I/O                     |                          | Default: PC13<br>Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1   |
| PC14-OSC32IN      | 3    | I/O                     |                          | Default: PC14<br>Additional: OSC32IN   |
| PC15-OSC32OUT     | 4    | I/O                     |                          | Default: PC15<br>Additional: OSC32OUT  |
| PF0-OSCIN         | 5    | I/O                     | 5VT                      | Default: PF0<br>Additional: OSCIN  |
| PF1-OSCOUT        | 6    | I/O                     | 5VT                      | Default: PF1<br>Additional: OSCOUT   |
| NRST              | 7    | I/O                     |                          | Default: NRST  |
| PC0               | 8    | I/O                     |                          | Default: PC0<br>Alternate: EVENTOUT<br>Additional: ADC_IN10  |
| PC1               | 9    | I/O                     |                          | Default: PC1<br>Alternate: EVENTOUT<br>Additional: ADC_IN11  |
| PC2               | 10   | I/O                     |                          | Default: PC2<br>Alternate: EVENTOUT<br>Additional: ADC_IN12  |
| PC3               | 11   | I/O                     |                          | Default: PC3<br>Alternate: EVENTOUT<br>Additional: ADC_IN13  |
| VSSA              | 12   | P                       |                          | Default: VSSA  |
| VDDA              | 13   | P                       |                          | Default: VDDA  |
| PA0-WKUP          | 14   | I/O                     |                          | Default: PA0<br>Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, I2C1_SCL<br>Additional: ADC_IN0, RTC_TAMP1, WKUP0 |
| PA1               | 15   | I/O                     |                          | Default: PA1   |

| GD32F130R8 LQFP64 |      |                         |                          |   |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description   |
|                   |      |                         |                          | Alternate: USART1_RTS/USART1_DE, TIMER1_CH1, I2C1_SDA, EVENTOUT<br>Additional: ADC_IN1  |
| PA2               | 16   | I/O                     |                          | Default: PA2<br>Alternate: USART1_TX, TIMER1_CH2, TIMER14_CH0 ,<br>Additional: ADC_IN2  |
| PA3               | 17   | I/O                     |                          | Default: PA3<br>Alternate: USART1_RX, TIMER1_CH3, TIMER14_CH1<br>Additional: ADC_IN3  |
| PF4               | 18   | I/O                     | 5VT                      | Default: PF4<br>Alternate: SPI1_NSS, EVENTOUT   |
| PF5               | 19   | I/O                     | 5VT                      | Default: PF5<br>Alternate: EVENTOUT   |
| PA4               | 20   | I/O                     |                          | Default: PA4<br>Alternate: SPI0_NSS, USART1_CK, TIMER13_CH0,<br>SPI1_NSS<br>Additional: ADC_IN4                               |
| PA5               | 21   | I/O                     |                          | Default: PA5<br>Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI<br>Additional: ADC_IN5  |
| PA6               | 22   | I/O                     |                          | Default: PA6<br>Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN,<br>TIMER15_CH0, EVENTOUT<br>Additional: ADC_IN6               |
| PA7               | 23   | I/O                     |                          | Default: PA7<br>Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0,<br>TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT<br>Additional: ADC_IN7 |
| PC4               | 24   | I/O                     |                          | Default: PC4<br>Alternate: EVENTOUT<br>Additional: ADC_IN14   |
| PC5               | 25   | I/O                     |                          | Default: PC5<br>Additional: ADC_IN15  |
| PB0               | 26   | I/O                     |                          | Default: PB0<br>Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX,<br>EVENTOUT<br>Additional: ADC_IN8                           |
| PB1               | 27   | I/O                     |                          | Default: PB1<br>Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON,<br>SPI1_SCK<br>Additional: ADC_IN9                         |
| PB2               | 28   | I/O                     | 5VT                      | Default: PB2  |

| GD32F130R8 LQFP64 |      |                         |                          |  |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
| PB10              | 29   | I/O                     | 5VT                      | Default: PB10<br>Alternate: I2C1_SCL, TIMER1_CH2   |
| PB11              | 30   | I/O                     | 5VT                      | Default: PB11<br>Alternate: I2C1_SDA, TIMER1_CH3, EVENTOUT   |
| VSS               | 31   | P                       |                          | Default: VSS   |
| VDD               | 32   | P                       |                          | Default: VDD   |
| PB12              | 33   | I/O                     | 5VT                      | Default: PB12<br>Alternate: SPI1_NSS, TIMER0_BRKIN, I2C1_SMBA, EVENTOUT                                    |
| PB13              | 34   | I/O                     | 5VT                      | Default: PB13<br>Alternate: SPI1_SCK, TIMER0_CH0_ON  |
| PB14              | 35   | I/O                     | 5VT                      | Default: PB14<br>Alternate: SPI1_MISO, TIMER0_CH1_ON, TIMER14_CH0  |
| PB15              | 36   | I/O                     | 5VT                      | Default: PB15<br>Alternate: SPI1_MOSI, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1<br>Additional: RTC_REFIN |
| PC6               | 37   | I/O                     | 5VT                      | Default: PC6<br>Alternate: TIMER2_CH0  |
| PC7               | 38   | I/O                     | 5VT                      | Default: PC7<br>Alternate: TIMER2_CH1  |
| PC8               | 39   | I/O                     | 5VT                      | Default: PC8<br>Alternate: TIMER2_CH2  |
| PC9               | 40   | I/O                     | 5VT                      | Default: PC9<br>Alternate: TIMER2_CH3  |
| PA8               | 41   | I/O                     | 5VT                      | Default: PA8<br>Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX, EVENTOUT                              |
| PA9               | 42   | I/O                     | 5VT                      | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL                                  |
| PA10              | 43   | I/O                     | 5VT                      | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA                                 |
| PA11              | 44   | I/O                     | 5VT                      | Default: PA11<br>Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT   |
| PA12              | 45   | I/O                     | 5VT                      | Default: PA12<br>Alternate: USART0_RTS/USART0_DE, TIMER0_ETI, EVENTOUT                                     |
| PA13              | 46   | I/O                     | 5VT                      | Default: PA13<br>Alternate: IFRP_OUT, SWDIO, SPI1_MISO   |

| GD32F130R8 LQFP64 |      |                         |                          |  |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
| PF6               | 47   | I/O                     | 5VT                      | Default: PF6<br>Alternate: I2C1_SCL  |
| PF7               | 48   | I/O                     | 5VT                      | Default: PF7<br>Alternate: I2C1_SDA  |
| PA14              | 49   | I/O                     | 5VT                      | Default: PA14<br>Alternate: USART1_TX, SWCLK, SPI1_MOSI  |
| PA15              | 50   | I/O                     | 5VT                      | Default: PA15<br>Alternate: SPI0_NSS, USART1_RX, TIMER1_CH0,<br>TIMER1_ETI, SPI1_NSS, EVENTOUT |
| PC10              | 51   | I/O                     | 5VT                      | Default: PC10  |
| PC11              | 52   | I/O                     | 5VT                      | Default: PC11  |
| PC12              | 53   | I/O                     | 5VT                      | Default: PC12  |
| PD2               | 54   | I/O                     | 5VT                      | Default: PD2<br>Alternate: TIMER2_ETI  |
| PB3               | 55   | I/O                     | 5VT                      | Default: PB3<br>Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT                                      |
| PB4               | 56   | I/O                     | 5VT                      | Default: PB4<br>Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT                                     |
| PB5               | 57   | I/O                     | 5VT                      | Default: PB5<br>Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN,<br>TIMER2_CH1                  |
| PB6               | 58   | I/O                     | 5VT                      | Default: PB6<br>Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON                                 |
| PB7               | 59   | I/O                     | 5VT                      | Default: PB7<br>Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON                                 |
| BOOT0             | 60   | I                       |                          | Default: BOOT0   |
| PB8               | 61   | I/O                     | 5VT                      | Default: PB8<br>Alternate: I2C0_SCL, TIMER15_CH0   |
| PB9               | 62   | I/O                     | 5VT                      | Default: PB9<br>Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0,<br>EVENTOUT                        |
| VSS               | 63   | P                       |                          | Default: VSS   |
| VDD               | 64   | P                       |                          | Default: VDD   |

**Notes:**

- (1) Type: I = input, O = output, P = power.  
(2) I/O Level: 5VT = 5 V tolerant.

## 2.6.2. GD32F130Cx LQFP48 pin definitions

**Table 2-4. GD32F130Cx LQFP48 pin definitions**

| GD32F130Cx LQFP48 |      |                         |                          |  |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
| VBAT              | 1    | P                       |                          | Default: VBAT  |
| PC13-TAMPER-RTC   | 2    | I/O                     |                          | Default: PC13<br>Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1   |
| PC14-OSC32IN      | 3    | I/O                     |                          | Default: PC14<br>Additional: OSC32IN   |
| PC15-OSC32OUT     | 4    | I/O                     |                          | Default: PC15<br>Additional: OSC32OUT  |
| PF0-OSCIN         | 5    | I/O                     | 5VT                      | Default: PF0<br>Additional: OSCIN  |
| PF1-OSCOU         | 6    | I/O                     | 5VT                      | Default: PF1<br>Additional: OSCOUT   |
| NRST              | 7    | I/O                     |                          | Default: NRST  |
| VSSA              | 8    | P                       |                          | Default: VSSA  |
| VDDA              | 9    | P                       |                          | Default: VDDA  |
| PA0-WKUP          | 10   | I/O                     |                          | Default: PA0<br>Alternate: USART0_CTS <sup>(3)</sup> , USART1_CTS <sup>(4)</sup> , TIMER1_CH0, TIMER1_ETI, I2C1_SCL <sup>(5)</sup><br>Additional: ADC_IN0, RTC_TAMP1, WKUP0                                  |
| PA1               | 11   | I/O                     |                          | Default: PA1<br>Alternate: USART0_RTS <sup>(3)</sup> /USART0_DE <sup>(3)</sup> , USART1_RTS <sup>(4)</sup> /USART1_DE <sup>(4)</sup> , TIMER1_CH1, I2C1_SDA <sup>(5)</sup> , EVENTOUT<br>Additional: ADC_IN1 |
| PA2               | 12   | I/O                     |                          | Default: PA2<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , TIMER1_CH2, TIMER14_CH0<br>Additional: ADC_IN2  |
| PA3               | 13   | I/O                     |                          | Default: PA3<br>Alternate: USART0_RX <sup>(3)</sup> , USART1_RX <sup>(4)</sup> , TIMER1_CH3, TIMER14_CH1<br>Additional: ADC_IN3  |
| PA4               | 14   | I/O                     |                          | Default: PA4<br>Alternate: SPI0_NSS, USART0_CK <sup>(3)</sup> , USART1_CK <sup>(4)</sup> , TIMER13_CH0, SPI1_NSS <sup>(5)</sup><br>Additional: ADC_IN4   |

| GD32F130Cx LQFP48 |      |                         |                          |   |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description   |
| PA5               | 15   | I/O                     |                          | Default: PA5<br>Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI<br>Additional: ADC_IN5  |
| PA6               | 16   | I/O                     |                          | Default: PA6<br>Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT<br>Additional: ADC_IN6  |
| PA7               | 17   | I/O                     |                          | Default: PA7<br>Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT<br>Additional: ADC_IN7                            |
| PB0               | 18   | I/O                     |                          | Default: PB0<br>Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX <sup>(4)</sup> , EVENTOUT<br>Additional: ADC_IN8                                      |
| PB1               | 19   | I/O                     |                          | Default: PB1<br>Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK <sup>(5)</sup><br>Additional: ADC_IN9                                     |
| PB2               | 20   | I/O                     | 5VT                      | Default: PB2  |
| PB10              | 21   | I/O                     | 5VT                      | Default: PB10<br>Alternate: I2C1_SCL <sup>(5)</sup> , TIMER1_CH2  |
| PB11              | 22   | I/O                     | 5VT                      | Default: PB11<br>Alternate: I2C1_SDA <sup>(5)</sup> , TIMER1_CH3, EVENTOUT  |
| VSS               | 23   | P                       |                          | Default: VSS  |
| VDD               | 24   | P                       |                          | Default: VDD  |
| PB12              | 25   | I/O                     | 5VT                      | Default: PB12<br>Alternate: SPI0_NSS <sup>(3)</sup> , SPI1_NSS <sup>(5)</sup> , TIMER0_BRKIN, I2C1_SMBA <sup>(5)</sup> , EVENTOUT                     |
| PB13              | 26   | I/O                     | 5VT                      | Default: PB13<br>Alternate: SPI0_SCK <sup>(3)</sup> , SPI1_SCK <sup>(5)</sup> , TIMER0_CH0_ON   |
| PB14              | 27   | I/O                     | 5VT                      | Default: PB14<br>Alternate: SPI0_MISO <sup>(3)</sup> , SPI1_MISO <sup>(5)</sup> , TIMER0_CH1_ON, TIMER14_CH0  |
| PB15              | 28   | I/O                     | 5VT                      | Default: PB15<br>Alternate: SPI0_MOSI <sup>(3)</sup> , SPI1_MOSI <sup>(5)</sup> , TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1<br>Additional: RTC_REFIN |
| PA8               | 29   | I/O                     | 5VT                      | Default: PA8<br>Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX <sup>(4)</sup> , EVENTOUT   |

| GD32F130Cx LQFP48 |      |                         |                          |  |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
| PA9               | 30   | I/O                     | 5VT                      | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL  |
| PA10              | 31   | I/O                     | 5VT                      | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA   |
| PA11              | 32   | I/O                     | 5VT                      | Default: PA11<br>Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT   |
| PA12              | 33   | I/O                     | 5VT                      | Default: PA12<br>Alternate: USART0_RTS/USART0_DE, TIMER0_ETI, EVENTOUT   |
| PA13              | 34   | I/O                     | 5VT                      | Default: PA13<br>Alternate: IFRP_OUT, SWDIO, SPI1_MISO <sup>(5)</sup>  |
| PF6               | 35   | I/O                     | 5VT                      | Default: PF6<br>Alternate: I2C1_SCL <sup>(5)</sup> , I2C0_SCL <sup>(6)</sup>   |
| PF7               | 36   | I/O                     | 5VT                      | Default: PF7<br>Alternate: I2C1_SDA <sup>(5)</sup> , I2C0_SCL <sup>(6)</sup>   |
| PA14              | 37   | I/O                     | 5VT                      | Default: PA14<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , SWCLK, SPI1_MOSI <sup>(5)</sup>                                      |
| PA15              | 38   | I/O                     | 5VT                      | Default: PA15<br>Alternate: SPI0_NSS, USART0_RX <sup>(3)</sup> , USART1_RX <sup>(4)</sup> , TIMER1_CH0, TIMER1_ETI, SPI1_NSS <sup>(5)</sup> , EVENTOUT |
| PB3               | 39   | I/O                     | 5VT                      | Default: PB3<br>Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT  |
| PB4               | 40   | I/O                     | 5VT                      | Default: PB4<br>Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT   |
| PB5               | 41   | I/O                     | 5VT                      | Default: PB5<br>Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1   |
| PB6               | 42   | I/O                     | 5VT                      | Default: PB6<br>Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON   |
| PB7               | 43   | I/O                     | 5VT                      | Default: PB7<br>Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON   |
| BOOT0             | 44   | I                       |                          | Default: BOOT0   |
| PB8               | 45   | I/O                     | 5VT                      | Default: PB8<br>Alternate: I2C0_SCL, TIMER15_CH0,  |
| PB9               | 46   | I/O                     | 5VT                      | Default: PB9<br>Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT   |
| VSS               | 47   | P                       |                          | Default: VSS   |

| GD32F130Cx LQFP48 |      |                         |                          |                       |
|-------------------|------|-------------------------|--------------------------|-----------------------|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description |
| VDD               | 48   | P                       |                          | Default: VDD          |

**Notes:**

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32F130C4 devices only.
- (4) Functions are available on GD32F130C8/6 devices.
- (5) Functions are available on GD32F130C8 devices.
- (6) Functions are available on GD32F130C4/6 devices.

### 2.6.3. GD32F130Kx LQFP32 pin definitions

**Table 2-5. GD32F130Kx LQFP32 pin definitions**

| GD32F130Kx LQFP32 |      |                         |                          |  |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
| VDD               | 1    | P                       |                          | Default: VDD   |
| PF0-OSCIN         | 2    | I/O                     | 5VT                      | Default: PF0<br>Additional: OSCIN  |
| PF1-OSCOUT        | 3    | I/O                     | 5VT                      | Default: PF1<br>Additional: OSCOUT   |
| NRST              | 4    | I/O                     |                          | Default: NRST  |
| VDDA              | 5    | P                       |                          | Default: VDDA  |
| PA0-WKUP          | 6    | I/O                     |                          | Default: PA0<br>Alternate: USART0_CTS <sup>(3)</sup> , USART1_CTS <sup>(4)</sup> , TIMER1_CH0, TIMER1_ETI, I2C1_SCL <sup>(5)</sup><br>Additional: ADC_IN0, RTC_TAMP1, WKUP0                                  |
| PA1               | 7    | I/O                     |                          | Default: PA1<br>Alternate: USART0_RTS <sup>(3)</sup> /USART0_DE <sup>(3)</sup> , USART1_RTS <sup>(4)</sup> /USART1_DE <sup>(4)</sup> , TIMER1_CH1, I2C1_SDA <sup>(5)</sup> , EVENTOUT<br>Additional: ADC_IN1 |
| PA2               | 8    | I/O                     |                          | Default: PA2<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , TIMER1_CH2, TIMER14_CH0<br>Additional: ADC_IN2  |
| PA3               | 9    | I/O                     |                          | Default: PA3   |



| GD32F130Kx LQFP32 |      |                         |                          |  |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
|                   |      |                         |                          | Alternate: USART0_RX <sup>(3)</sup> , USART1_RX <sup>(4)</sup> , TIMER1_CH3, TIMER14_CH1<br>Additional: ADC_IN3  |
| PA4               | 10   | I/O                     |                          | Default: PA4<br>Alternate: SPI0_NSS, USART0_CK <sup>(3)</sup> , USART1_CK <sup>(4)</sup> , TIMER13_CH0, SPI1_NSS <sup>(5)</sup><br>Additional: ADC_IN4 |
| PA5               | 11   | I/O                     |                          | Default: PA5<br>Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI<br>Additional: ADC_IN5   |
| PA6               | 12   | I/O                     |                          | Default: PA6<br>Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT<br>Additional: ADC_IN6   |
| PA7               | 13   | I/O                     |                          | Default: PA7<br>Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT<br>Additional: ADC_IN7                             |
| PB0               | 14   | I/O                     |                          | Default: PB0<br>Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX <sup>(4)</sup> , EVENTOUT<br>Additional: ADC_IN8                                       |
| PB1               | 15   | I/O                     |                          | Default: PB1<br>Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK <sup>(5)</sup><br>Additional: ADC_IN9                                      |
| VSS               | 16   | P                       | 5VT                      | Default: VSS   |
| VDD               | 17   | P                       |                          | Default: VDD   |
| PA8               | 18   | I/O                     | 5VT                      | Default: PA8<br>Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX <sup>(4)</sup> , EVENTOUT  |
| PA9               | 19   | I/O                     | 5VT                      | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL  |
| PA10              | 20   | I/O                     | 5VT                      | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA   |
| PA11              | 21   | I/O                     | 5VT                      | Default: PA11<br>Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT   |
| PA12              | 22   | I/O                     | 5VT                      | Default: PA12<br>Alternate: USART0_RTS/USART0_DE, TIMER0_ETI,  |

| GD32F130Kx LQFP32 |      |                         |                          |  |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
|                   |      |                         |                          | EVENTOUT   |
| PA13              | 23   | I/O                     | 5VT                      | Default: PA13<br>Alternate: IFRP_OUT, SWDIO, SPI1_MISO <sup>(5)</sup>  |
| PA14              | 24   | I/O                     | 5VT                      | Default: PA14<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , SWCLK, SPI1_MOSI <sup>(5)</sup>                                      |
| PA15              | 25   | I/O                     | 5VT                      | Default: PA15<br>Alternate: SPI0_NSS, USART0_RX <sup>(3)</sup> , USART1_RX <sup>(4)</sup> , TIMER1_CH0, TIMER1_ETI, SPI1_NSS <sup>(5)</sup> , EVENTOUT |
| PB3               | 26   | I/O                     | 5VT                      | Default: PB3<br>Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT  |
| PB4               | 27   | I/O                     | 5VT                      | Default: PB4<br>Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT   |
| PB5               | 28   | I/O                     | 5VT                      | Default: PB5<br>Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1   |
| PB6               | 29   | I/O                     | 5VT                      | Default: PB6<br>Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON   |
| PB7               | 30   | I/O                     | 5VT                      | Default: PB7<br>Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON   |
| BOOT0             | 31   | I                       |                          | Default: BOOT0   |
| VSS               | 32   | P                       |                          | Default: VSS   |

**Notes:**

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32F130K4 devices only.
- (4) Functions are available on GD32F130K8/6 devices.
- (5) Functions are available on GD32F130K8 devices.

#### 2.6.4. GD32F130Kx QFN32 pin definitions

**Table 2-6. GD32F130Kx QFN32 pin definitions**

| GD32F130Kx QFN32 |      |                         |                          |                       |
|------------------|------|-------------------------|--------------------------|-----------------------|
| Pin Name         | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description |
| VDD              | 1    | P                       |                          | Default: VDD          |

| GD32F130Kx QFN32 |      |                         |                          |  |
|------------------|------|-------------------------|--------------------------|--|
| Pin Name         | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
| PF0-OSCIN        | 2    | I/O                     | 5VT                      | Default: PF0<br>Additional: OSCIN  |
| PF1-OSCOOUT      | 3    | I/O                     | 5VT                      | Default: PF1<br>Additional: OSCOUT   |
| NRST             | 4    | I/O                     |                          | Default: NRST  |
| VDDA             | 5    | P                       |                          | Default: VDDA  |
| PA0-WKUP         | 6    | I/O                     |                          | Default: PA0<br>Alternate: USART0_CTS <sup>(3)</sup> , USART1_CTS <sup>(4)</sup> , TIMER1_CH0, TIMER1_ETI, I2C1_SCL <sup>(5)</sup><br>Additional: ADC_IN0, RTC_TAMP1, WKUP0                                  |
| PA1              | 7    | I/O                     |                          | Default: PA1<br>Alternate: USART0_RTS <sup>(3)</sup> /USART0_DE <sup>(3)</sup> , USART1_RTS <sup>(4)</sup> /USART1_DE <sup>(4)</sup> , TIMER1_CH1, I2C1_SDA <sup>(5)</sup> , EVENTOUT<br>Additional: ADC_IN1 |
| PA2              | 8    | I/O                     |                          | Default: PA2<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , TIMER1_CH2, TIMER14_CH0<br>Additional: ADC_IN2  |
| PA3              | 9    | I/O                     |                          | Default: PA3<br>Alternate: USART0_RX <sup>(3)</sup> , USART1_RX <sup>(4)</sup> , TIMER1_CH3, TIMER14_CH1<br>Additional: ADC_IN3  |
| PA4              | 10   | I/O                     |                          | Default: PA4<br>Alternate: SPI0_NSS, USART0_CK <sup>(3)</sup> , USART1_CK <sup>(4)</sup> , TIMER13_CH0, SPI1_NSS <sup>(5)</sup><br>Additional: ADC_IN4   |
| PA5              | 11   | I/O                     |                          | Default: PA5<br>Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI<br>Additional: ADC_IN5   |
| PA6              | 12   | I/O                     |                          | Default: PA6<br>Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT<br>Additional: ADC_IN6   |
| PA7              | 13   | I/O                     |                          | Default: PA7<br>Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT<br>Additional: ADC_IN7   |
| PB0              | 14   | I/O                     |                          | Default: PB0<br>Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX <sup>(4)</sup> , EVENTOUT  |

| GD32F130Kx QFN32 |      |                         |                          |  |
|------------------|------|-------------------------|--------------------------|--|
| Pin Name         | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
|                  |      |                         |                          | Additional: ADC_IN8  |
| PB1              | 15   | I/O                     |                          | Default: PB1<br>Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK <sup>(5)</sup><br>Additional: ADC_IN9                                      |
| PB2              | 16   | I/O                     | 5VT                      | Default: PB2   |
| VDD              | 17   | P                       |                          | Default: VDD   |
| PA8              | 18   | I/O                     | 5VT                      | Default: PA8<br>Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX <sup>(4)</sup> , EVENTOUT  |
| PA9              | 19   | I/O                     | 5VT                      | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL  |
| PA10             | 20   | I/O                     | 5VT                      | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA   |
| PA11             | 21   | I/O                     | 5VT                      | Default: PA11<br>Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT   |
| PA12             | 22   | I/O                     | 5VT                      | Default: PA12<br>Alternate: USART0_RTS/USART0_DE, TIMER0_ETI, EVENTOUT   |
| PA13             | 23   | I/O                     | 5VT                      | Default: PA13<br>Alternate: IFRP_OUT, SWDIO, SPI1_MISO <sup>(5)</sup>  |
| PA14             | 24   | I/O                     | 5VT                      | Default: PA14<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , SWCLK, SPI1_MOSI <sup>(5)</sup>                                      |
| PA15             | 25   | I/O                     | 5VT                      | Default: PA15<br>Alternate: SPI0_NSS, USART0_RX <sup>(3)</sup> , USART1_RX <sup>(4)</sup> , TIMER1_CH0, TIMER1_ETI, SPI1_NSS <sup>(5)</sup> , EVENTOUT |
| PB3              | 26   | I/O                     | 5VT                      | Default: PB3<br>Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT  |
| PB4              | 27   | I/O                     | 5VT                      | Default: PB4<br>Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT   |
| PB5              | 28   | I/O                     | 5VT                      | Default: PB5<br>Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1   |
| PB6              | 29   | I/O                     | 5VT                      | Default: PB6<br>Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON   |
| PB7              | 30   | I/O                     | 5VT                      | Default: PB7<br>Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON   |
| BOOT0            | 31   | I                       |                          | Default: BOOT0   |

| GD32F130Kx QFN32 |      |                         |                          |  |
|------------------|------|-------------------------|--------------------------|--|
| Pin Name         | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description                            |
| PB8              | 32   | I/O                     | 5VT                      | Default: PB8<br>Alternate: I2C0_SCL, TIMER15_CH0 |

**Notes:**

- (6) Type: I = input, O = output, P = power.
- (7) I/O Level: 5VT = 5 V tolerant.
- (8) Functions are available on GD32F130K4 devices only.
- (9) Functions are available on GD32F130K8/6 devices.
- (10) Functions are available on GD32F130K8 devices.

## 2.6.5. GD32F130Gx QFN28 pin definitions

Table 2-7. GD32F130Gx QFN28 pin definitions

| GD32F130Gx QFN28 |      |                         |                          |  |
|------------------|------|-------------------------|--------------------------|--|
| Pin Name         | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
| BOOT0            | 1    | I                       |                          | Default: BOOT0   |
| PF0-OSCIN        | 2    | I/O                     | 5VT                      | Default: PF0<br>Additional: OSCIN  |
| PF1-OSCOUT       | 3    | I/O                     | 5VT                      | Default: PF1<br>Additional: OSCOUT   |
| NRST             | 4    | I/O                     |                          | Default: NRST  |
| VDDA             | 5    | P                       |                          | Default: VDDA  |
| PA0-WKUP         | 6    | I/O                     |                          | Default: PA0<br>Alternate: USART0_CTS <sup>(3)</sup> , USART1_CTS <sup>(4)</sup> , TIMER1_CH0, TIMER1_ETI, I2C1_SCL <sup>(5)</sup><br>Additional: ADC_IN0, RTC_TAMP1, WKUP0                                  |
| PA1              | 7    | I/O                     |                          | Default: PA1<br>Alternate: USART0_RTS <sup>(3)</sup> /USART0_DE <sup>(3)</sup> , USART1_RTS <sup>(4)</sup> /USART1_DE <sup>(4)</sup> , TIMER1_CH1, I2C1_SDA <sup>(5)</sup> , EVENTOUT<br>Additional: ADC_IN1 |
| PA2              | 8    | I/O                     |                          | Default: PA2<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , TIMER1_CH2, TIMER14_CH0<br>Additional: ADC_IN2  |
| PA3              | 9    | I/O                     |                          | Default: PA3<br>Alternate: USART0_RX <sup>(3)</sup> , USART1_RX <sup>(4)</sup> , TIMER1_CH3, TIMER14_CH1<br>Additional: ADC_IN3  |
| PA4              | 10   | I/O                     |                          | Default: PA4<br>Alternate: SPI0_NSS, USART0_CK <sup>(3)</sup> , USART1_CK <sup>(4)</sup> , TIMER13_CH0, SPI1_NSS <sup>(5)</sup><br>Additional: ADC_IN4   |
| PA5              | 11   | I/O                     |                          | Default: PA5<br>Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI<br>Additional: ADC_IN5   |
| PA6              | 12   | I/O                     |                          | Default: PA6<br>Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT<br>Additional: ADC_IN6   |
| PA7              | 13   | I/O                     |                          | Default: PA7<br>Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT  |

| GD32F130Gx QFN28 |      |                         |                          |  |
|------------------|------|-------------------------|--------------------------|--|
| Pin Name         | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
|                  |      |                         |                          | Additional: ADC_IN7  |
| PB0              | 14   | I/O                     |                          | Default: PB0<br>Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX <sup>(4)</sup> , EVENTOUT<br>Additional: ADC_IN8                                       |
| PB1              | 15   | I/O                     |                          | Default: PB1<br>Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK <sup>(5)</sup><br>Additional: ADC_IN9                                      |
| VSS              | 16   | P                       |                          | Default: VSS   |
| VDD              | 17   | P                       |                          | Default: VDD   |
| PA8              | 18   | I/O                     | 5VT                      | Default: PA8<br>Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX <sup>(4)</sup> , EVENTOUT  |
| PA9              | 19   | I/O                     | 5VT                      | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL  |
| PA10             | 20   | I/O                     | 5VT                      | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA   |
| PA13             | 21   | I/O                     | 5VT                      | Default: PA13<br>Alternate: IFRP_OUT, SWDIO, SPI1_MISO <sup>(5)</sup>  |
| PA14             | 22   | I/O                     | 5VT                      | Default: PA14<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , SWCLK, SPI1_MOSI <sup>(5)</sup>                                      |
| PA15             | 23   | I/O                     | 5VT                      | Default: PA15<br>Alternate: SPI0_NSS, USART0_RX <sup>(3)</sup> , USART1_RX <sup>(4)</sup> , TIMER1_CH0, TIMER1_ETI, SPI1_NSS <sup>(5)</sup> , EVENTOUT |
| PB3              | 24   | I/O                     | 5VT                      | Default: PB3<br>Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT  |
| PB4              | 25   | I/O                     | 5VT                      | Default: PB4<br>Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT   |
| PB5              | 26   | I/O                     | 5VT                      | Default: PB5<br>Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1   |
| PB6              | 27   | I/O                     | 5VT                      | Default: PB6<br>Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON   |
| PB7              | 28   | I/O                     | 5VT                      | Default: PB7<br>Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON   |

**Notes:**

(1) Type: I = input, O = output, P = power.

- (2) I/O Level: 5VT = 5 V tolerant.  
(3) Functions are available on GD32F130G4 devices only.  
(4) Functions are available on GD32F130G8/6 devices.  
(5) Functions are available on GD32F130G8 devices.

## 2.6.6. GD32F130Fx TSSOP20 pin definitions

Table 2-8. GD32F130Fx TSSOP20 pin definitions

| GD32F130Fx TSSOP20 |      |                         |                          |  |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name           | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
| BOOT0              | 1    | I                       |                          | Default: BOOT0   |
| PF0-OSCIN          | 2    | I/O                     | 5VT                      | Default: PF0<br>Additional: OSCIN  |
| PF1-OSCOUT         | 3    | I/O                     | 5VT                      | Default: PF1<br>Additional: OSCOUT   |
| NRST               | 4    | I/O                     |                          | Default: NRST  |
| VDDA               | 5    | P                       |                          | Default: VDDA  |
| PA0-WKUP           | 6    | I/O                     |                          | Default: PA0<br>Alternate: USART0_CTS <sup>(3)</sup> , USART1_CTS <sup>(4)</sup> , TIMER1_CH0, TIMER1_ETI, I2C1_SCL <sup>(5)</sup><br>Additional: ADC_IN0, RTC_TAMP1, WKUP0                                  |
| PA1                | 7    | I/O                     |                          | Default: PA1<br>Alternate: USART0_RTS <sup>(3)</sup> /USART0_DE <sup>(3)</sup> , USART1_RTS <sup>(4)</sup> /USART1_DE <sup>(4)</sup> , TIMER1_CH1, I2C1_SDA <sup>(5)</sup> , EVENTOUT<br>Additional: ADC_IN1 |
| PA2                | 8    | I/O                     |                          | Default: PA2<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , TIMER1_CH2, TIMER14_CH0<br>Additional: ADC_IN2  |
| PA3                | 9    | I/O                     |                          | Default: PA3<br>Alternate: USART0_RX <sup>(3)</sup> , USART1_RX <sup>(4)</sup> , TIMER1_CH3, TIMER14_CH1<br>Additional: ADC_IN3  |
| PA4                | 10   | I/O                     |                          | Default: PA4<br>Alternate: SPI0_NSS, USART0_CK <sup>(3)</sup> , USART1_CK <sup>(4)</sup> , TIMER13_CH0, SPI1_NSS <sup>(5)</sup><br>Additional: ADC_IN4   |
| PA5                | 11   | I/O                     |                          | Default: PA5<br>Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI<br>Additional: ADC_IN5   |
| PA6                | 12   | I/O                     |                          | Default: PA6   |



| GD32F130Fx TSSOP20 |      |                         |                          |  |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name           | Pins | Pin Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Functions description  |
|                    |      |                         |                          | Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT<br>Additional: ADC_IN6                               |
| PA7                | 13   | I/O                     |                          | Default: PA7<br>Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT<br>Additional: ADC_IN7 |
| PB1                | 14   | I/O                     |                          | Default: PB1<br>Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK <sup>(5)</sup><br>Additional: ADC_IN9          |
| VSS                | 15   | P                       |                          | Default: VSS   |
| VDD                | 16   | P                       |                          | Default: VDD   |
| PA9                | 17   | I/O                     | 5VT                      | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL  |
| PA10               | 18   | I/O                     | 5VT                      | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA   |
| PA13               | 19   | I/O                     | 5VT                      | Default: PA13<br>Alternate: IFRP_OUT, SWDIO, SPI1_MISO <sup>(5)</sup>  |
| PA14               | 20   | I/O                     | 5VT                      | Default: PA14<br>Alternate: USART0_TX <sup>(3)</sup> , USART1_TX <sup>(4)</sup> , SWCLK, SPI1_MOSI <sup>(5)</sup>          |

**Notes:**

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32F130F4 devices only.
- (4) Functions are available on GD32F130F8/6 devices.
- (5) Functions are available on GD32F130F8 devices.

## 2.6.7. GD32F130xx pin alternate functions

**Table 2-9. Port A alternate functions summary**

| Pin Name | AF0           | AF1  | AF2                              | AF3      | AF4                      | AF5         | AF6                     |
|----------|---------------|--|----------------------------------|----------|--------------------------|-------------|-------------------------|
| PA0      |               | USART0_CTS <sup>(1)</sup><br>USART1_CTS <sup>(2)</sup>       | TIMER1_C<br>H0<br>TIMER1_E<br>TI |          | I2C1_SCL <sup>(3)</sup>  |             |                         |
| PA1      | EVENTOUT      | USART0_RT0_DE <sup>(1)</sup><br>USART1_RT0_DE <sup>(2)</sup> | TIMER1_C<br>H1                   |          | I2C1_SDA <sup>(3)</sup>  |             |                         |
| PA2      | TIMER14_CH0   | USART0_TX <sup>(1)</sup><br>USART1_TX <sup>(2)</sup>         | TIMER1_C<br>H2                   |          |                          |             |                         |
| PA3      | TIMER14_CH1   | USART0_RX <sup>(1)</sup><br>USART1_RX <sup>(2)</sup>         | TIMER1_C<br>H3                   |          |                          |             |                         |
| PA4      | SPI0_NSS      | USART0_CK <sup>(1)</sup><br>USART1_CK <sup>(2)</sup>         |                                  |          | TIMER13_CH0              |             | SPI1_NSS <sup>(3)</sup> |
| PA5      | SPI0_SCK      |  | TIMER1_C<br>H0<br>TIMER1_E<br>TI |          |                          |             |                         |
| PA6      | SPI0_MISO     | TIMER2_C<br>H0   | TIMER0_B<br>RKIN                 |          |                          | TIMER15_CH0 | EVENTOUT                |
| PA7      | SPI0_MOSI     | TIMER2_C<br>H1   | TIMER0_C<br>H0_ON                |          | TIMER13_CH0              | TIMER16_CH0 | EVENTOUT                |
| PA8      | CK_OUT        | USART0_CK  | TIMER0_C<br>H0                   | EVENTOUT | USART1_TX <sup>(2)</sup> |             |                         |
| PA9      | TIMER14_BRKIN | USART0_TX  | TIMER0_C<br>H1                   |          | I2C0_SCL                 |             |                         |
| PA10     | TIMER16_BRKIN | USART0_RX  | TIMER0_C<br>H2                   |          | I2C0_SDA                 |             |                         |
| PA11     | EVENTOUT      | USART0_CTS   | TIMER0_C<br>H3                   |          |                          |             |                         |
| PA12     | EVENTOUT      | USART0_RT0_DE  | TIMER0_E                         |          |                          |             |                         |

|      |          |  |                                  |              |  |  |                              |
|------|----------|--|----------------------------------|--------------|--|--|------------------------------|
|      | T        | TS/USART<br>0_DE   | TI                               |              |  |  |                              |
| PA13 | SWDIO    | IFRP_OUT   |                                  |              |  |  | SPI1_MISO<br>(3)             |
| PA14 | SWCLK    | USART0_T<br>X <sup>(1)</sup><br>USART1_T<br>X <sup>(2)</sup> |                                  |              |  |  | SPI1_MOSI<br>(3)             |
| PA15 | SPI0_NSS | USART0_R<br>X <sup>(1)</sup><br>USART1_R<br>X <sup>(2)</sup> | TIMER1_C<br>H0<br>TIMER1_E<br>TI | EVENTOU<br>T |  |  | SPI1_NSS <sup>(3)</sup><br>) |

**Notes:**

- (1) Functions are available on GD32F130x4 devices only.  
(2) Functions are available on GD32F130x8/6 devices.  
(3) Functions are available on GD32F130x8 devices.

**Table 2-10. Port B alternate functions summary**

| Pin Name | AF0                     | AF1                          | AF2                | AF3           | AF4                          | AF5 | AF6                     |
|----------|-------------------------|------------------------------|--------------------|---------------|------------------------------|-----|-------------------------|
| PB0      | EVENTOU<br>T            | TIMER2_C<br>H2               | TIMER0_C<br>H1_ON  |               | USART1_R<br>X <sup>(2)</sup> |     |                         |
| PB1      | TIMER13_<br>CH0         | TIMER2_C<br>H3               | TIMER0_C<br>H2_ON  |               |                              |     | SPI1_SCK <sup>(3)</sup> |
| PB2      |                         |                              |                    |               |                              |     |                         |
| PB3      | SPI0_SCK                | EVETOUT                      | TIMER1_C<br>H1     |               |                              |     |                         |
| PB4      | SPI0_MISO               | TIMER2_C<br>H0               | EVENTOU<br>T       |               |                              |     |                         |
| PB5      | SPI0_MOSI               | TIMER2_C<br>H1               | TIMER15_<br>BRKIN  | I2C0_SMB<br>A |                              |     |                         |
| PB6      | USART0_T<br>X           | I2C0_SCL                     | TIMER15_<br>CH0_ON |               |                              |     |                         |
| PB7      | USART0_R<br>X           | I2C0_SDA                     | TIMER16_<br>CH0_ON |               |                              |     |                         |
| PB8      |                         | I2C0_SCL                     | TIMER15_<br>CH0    |               |                              |     |                         |
| PB9      | IFRP_OUT                | I2C0_SDA                     | TIMER16_<br>CH0    | EVENTOU<br>T  |                              |     |                         |
| PB10     |                         | I2C1_SCL <sup>(3)</sup><br>) | TIMER1_C<br>H2     |               |                              |     |                         |
| PB11     | EVENTOU<br>T            | I2C1_SDA <sup>(3)</sup>      | TIMER1_C<br>H3     |               |                              |     |                         |
| PB12     | SPI0_NSS <sup>(3)</sup> | EVENTOU                      | TIMER0_B           |               | I2C1_SMB                     |     |                         |

|      |  |                 |                   |                    |                  |  |  |
|------|--|-----------------|-------------------|--------------------|------------------|--|--|
|      | <sup>1)</sup><br>SPI1_NSS(<br><sup>3)</sup>  | T               | RKIN              |                    | A <sup>(3)</sup> |  |  |
| PB13 | <sup>1)</sup><br>SPI0_SCK(<br><sup>3)</sup><br><sup>1)</sup><br>SPI1_SCK(<br><sup>3)</sup>     |                 | TIMER0_C<br>H0_ON |                    |                  |  |  |
| PB14 | <sup>(1)</sup><br>SPI0_MISO<br><sup>(3)</sup><br><sup>(1)</sup><br>SPI1_MISO<br><sup>(3)</sup> | TIMER14_<br>CH0 | TIMER0_C<br>H1_ON |                    |                  |  |  |
| PB15 | <sup>(1)</sup><br>SPI0_MOSI<br><sup>(3)</sup><br><sup>(1)</sup><br>SPI1_MOSI<br><sup>(3)</sup> | TIMER14_<br>CH1 | TIMER0_C<br>H2_ON | TIMER14_<br>CH0_ON |                  |  |  |

**Notes:**

- (1) Functions are available on GD32F130x4 devices only.
- (2) Functions are available on GD32F130x8/6 devices.
- (3) Functions are available on GD32F130x8 devices.

**Table 2-11. Port C & D & F alternate functions summary**

| Pin Name | AF0  | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 |
|----------|--|-----|-----|-----|-----|-----|-----|
| PC0      | EVENTO<br>T  |     |     |     |     |     |     |
| PC1      | EVENTO<br>T  |     |     |     |     |     |     |
| PC2      | EVENTO<br>T  |     |     |     |     |     |     |
| PC3      | EVENTO<br>T  |     |     |     |     |     |     |
| PC4      | EVENTO<br>T  |     |     |     |     |     |     |
| PC6      | TIMER2_C<br>H0   |     |     |     |     |     |     |
| PC7      | TIMER2_C<br>H1   |     |     |     |     |     |     |
| PC8      | TIMER2_C<br>H2   |     |     |     |     |     |     |
| PC9      | TIMER2_C<br>H3   |     |     |     |     |     |     |
| PD2      | TIMER2_E<br>TI   |     |     |     |     |     |     |
| PF4      | SPI1_NSS,<br>EVENTO<br>T                                     |     |     |     |     |     |     |
| PF5      | EVENTO<br>T  |     |     |     |     |     |     |
| PF6      | I2C0_SCL <sup>(1)</sup><br>)<br>I2C1_SCL <sup>(2)</sup><br>) |     |     |     |     |     |     |
| PF7      | I2C0_SDA <sup>(1)</sup><br>)<br>I2C1_SDA <sup>(2)</sup><br>) |     |     |     |     |     |     |

**Notes:**

(1) Functions are available on GD32F130x4/6 devices.

(2) Functions are available on GD32F130x8 devices only.

## 3. Functional description

### 3.1. Arm® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of Arm® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit Arm® Cortex®-M3 processor core
- Up to 48 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the Armv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

### 3.2. On-chip memory

- Up to 64 Kbytes of Flash memory
- The region of the MCU executing instructions without waiting time is up to 32K bytes (in case that the Flash size equal to 16K or 32K, all memory is no waiting time). A long time delay when CPU fetches the instructions out of the range.
- Up to 8 Kbytes of SRAM with hardware parity checking

The Arm® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 64 Kbytes of inner Flash at most, which includes code Flash and data Flash is available for storing programs and data, and there is no waiting time within code Flash area when CPU executes instructions. The [Table 2-2. GD32F130xx memory map](#) shows the memory map of the GD32F130xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

### 3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 48 MHz. See [Figure 2-8. GD32F130xx clock tree](#) for details on the clock tree.

GD32F1x0 Reset Control includes the control of three kinds of reset: power reset, system reset and backup domain reset. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when  $V_{DD}$  is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- $V_{DD}$  range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through VDD pins.
- $V_{SSA}$ ,  $V_{DDA}$  range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL.  $V_{DDA}$  and  $V_{SSA}$  must be connected to VDD and VSS, respectively.
- $V_{BAT}$  range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

### 3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PA2 and PA3, PA14 and PA15).

### 3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep mode**

In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, the RTC tamper and timestamp, the USART0 wakeup and the CEC wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

- **Standby mode**

In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

### 3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 1 MSPS.
- Input voltage range:  $V_{SSA}$  to  $V_{DDA}$  (2.6 to 3.6 V).
- Temperature sensor.

One 12-bit 1 MSPS multi-channel ADCs are integrated in the device. It is a total of up to 16 multiplexed external channels, 1 channel for internal temperature sensor ( $V_{SENSE}$ ), 1 channel for internal reference voltage ( $V_{REFINT}$ ) and 1 channel for battery voltage ( $V_{BAT}$ ). The input voltage range is between  $V_{SSA}$  and  $V_{DDA}$ . An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general timers (TIMERx, x=1,2,14) and the advanced timers (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC\_IN16 input channel which is used to convert the sensor output voltage into a digital value. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.



### 3.7. DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

### 3.8. General-purpose inputs/outputs (GPIOs)

- Up to 55 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 55 general purpose I/O pins (GPIO) in GD32F130xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4-PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

### 3.9. Timers and PWM generation

- One 16-bit advanced timer (TIMER0), one 32-bit general timer (TIMER1) and five 16-bit general timers (TIMER2, TIMER13 ~ TIMER16)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels.

It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, generation of PWM waveform (edge-aligned or center-aligned mode) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMEx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The GD32F130xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler, It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wake up interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

### 3.10. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers
- Calendar with subsecond, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

### 3.11. Inter-integrated circuit (I2C)

- Up to two I2Cs bus interfaces can support both master and slave mode with a frequency up to 400 KHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

### 3.12. Serial peripheral interface (SPI)

- Up to two SPIs interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

### 3.13. Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating speed up to 6 Mbit/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support

- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

### 3.14. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

### 3.15. Package and operation temperature

- LQFP64 (GD32F130Rx), LQFP48 (GD32F130Cx), LQFP32 (GD32F130Kx), QFN32 (GD32F130Kx), QFN28 (GD32F130Gx) and TSSOP20 (GD32F130Fx)
- Operation temperature range: -40°C to +85°C (industrial level)

## 4. Electrical characteristics

### 4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4-1. Absolute maximum ratings<sup>(1)(4)</sup>**

| Symbol               | Parameter  | Min             | Max             | Unit |
|----------------------|--|-----------------|-----------------|------|
| $V_{DD}$             | External voltage range <sup>(2)</sup>                    | $V_{SS} - 0.3$  | $V_{SS} + 3.6$  | V    |
| $V_{DDA}$            | External analog supply voltage                           | $V_{SSA} - 0.3$ | $V_{SSA} + 3.6$ | V    |
| $V_{BAT}$            | External battery supply voltage                          | $V_{SS} - 0.3$  | $V_{SS} + 3.6$  | V    |
| $V_{IN}$             | Input voltage on 5V tolerant pin <sup>(3)</sup>          | $V_{SS} - 0.3$  | $V_{DD} + 4.0$  | V    |
|                      | Input voltage on other I/O                               | $V_{SS} - 0.3$  | 4.0             | V    |
| $ \Delta V_{DDX} $   | Variations between different VDD power pins              | —               | 50              | mV   |
| $ V_{SSX} - V_{SS} $ | Variations between different ground pins                 | —               | 50              | mV   |
| $I_{IO}$             | Maximum current for GPIO pins                            | —               | $\pm 25$        | mA   |
| $T_A$                | Operating temperature range                              | -40             | +85             | °C   |
| $P_D$                | Power dissipation at $T_A = 85^\circ\text{C}$ of LQFP64  | —               | 629             | mW   |
|                      | Power dissipation at $T_A = 85^\circ\text{C}$ of LQFP48  | —               | 621             |      |
|                      | Power dissipation at $T_A = 85^\circ\text{C}$ of LQFP32  | —               | 605             |      |
|                      | Power dissipation at $T_A = 85^\circ\text{C}$ of QFN32   | —               | 825             |      |
|                      | Power dissipation at $T_A = 85^\circ\text{C}$ of QFN28   | —               | 605             |      |
|                      | Power dissipation at $T_A = 85^\circ\text{C}$ of TSSOP20 | —               | 482             |      |
| $T_{STG}$            | Storage temperature range                                | -55             | +150            | °C   |
| $T_J$                | Maximum junction temperature                             | —               | +125            | °C   |

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3)  $V_{IN}$  maximum value cannot exceed 5.5 V.

(4) It is recommended that  $V_{DD}$  and  $V_{DDA}$  are powered by the same source. The maximum difference between  $V_{DD}$  and  $V_{DDA}$  does not exceed 300 mV during power-up and operation.

### 4.2. Operating conditions characteristics

**Table 4-2. DC operating conditions**

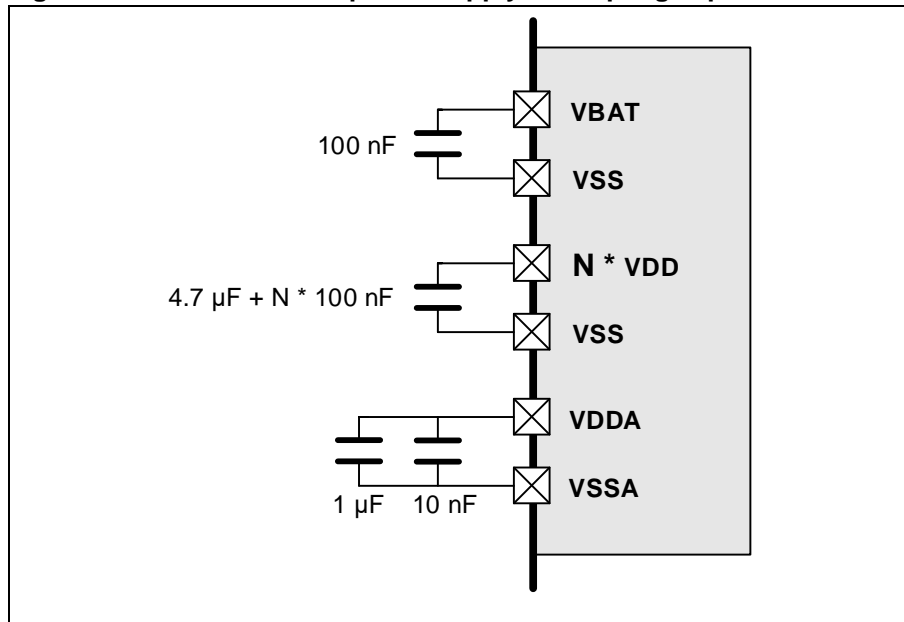
| Symbol    | Parameter              | Conditions       | Min                | Typ | Max <sup>(1)</sup> | Unit |
|-----------|------------------------|------------------|--------------------|-----|--------------------|------|
| $V_{DD}$  | Supply voltage         | —                | 2.6                | 3.3 | 3.6                | V    |
| $V_{DDA}$ | Analog supply voltage  | Same as $V_{DD}$ | 2.6                | 3.3 | 3.6                | V    |
| $V_{BAT}$ | Battery supply voltage | —                | 1.8 <sup>(2)</sup> | —   | 3.6                | V    |

(1) Based on characterization, not tested in production.

(2) In the application which  $V_{BAT}$  supply the backup domains, if the  $V_{BAT}$  voltage drops below the minimum value,

when  $V_{DD}$  is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

**Figure 4-1. Recommended power supply decoupling capacitors<sup>(1)</sup>**



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board. More details refer to **AN108 GD32F1x0 Hardware Development Guide**.

**Table 4-3. Clock frequency<sup>(1)</sup>**

| Symbol      | Parameter            | Conditions | Min | Max | Unit |
|-------------|----------------------|------------|-----|-----|------|
| $f_{HCLK1}$ | AHB1 clock frequency | —          | —   | 48  | MHz  |
| $f_{HCLK2}$ | AHB2 clock frequency | —          | —   | 48  | MHz  |
| $f_{APB1}$  | APB1 clock frequency | —          | —   | 48  | MHz  |
| $f_{APB2}$  | APB2 clock frequency | —          | —   | 48  | MHz  |

(1) Guaranteed by design, not tested in production.

**Table 4-4. Operating conditions at Power up/ Power down<sup>(1)</sup>**

| Symbol    | Parameter               | Conditions | Min | Max      | Unit                   |
|-----------|-------------------------|------------|-----|----------|------------------------|
| $t_{VDD}$ | $V_{DD}$ rise time rate | —          | 0   | $\infty$ | $\mu\text{s}/\text{v}$ |
|           | $V_{DD}$ fall time rate |            | 20  | $\infty$ |                        |

(1) Guaranteed by design, not tested in production.

**Table 4-5. Start-up timings of Operating conditions<sup>(1)(2)(3)</sup>**

| Symbol                | Parameter     | Conditions              | Typ | Unit          |
|-----------------------|---------------|-------------------------|-----|---------------|
| $t_{\text{start-up}}$ | Start-up time | Clock source from HXTAL | 19  | ms            |
|                       |               | Clock source from IRC8M | 19  | $\mu\text{s}$ |

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

(3) PLL is off.

**Table 4-6. Power saving mode wakeup timings characteristics<sup>(1)(2)</sup>**

| Symbol                  | Parameter                                     | Typ | Unit          |
|-------------------------|---|-----|---------------|
| $t_{\text{sleep}}$      | Wakeup from Sleep mode                        | 3.3 | $\mu\text{s}$ |
| $t_{\text{Deep-sleep}}$ | Wakeup from Deep-sleep mode (LDO in run mode) | 4.9 |               |

| Symbol               | Parameter   | Typ | Unit |
|----------------------|---|-----|------|
|                      | Wakeup from Deep-sleep mode (LDO in low power mode) | 4.9 |      |
| $t_{\text{Standby}}$ | Wakeup from Standby mode                            | 21  | ms   |

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions:  $V_{\text{DD}} = V_{\text{DDA}} = 3.3\text{ V}$ , IRC8M = System clock = 8MHz.

### 4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

**Table 4-7. Power consumption characteristics**<sup>(2)(3)(3)(4)(5)(6)</sup>

| Symbol                           | Parameter                   | Conditions   | Min | Typ <sup>(1)</sup> | Max | Unit |
|----------------------------------|-----------------------------|--|-----|--------------------|-----|------|
| $I_{\text{DD}} + I_{\text{DDA}}$ | Supply current (Run mode)   | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System clock=48 MHz, All peripherals enabled                  | —   | 18.5               | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System clock =48 MHz, All peripherals disabled                | —   | 13.2               | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System clock =36 MHz, All peripherals enabled                 | —   | 14.6               | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System Clock =36 MHz, All peripherals disabled                | —   | 10.5               | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System clock =24 MHz, All peripherals enabled                 | —   | 10.3               | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System Clock =24 MHz, All peripherals disabled                | —   | 7.5                | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System clock =16 MHz, All peripherals enabled                 | —   | 7.4                | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System Clock =16 MHz, All peripherals disabled                | —   | 5.6                | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System clock =8 MHz, All peripherals enabled                  | —   | 4.5                | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, System Clock =8 MHz, All peripherals disabled                 | —   | 3.6                | —   | mA   |
|                                  | Supply current (Sleep mode) | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals enabled  | —   | 11.6               | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals disabled | —   | 5.1                | —   | mA   |
|                                  |                             | $V_{\text{DD}}=V_{\text{DDA}}=3.3\text{V}$ , HXTAL=8MHz, CPU clock off, System clock =36 MHz, All peripherals enabled  | —   | 9.1                | —   | mA   |

| Symbol  | Parameter                        | Conditions  | Min   | Typ <sup>(1)</sup> | Max  | Unit |
|---|----------------------------------|---|---|--------------------|------|------|
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, HXTAL=8MHz, CPU clock off, System clock =36 MHz, All peripherals disabled | —   | 4.2                | —    | mA   |
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, HXTAL=8MHz, CPU clock off, System clock =24 MHz, All peripherals enabled  | —   | 6.6                | —    | mA   |
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, HXTAL=8MHz, CPU clock off, System clock =24 MHz, All peripherals disabled | —   | 3.4                | —    | mA   |
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, HXTAL=8MHz, CPU clock off, System clock =16 MHz, All peripherals enabled  | —   | 5.0                | —    | mA   |
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, HXTAL=8MHz, CPU clock off, System clock =16 MHz, All peripherals disabled | —   | 2.8                | —    | mA   |
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, HXTAL=8MHz, CPU clock off, System clock =8 MHz, All peripherals enabled   | —   | 3.3                | —    | mA   |
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, HXTAL=8MHz, CPU clock off, System clock =8 MHz, All peripherals disabled  | —   | 2.2                | —    | mA   |
|   | Supply current (Deep-sleep mode) | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, Regulator in run mode, IRC40K off, RTC off                                | —   | 263                | 1100 | μA   |
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, Regulator in low power mode, IRC40K off, RTC off                          | —   | 255                | —    | μA   |
|   | Supply current (Standby mode)    | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, LXTAL off, IRC40K on, RTC on  | —   | 7.3                | —    | μA   |
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, LXTAL off, IRC40K on, RTC off   | —   | 6.8                | —    | μA   |
|   |                                  | V <sub>DD</sub> = V <sub>D<sub>DDA</sub></sub> =3.3V, LXTAL off, IRC40K off, RTC off  | —   | 5.5                | 27.5 | μA   |
|   | IBAT                             | Battery supply current  | V <sub>DD</sub> and V <sub>D<sub>DDA</sub></sub> not available, V <sub>BAT</sub> =3.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving | —                  | 2.6  | —    |
| V <sub>DD</sub> and V <sub>D<sub>DDA</sub></sub> not available, V <sub>BAT</sub> =3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving |                                  |   | —   | 2.4                | —    | μA   |
| V <sub>DD</sub> and V <sub>D<sub>DDA</sub></sub> not available, V <sub>BAT</sub> =2.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving |                                  |   | —   | 1.9                | —    | μA   |
| V <sub>DD</sub> and V <sub>D<sub>DDA</sub></sub> not available, V <sub>BAT</sub> =1.8 V, LXTAL on with external crystal, RTC on, LXTAL High driving |                                  |   | —   | 1.3                | —    | μA   |



| Symbol | Parameter | Conditions   | Min | Typ <sup>(1)</sup> | Max | Unit |
|--------|-----------|--|-----|--------------------|-----|------|
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | —   | 2.6                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | —   | 2.3                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =2.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | —   | 1.8                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | —   | 1.3                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving  | —   | 1.5                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving  | —   | 1.4                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =2.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving  | —   | 1.2                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving  | —   | 1.0                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =3.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving         | —   | 1.4                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving         | —   | 1.3                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =2.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving         | —   | 1.1                | —   | μA   |
|        |           | V <sub>DD</sub> and V <sub>DDA</sub> not available, V <sub>BAT</sub> =1.8 V, LXTAL on with external crystal, RTC on, LXTAL Low driving         | —   | 0.9                | —   | μA   |

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for T<sub>A</sub> = 25 °C and test result is mean value.

(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

(5) When analog peripheral blocks such as ADCs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

(6) All GPIOs are configured as analog mode except standby mode.

Figure 4-2. Typical supply current consumption in Run mode

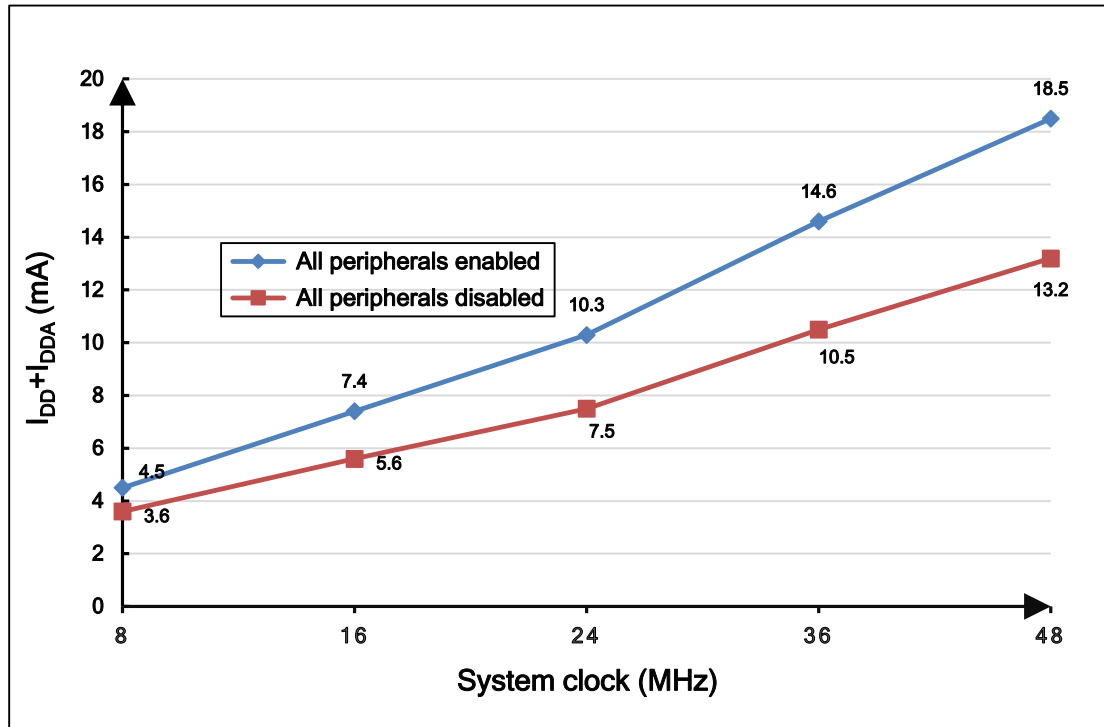
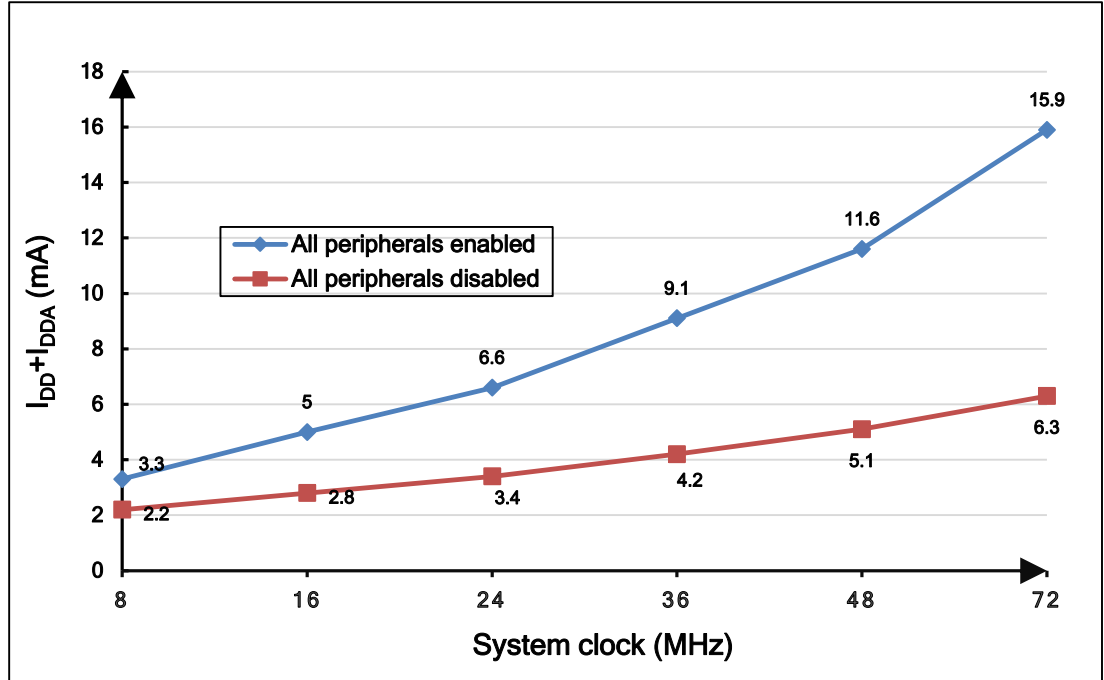


Figure 4-3. Typical supply current consumption in Sleep mode



#### 4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is

given in the [Table 4-8. EMS characteristics](#), based on the EMS levels and classes compliant with IEC 61000 series standard.

**Table 4-8. EMS characteristics<sup>(1)</sup>**

| Symbol           | Parameter  | Conditions  | Level/Class |
|------------------|--|---|-------------|
| V <sub>ESD</sub> | Voltage applied to all device pins to induce a functional disturbance  | V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = +25 °C<br>conforms to IEC 61000-4-2 | 3B          |
| V <sub>FTB</sub> | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V <sub>DD</sub> and V <sub>SS</sub> pins | V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = +25 °C<br>conforms to IEC 61000-4-4 | 4A          |

(1) Based on characterization, not tested in production.

EMI (Electromagnetic Interference) emission test result is given in the [Table 4-9. EMI characteristics<sup>\(1\)</sup>](#), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

**Table 4-9. EMI characteristics<sup>(1)</sup>**

| Symbol           | Parameter  | Conditions   | Tested frequency band | Max vs.<br>[f <sub>HXTAL</sub> /f <sub>HCLK</sub> ] | Unit |
|------------------|------------|--|-----------------------|---|------|
|                  |            |  |                       | 8/48 MHz  |      |
| S <sub>EMI</sub> | Peak level | V <sub>DD</sub> = 3.6 V, T <sub>A</sub> = +25 °C,<br>LQFP64, f <sub>HCLK</sub> = 48 MHz,<br>conforms to SAE J1752-<br>3:2017 | 0.15 to 30 MHz        | 9.83  | dBμV |
|                  |            |  | 30 to 130 MHz         | 9.00  |      |
|                  |            |  | 130 MHz to 1GHz       | 14.64   |      |

(1) Based on characterization, not tested in production.

## 4.5. Power supply supervisor characteristics

**Table 4-10. Power supply supervisor characteristics**

| Symbol                        | Parameter                      | Conditions                    | Min | Typ   | Max | Unit |
|-------------------------------|--------------------------------|-------------------------------|-----|-------|-----|------|
| $V_{LVD}^{(1)}$               | Low Voltage Detector Threshold | LVDT<2:0> = 000(rising edge)  | —   | 2.123 | —   | V    |
|                               |                                | LVDT<2:0> = 000(falling edge) | —   | 2.019 | —   | V    |
|                               |                                | LVDT<2:0> = 001(rising edge)  | —   | 2.213 | —   | V    |
|                               |                                | LVDT<2:0> = 001(falling edge) | —   | 2.181 | —   | V    |
|                               |                                | LVDT<2:0> = 010(rising edge)  | —   | 2.31  | —   | V    |
|                               |                                | LVDT<2:0> = 010(falling edge) | —   | 2.194 | —   | V    |
|                               |                                | LVDT<2:0> = 011(rising edge)  | —   | 2.404 | —   | V    |
|                               |                                | LVDT<2:0> = 011(falling edge) | —   | 2.304 | —   | V    |
|                               |                                | LVDT<2:0> = 100(rising edge)  | —   | 2.505 | —   | V    |
|                               |                                | LVDT<2:0> = 100(falling edge) | —   | 2.382 | —   | V    |
|                               |                                | LVDT<2:0> = 101(rising edge)  | —   | 2.604 | —   | V    |
|                               |                                | LVDT<2:0> = 101(falling edge) | —   | 2.498 | —   | V    |
|                               |                                | LVDT<2:0> = 110(rising edge)  | —   | 2.702 | —   | V    |
|                               |                                | LVDT<2:0> = 110(falling edge) | —   | 2.59  | —   | V    |
| LVDT<2:0> = 111(rising edge)  | —                              | 2.803                         | —   | V     |     |      |
| LVDT<2:0> = 111(falling edge) | —                              | 2.684                         | —   | V     |     |      |
| $V_{LVDhyst}^{(2)}$           | LVD hysteresis                 | —                             | —   | 100   | —   | mV   |
| $V_{POR}^{(1)}$               | Power on reset threshold       | PDRVS = 0                     | —   | 2.4   | —   | V    |
| $V_{PDR}^{(1)}$               | Power down reset threshold     |                               | —   | 2.35  | —   | V    |
| $V_{PDRhyst}^{(2)}$           | PDR hysteresis                 |                               | —   | 0.05  | —   | V    |
| $t_{RSTTEMPO}^{(2)}$          | Reset temporization            |                               | —   | 2     | —   | ms   |
| $V_{POR}^{(1)}$               | Power on reset threshold       | PDRVS = 1                     | —   | 2.4   | —   | V    |
| $V_{PDR}^{(1)}$               | Power down reset threshold     |                               | —   | 1.8   | —   | V    |
| $V_{PDRhyst}^{(2)}$           | PDR hysteresis                 |                               | —   | 0.6   | —   | V    |
| $t_{RSTTEMPO}^{(2)}$          | Reset temporization            |                               | —   | 2     | —   | ms   |

- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.

## 4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

**Table 4-11. ESD characteristics**

| Symbol         | Parameter   | Conditions                                      | Min | Typ | Max  | Unit |
|----------------|---|---|-----|-----|------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model)    | $T_A=25\text{ }^\circ\text{C}$ ; JS-001-2014    | —   | —   | 5000 | V    |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A=25\text{ }^\circ\text{C}$ ;<br>JS-002-2014 | —   | —   | 500  | V    |

**Table 4-12. Static latch-up characteristics**

| Symbol | Parameter                        | Conditions                              | Min | Typ | Max       | Unit |
|--------|----------------------------------|---|-----|-----|-----------|------|
| LU     | I-test                           | $T_A=25\text{ }^\circ\text{C}$ ; JESD78 | —   | —   | $\pm 100$ | mA   |
|        | $V_{\text{supply}}$ over voltage |   | —   | —   | 5.4       | V    |

## 4.7. External clock characteristics

**Table 4-13. High speed crystal oscillator (HXTAL) generated from a crystal/ceramic characteristics**

| Symbol                 | Parameter  | Conditions                                     | Min | Typ | Max | Unit       |
|------------------------|--|--|-----|-----|-----|------------|
| $f_{HXTAL}^{(1)}$      | Crystal or ceramic frequency                         | $V_{DD}=3.3V$                                  | 4   | 8   | 32  | MHz        |
| $R_F^{(2)}$            | Feedback resistor                                    | —  | —   | 200 | —   | k $\Omega$ |
| $C_{HXTAL}^{(2)(3)}$   | Recommended matching capacitance on OSCIN and OSCOUT | —  | —   | 20  | 30  | pF         |
| $D_{ucy(HXTAL)}^{(2)}$ | Crystal or ceramic duty cycle                        | —  | 30  | 50  | 70  | %          |
| $g_m^{(2)}$            | Oscillator transconductance                          | Startup  | —   | 25  | —   | mA/V       |
| $I_{DDHXTAL}^{(1)}$    | HXTAL oscillator operating current                   | $V_{DD}=3.3V$ , $T_A=25\text{ }^\circ\text{C}$ | —   | 1.1 | —   | mA         |
| $t_{SUHXTAL}^{(1)}$    | HXTAL oscillator startup time                        | $V_{DD}=3.3V$ , $T_A=25\text{ }^\circ\text{C}$ | —   | 1.5 | —   | ms         |

- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.
- (3)  $C_{HXTAL1} = C_{HXTAL2} = 2 \cdot (C_{LOAD} - C_S)$ , For  $C_{HXTAL1}$  and  $C_{HXTAL2}$ , it is recommended matching capacitance on OSCIN and OSCOUT. For  $C_{LOAD}$ , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For  $C_S$ , it is PCB and MCU pin stray capacitance.

**Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)**

| Symbol                        | Parameter                                     | Conditions                      | Min                 | Typ | Max                 | Unit |
|-------------------------------|---|---------------------------------|---------------------|-----|---------------------|------|
| $f_{\text{HXTAL\_ext}}^{(1)}$ | External clock source or oscillator frequency | $V_{\text{DD}} = 3.3 \text{ V}$ | 1                   | —   | 50                  | MHz  |
| $V_{\text{HXTALH}}^{(2)}$     | OSCIN input pin high level voltage            | $V_{\text{DD}} = 3.3 \text{ V}$ | $0.7 V_{\text{DD}}$ | —   | $V_{\text{DD}}$     | V    |
| $V_{\text{HXTALL}}^{(2)}$     | OSCIN input pin low level voltage             |                                 | $V_{\text{SS}}$     | —   | $0.3 V_{\text{DD}}$ | V    |
| $t_{\text{H/L(HXTAL)}}^{(2)}$ | OSCIN high or low time                        | —                               | 5                   | —   | —                   | ns   |
| $t_{\text{R/F(HXTAL)}}^{(2)}$ | OSCIN rise or fall time                       | —                               | —                   | —   | 10                  | ns   |
| $C_{\text{IN}}^{(2)}$         | OSCIN input capacitance                       | —                               | —                   | 5   | —                   | pF   |
| $D_{\text{ucy(HXTAL)}}^{(2)}$ | Duty cycle                                    | —                               | 40                  | —   | 60                  | %    |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics**

| Symbol                        | Parameter  | Conditions                    | Min | Typ    | Max | Unit            |
|-------------------------------|--|-------------------------------|-----|--------|-----|-----------------|
| $f_{\text{LXTAL}}^{(1)}$      | Low Speed crystal oscillator (LXTAL) frequency           | $V_{\text{DD}} = 3.3\text{V}$ | —   | 32.768 | —   | KHz             |
| $C_{\text{LXTAL}}^{(2)(3)}$   | Recommended matching capacitance on OSC32IN and OSC32OUT | —                             | —   | 10     | —   | pF              |
| $D_{\text{ucy(LXTAL)}}^{(2)}$ | Crystal or ceramic duty cycle                            | —                             | 48  | 50     | 52  | %               |
| $g_{\text{m}}^{(2)}$          | Oscillator transconductance                              | Lower driving capability      | —   | 4      | —   | $\mu\text{A/V}$ |
|                               |  | Higher driving capability     | —   | 18     | —   |                 |
| $I_{\text{DDLXTAL}}^{(1)}$    | LXTAL oscillator operating current                       | Lower driving capability      | —   | 0.9    | —   | $\mu\text{A}$   |
|                               |  | Higher driving capability     | —   | 1.9    | —   |                 |
| $t_{\text{SULXTAL}}^{(1)(4)}$ | LXTAL oscillator startup time                            | Lower driving capability      | —   | 1.36   | —   | s               |
|                               |  | Higher driving capability     | —   | 0.55   | —   | s               |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3)  $C_{\text{LXTAL1}} = C_{\text{LXTAL2}} = 2 \cdot (C_{\text{LOAD}} - C_{\text{S}})$ , For  $C_{\text{LXTAL1}}$  and  $C_{\text{LXTAL2}}$ , it is recommended matching capacitance on OSC32IN and OSC32OUT. For  $C_{\text{LOAD}}$ , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For  $C_{\text{S}}$ , it is PCB and MCU pin stray capacitance.

(4)  $t_{\text{SULXTAL}}$  is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

**Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)**

| Symbol                 | Parameter                                     | Conditions              | Min          | Typ    | Max          | Unit |
|------------------------|---|-------------------------|--------------|--------|--------------|------|
| $f_{LXTAL\_ext}^{(1)}$ | External clock source or oscillator frequency | $V_{DD} = 3.3\text{ V}$ | —            | 32.768 | 1000         | kHz  |
| $V_{LXTALH}^{(2)}$     | OSC32IN input pin high level voltage          | —                       | $0.7 V_{DD}$ | —      | $V_{DD}$     | V    |
| $V_{LXTALL}^{(2)}$     | OSC32IN input pin low level voltage           | —                       | $V_{SS}$     | —      | $0.3 V_{DD}$ |      |
| $t_{H/L(LXTAL)}^{(2)}$ | OSC32IN high or low time                      | —                       | 450          | —      | —            | ns   |
| $t_{R/F(LXTAL)}^{(2)}$ | OSC32IN rise or fall time                     | —                       | —            | —      | 50           |      |
| $C_{IN}^{(2)}$         | OSC32IN input capacitance                     | —                       | —            | 5      | —            | pF   |
| $Ducy_{(LXTAL)}^{(2)}$ | Duty cycle                                    | —                       | 30           | 50     | 70           | %    |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

## 4.8. Internal clock characteristics

**Table 4-17. Internal 8 MHz RC oscillator (IRC8M) characteristics**

| Symbol                                 | Parameter  | Conditions   | Min | Typ          | Max | Unit    |
|--|--|--|-----|--------------|-----|---------|
| $f_{IRC8M}$                            | Internal 8 MHz RC oscillator (IRC8M) frequency                         | $V_{DD}=V_{VDDA}=3.3V$   | —   | 8            | —   | MHz     |
| $ACC_{IRC8M}$                          | IRC8M oscillator Frequency accuracy, Factory-trimmed                   | $V_{DD}=V_{VDDA}=3.3V$ ,<br>$T_A=-40^{\circ}C \sim +85^{\circ}C$ | —   | -1.7<br>~1.4 | —   | %       |
|  |  | $V_{DD}=V_{VDDA}=3.3V$ , $T_A=25^{\circ}C$                       | -1  | —            | +1  | %       |
|  | IRC8M oscillator Frequency accuracy, User trimming step <sup>(1)</sup> | —  | —   | 0.5          | —   | %       |
| $Ducy_{IRC8M}^{(2)}$                   | IRC8M oscillator duty cycle  | $V_{DD}=V_{VDDA}=3.3V$ , $f_{IRC8M}=8MHz$                        | 48  | 50           | 52  | %       |
| $I_{DDIRC8M}$<br>$+I_{DDAIRC8M}^{(1)}$ | IRC8M oscillator operating current                                     | $V_{DD}=V_{VDDA}=3.3V$ , $f_{IRC8M}=8MHz$                        | —   | 39           | 100 | $\mu A$ |
| $t_{SUIRC8M}^{(1)}$                    | IRC8M oscillator startup time  | $V_{DD}=V_{VDDA}=3.3V$ , $f_{IRC8M}=8MHz$                        | —   | 3.6          | —   | us      |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-18. Internal 40KHz RC oscillator (IRC40K) characteristics**

| Symbol                                     | Parameter                                       | Conditions   | Min | Typ   | Max | Unit    |
|--|---|--|-----|-------|-----|---------|
| $f_{IRC40K}^{(1)}$                         | Internal 40KHz RC oscillator (IRC40K) frequency | $V_{DD}=V_{VDDA}=3.3V$ ,<br>$T_A=-40^{\circ}C \sim +85^{\circ}C$ | —   | 40    | —   | KHz     |
| $I_{DDIRC40KI}$<br>$+I_{DDAIRC40KI}^{(2)}$ | IRC40K oscillator operating current             | $V_{DD}=V_{VDDA}=3.3V$ , $T_A=25^{\circ}C$                       | —   | 1.3   | —   | $\mu A$ |
| $t_{SUIRC40K}^{(2)}$                       | IRC40K oscillator startup                       | $V_{DD}=V_{CDDA}=3.3V$ , $T_A=25^{\circ}C$                       | —   | 115.7 | —   | $\mu s$ |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|        | time      |            |     |     |     |      |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

**Table 4-19. High speed internal clock (IRC14M) characteristics**

| Symbol                                   | Parameter   | Conditions  | Min | Typ            | Max | Unit    |
|--|---|---|-----|----------------|-----|---------|
| $f_{IRC14M}$                             | High Speed Internal Oscillator (IRC14M) frequency                       | $V_{DD}=V_{DDA}=3.3V$   | —   | 14             | —   | MHz     |
| $ACC_{IRC14M}$                           | IRC14M oscillator Frequency accuracy, Factory-trimmed                   | $V_{DD}=V_{DDA}=3.3V$ ,<br>$T_A=-40^{\circ}C \sim +85^{\circ}C$ | —   | -0.9~<br>0.029 | —   | %       |
|  |   | $V_{DD}=V_{CDDA}=3.3V$ , $T_A=25^{\circ}C$                      | -1  | —              | +1  | %       |
|  | IRC14M oscillator Frequency accuracy, User trimming step <sup>(1)</sup> | —   | —   | 0.5            | —   | %       |
| $D_{IRC14M}^{(2)}$                       | IRC14M oscillator duty cycle  | $V_{DD}=V_{DDA}=3.3V$ ,<br>$f_{IRC14M}=14MHz$                   | 48  | 50             | 52  | %       |
| $I_{DDIRC14M}$<br>$+I_{DDAIRC14M}^{(1)}$ | IRC14M oscillator operating current                                     | $V_{DD}=V_{DDA}=3.3V$ ,<br>$f_{IRC14M}=14MHz$                   | —   | 54             | —   | $\mu A$ |
| $t_{SUIRC14M}^{(1)}$                     | IRC14M oscillator startup time  | $V_{DD}=V_{DDA}=3.3V$ ,<br>$f_{IRC14M}=14MHz$                   | —   | 2.9            | —   | $\mu s$ |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

## 4.9. PLL characteristics

**Table 4-20. PLL characteristics**

| Symbol                  | Parameter                            | Conditions        | Min | Typ   | Max | Unit    |
|-------------------------|--------------------------------------|-------------------|-----|-------|-----|---------|
| $f_{PLLIN}^{(1)}$       | PLL input clock frequency            | —                 | 1   | —     | 25  | MHz     |
| $f_{PLLOUT}^{(2)}$      | PLL output clock frequency           | —                 | 16  | —     | 72  | MHz     |
| $f_{VCO}^{(2)}$         | PLL VCO output clock frequency       | —                 | —   | —     | 72  | MHz     |
| $t_{LOCK}^{(2)}$        | PLL lock time                        | —                 | —   | —     | 300 | $\mu s$ |
| $I_{DDA}^{(1)}$         | Current consumption on $V_{DDA}$     | VCO freq = 48 MHz | —   | 270   | —   | $\mu A$ |
| $Jitter_{PLL}^{(1)(3)}$ | Cycle to cycle Jitter (rms)          | System clock      | —   | 32.1  | —   | ps      |
|                         | Cycle to cycle Jitter (peak to peak) |                   | —   | 255.6 | —   |         |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) Value given with main PLL running.



## 4.10. Memory characteristics

**Table 4-21. Flash memory characteristics**

| Symbol                                  | Parameter   | Conditions                       | Min <sup>(1)</sup> | Typ <sup>(1)</sup> | Max <sup>(2)</sup> | Unit    |
|---|---|----------------------------------|--------------------|--------------------|--------------------|---------|
| PE <sub>CYC</sub>                       | Number of guaranteed program /erase cycles before failure (Endurance) | T <sub>A</sub> = -40 °C ~ +85 °C | 100                | —                  | —                  | kcycles |
| t <sub>RET</sub>                        | Data retention time   | —                                | —                  | 20                 | —                  | years   |
| t <sub>PROG</sub>                       | Word programming time   | T <sub>A</sub> = -40°C ~ +85 °C  | —                  | 37.5               | 105                | μs      |
| t <sub>ERASE</sub>                      | Page erase time   | T <sub>A</sub> = -40°C ~ +85 °C  | —                  | 50                 | 400                | ms      |
| t <sub>MERASE(16K)</sub> <sup>(2)</sup> | Mass erase time   | T <sub>A</sub> = -40°C ~ +85 °C  | —                  | 0.3                | 3                  | s       |
| t <sub>MERASE(32K)</sub> <sup>(2)</sup> | Mass erase time   | T <sub>A</sub> = -40°C ~ +85 °C  | —                  | 0.6                | 6                  | s       |
| t <sub>MERASE(64K)</sub> <sup>(2)</sup> | Mass erase time   | T <sub>A</sub> = -40°C ~ +85 °C  | —                  | 1.2                | 12                 | s       |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

## 4.11. NRST pin characteristics

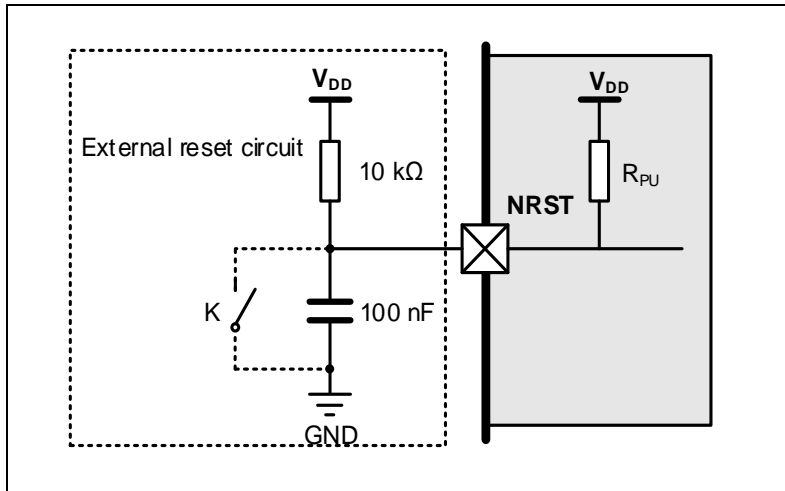
**Table 4-22. NRST pin characteristics**

| Symbol                               | Parameter                          | Conditions                                 | Min                 | Typ | Max                   | Unit |
|--------------------------------------|------------------------------------|--|---------------------|-----|-----------------------|------|
| V <sub>IL(NRST)</sub> <sup>(1)</sup> | NRST Input low level voltage       | V <sub>DD</sub> = V <sub>DDA</sub> = 2.6 V | -0.3                | —   | 0.3 V <sub>DD</sub>   | V    |
| V <sub>IH(NRST)</sub> <sup>(1)</sup> | NRST Input high level voltage      |  | 0.7 V <sub>DD</sub> | —   | V <sub>DD</sub> + 0.3 |      |
| V <sub>hyst</sub> <sup>(2)</sup>     | Schmidt trigger Voltage hysteresis |  | —                   | 330 | —                     | mV   |
| V <sub>IL(NRST)</sub> <sup>(1)</sup> | NRST Input low level voltage       | V <sub>DD</sub> = V <sub>DDA</sub> = 3.3 V | -0.3                | —   | 0.3 V <sub>DD</sub>   | V    |
| V <sub>IH(NRST)</sub> <sup>(1)</sup> | NRST Input high level voltage      |  | 0.7 V <sub>DD</sub> | —   | V <sub>DD</sub> + 0.3 |      |
| V <sub>hyst</sub> <sup>(2)</sup>     | Schmidt trigger Voltage hysteresis |  | —                   | 340 | —                     | mV   |
| V <sub>IL(NRST)</sub> <sup>(1)</sup> | NRST Input low level voltage       | V <sub>DD</sub> = V <sub>DDA</sub> = 3.6 V | -0.3                | —   | 0.3 V <sub>DD</sub>   | V    |
| V <sub>IH(NRST)</sub> <sup>(1)</sup> | NRST Input high level voltage      |  | 0.7 V <sub>DD</sub> | —   | V <sub>DD</sub> + 0.3 |      |
| V <sub>hyst</sub> <sup>(2)</sup>     | Schmidt trigger Voltage hysteresis |  | —                   | 350 | —                     | mV   |
| R <sub>pu</sub> <sup>(2)</sup>       | Pull-up equivalent resistor        | —  | —                   | 40  | —                     | kΩ   |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit<sup>(1)</sup>



(1) Unless the voltage on NRST pin go below  $V_{IL(NRST)}$  level, the device would not generate a reliable reset.

## 4.12. GPIO characteristics

Table 4-23. I/O port DC characteristics<sup>(1)(3)</sup>

| Symbol                | Parameter  | Conditions   | Min          | Typ  | Max          | Unit |
|-----------------------|--|--|--------------|------|--------------|------|
| $V_{IL}$              | Standard IO Low level input voltage                                  | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.3\text{ V}$ | —            | —    | $0.3 V_{DD}$ | V    |
|                       | 5V-tolerant IO Low level input voltage                               | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.3\text{ V}$ | —            | —    | $0.3 V_{DD}$ |      |
| $V_{IH}$              | Standard IO High level input voltage                                 | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.3\text{ V}$ | $0.7 V_{DD}$ | —    | —            | V    |
|                       | 5 V-tolerant IO High level input voltage                             | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.3\text{ V}$ | $0.7 V_{DD}$ | —    | —            |      |
| <b>IO_speed=50MHz</b> |  |  |              |      |              |      |
| $V_{OL}$              | Low level output voltage for an IO Pin ( $I_{IO} = +8\text{ mA}$ )   | $V_{DD} = 2.6\text{ V}$                                | —            | 0.24 | —            | V    |
|                       |  | $V_{DD} = 3.3\text{ V}$                                | —            | 0.21 | —            |      |
|                       |  | $V_{DD} = 3.6\text{ V}$                                | —            | 0.2  | —            |      |
|                       | Low level output voltage for an IO Pin ( $I_{IO} = +20\text{ mA}$ )  | $V_{DD} = 2.6\text{ V}$                                | —            | 0.66 | —            |      |
|                       |  | $V_{DD} = 3.3\text{ V}$                                | —            | 0.56 | —            |      |
|                       |  | $V_{DD} = 3.6\text{ V}$                                | —            | 0.54 | —            |      |
| $V_{OH}$              | High level output voltage for an IO Pin ( $I_{IO} = +8\text{ mA}$ )  | $V_{DD} = 2.6\text{ V}$                                | —            | 2.25 | —            | V    |
|                       |  | $V_{DD} = 3.3\text{ V}$                                | —            | 2.94 | —            |      |
|                       |  | $V_{DD} = 3.6\text{ V}$                                | —            | 3.23 | —            |      |
|                       | High level output voltage for an IO Pin ( $I_{IO} = +20\text{ mA}$ ) | $V_{DD} = 2.6\text{ V}$                                | —            | 2.16 | —            |      |
|                       |  | $V_{DD} = 3.3\text{ V}$                                | —            | 2.36 | —            |      |
|                       |  | $V_{DD} = 3.6\text{ V}$                                | —            | 2.83 | —            |      |
| <b>IO_speed=10MHz</b> |  |  |              |      |              |      |
| $V_{OL}$              | Low level output   | $V_{DD} = 2.6\text{ V}$                                | —            | 0.35 | —            | V    |

| Symbol                         | Parameter  | Conditions                       | Min  | Typ  | Max | Unit |
|--------------------------------|--|----------------------------------|------|------|-----|------|
|                                | voltage for an IO Pin<br>(I <sub>IO</sub> = +4 mA)                       | V <sub>DD</sub> = 3.3 V          |      | 0.29 |     | V    |
|                                |  | V <sub>DD</sub> = 3.6 V          | —    | 0.28 | —   |      |
|                                | Low level output<br>voltage for an IO Pin<br>(I <sub>IO</sub> = +10 mA)  | V <sub>DD</sub> = 3.3 V          | —    | 0.82 | —   |      |
|                                |  | V <sub>DD</sub> = 3.6 V          | —    | 0.76 | —   |      |
| V <sub>OH</sub>                | High level output<br>voltage for an IO Pin<br>(I <sub>IO</sub> = +4 mA)  | V <sub>DD</sub> = 2.6 V          | —    | 2.21 | —   | V    |
|                                |  | V <sub>DD</sub> = 3.3 V          | —    | 2.96 | —   |      |
|                                |  | V <sub>DD</sub> = 3.6 V          | —    | 3.28 | —   |      |
|                                | High level output<br>voltage for an IO Pin<br>(I <sub>IO</sub> = +10 mA) | V <sub>DD</sub> = 3.3 V          | —    | 2.49 | —   |      |
| V <sub>DD</sub> = 3.6 V        |  | —                                | 2.85 | —    |     |      |
| <b>IO_speed=2MHz</b>           |  |                                  |      |      |     |      |
| V <sub>OL</sub>                | Low level output<br>voltage for an IO Pin<br>(I <sub>IO</sub> = +4 mA)   | V <sub>DD</sub> = 2.6 V          | —    | 0.91 | —   | V    |
|                                |  | V <sub>DD</sub> = 3.3 V          | —    | 0.72 | —   |      |
|                                |  | V <sub>DD</sub> = 3.6 V          | —    | 0.69 | —   |      |
| V <sub>OH</sub>                | High level output<br>voltage for an IO Pin<br>(I <sub>IO</sub> = +4 mA)  | V <sub>DD</sub> = 2.6 V          | —    | 1.75 | —   | V    |
|                                |  | V <sub>DD</sub> = 3.3 V          |      | 2.70 |     |      |
|                                |  | V <sub>DD</sub> = 3.6 V          | —    | 3.04 | —   |      |
| R <sub>PU</sub> <sup>(2)</sup> | Internal pull-up<br>resistor   | V <sub>IN</sub> =V <sub>SS</sub> | —    | 40   | —   | kΩ   |
| R <sub>PD</sub> <sup>(2)</sup> | Internal pull-down<br>resistor   | V <sub>IN</sub> =V <sub>DD</sub> | —    | 40   | —   | kΩ   |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current (typical source capability:3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

**Table 4-24. I/O port AC characteristics<sup>(1)(2)(4)</sup>**

| GPIOx_OSPDy[1:0] bit value <sup>(3)</sup>     | Parameter                            | Conditions  | Typ  | Unit |
|---|--------------------------------------|---|------|------|
| GPIOx_OSPDy [1:0] = X0<br>(IO_Speed = 2 MHz)  | T <sub>Rise</sub> /T <sub>Fall</sub> | 2.6 ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 10 pF | 65.2 | ns   |
|   |                                      | 2.6 ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF | 55.4 |      |
|   |                                      | 2.6 ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 50 pF | 45   |      |
| GPIOx_OSPDy [1:0] = 01<br>(IO_Speed = 10 MHz) | T <sub>Rise</sub> /T <sub>Fall</sub> | 2.6 ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 10 pF | 18.4 | ns   |
|   |                                      | 2.6 ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF | 25.6 |      |
|   |                                      | 2.6 ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 50 pF | 30.4 |      |
| GPIOx_OSPDy [1:0] = 11<br>(IO_Speed = 50 MHz) | T <sub>Rise</sub> /T <sub>Fall</sub> | 2.6 ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 10 pF | 2.6  | ns   |
|   |                                      | 2.6 ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF | 3.4  |      |
|   |                                      | 2.6 ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 50 pF | 4.8  |      |

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all test results given for TA = 25 °C.

(3) The I/O speed is configured using the GPIOx\_CTL -> MDy[1:0] bits.

(4) Only for reference, Depending on user's design.

## 4.13. ADC characteristics

**Table 4-25. ADC characteristics**

|                                  |  |                                 |      |       |                  |                    |
|----------------------------------|--|---------------------------------|------|-------|------------------|--------------------|
| V <sub>DDA</sub> <sup>(1)</sup>  | Operating voltage                              | —                               | 2.6  | 3.3   | 3.6              | V                  |
| V <sub>IN</sub> <sup>(1)</sup>   | ADC input voltage range                        | 16 external; 3 internal         | 0    | —     | V <sub>DDA</sub> | V                  |
| f <sub>ADC</sub> <sup>(1)</sup>  | ADC clock                                      | —                               | 0.6  | —     | 14               | MHz                |
| f <sub>s</sub> <sup>(1)</sup>    | Sampling rate                                  | 12-bit                          | 0.04 | —     | 1                | MSPS               |
| R <sub>AIN</sub> <sup>(2)</sup>  | External input impedance                       | See <a href="#">Equation 1</a>  | —    | —     | 54.8             | kΩ                 |
| R <sub>ADC</sub> <sup>(2)</sup>  | Input sampling switch resistance               | —                               | —    | —     | 0.2              | kΩ                 |
| C <sub>ADC</sub> <sup>(2)</sup>  | Input sampling capacitance                     | No pin/pad capacitance included | —    | 32    | —                | pF                 |
| t <sub>CAL</sub> <sup>(2)</sup>  | Calibration time                               | f <sub>ADC</sub> = 14 MHz       | —    | 5.928 | —                | μs                 |
| t <sub>s</sub> <sup>(2)</sup>    | Sampling time                                  | f <sub>ADC</sub> = 14 MHz       | 0.11 | —     | 17.11            | μs                 |
| t <sub>CONV</sub> <sup>(2)</sup> | Total conversion time(including sampling time) | 12-bit                          | —    | 14    | —                | 1/f <sub>ADC</sub> |
| t <sub>SU</sub> <sup>(2)</sup>   | Startup time                                   | —                               | —    | —     | 1                | μs                 |
| V <sub>DDA</sub> <sup>(1)</sup>  | Operating voltage                              | —                               | 2.6  | 3.3   | 3.6              | V                  |
| V <sub>IN</sub> <sup>(1)</sup>   | ADC input voltage range                        | 16 external; 3 internal         | 0    | —     | V <sub>DDA</sub> | V                  |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

$$\text{Equation 1: } R_{AIN \text{ max formula}} \quad R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

**Table 4-26. ADC R<sub>AIN max</sub> for f<sub>ADC</sub>=14 MHz**

| T <sub>s</sub> (cycles) | t <sub>s</sub> (μs) | R <sub>AIN max</sub> (kΩ) |
|-------------------------|---------------------|---------------------------|
| 1.5                     | 0.11                | 0.14                      |
| 7.5                     | 0.54                | 1.5                       |
| 13.5                    | 0.96                | 2.9                       |
| 28.5                    | 2.04                | 6.3                       |
| 41.5                    | 2.96                | 9.3                       |
| 55.5                    | 3.96                | 12.5                      |
| 71.5                    | 5.11                | 16.2                      |
| 239.5                   | 17.11               | 54.8                      |

## 4.14. Temperature sensor characteristics

**Table 4-27. Temperature sensor characteristics<sup>(1)</sup>**

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
|--------|-----------|-----|-----|-----|------|

|                     |  |   |           |   |                        |
|---------------------|--|---|-----------|---|------------------------|
| $T_L$               | VSENSE linearity with temperature              | — | $\pm 1.5$ | — | $^{\circ}\text{C}$     |
| Avg_Slope           | Average slope                                  | — | 4.1       | — | mV/ $^{\circ}\text{C}$ |
| $V_{25}$            | Voltage at 25 $^{\circ}\text{C}$               | — | 1.45      | — | V                      |
| $t_{S\_temp}^{(2)}$ | ADC sampling time when reading the temperature | — | 17.1      | — | $\mu\text{s}$          |

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

## 4.15. I2C characteristics

**Table 4-28. I2C characteristics** <sup>(1) (2) (3)</sup>

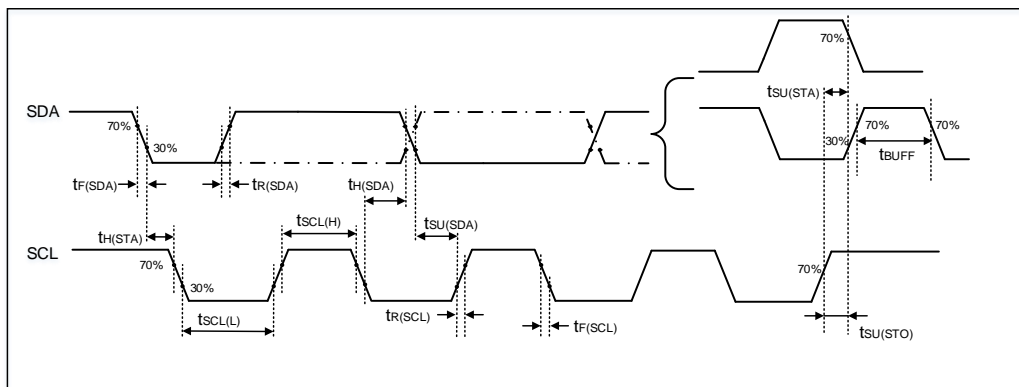
| Symbol         | Parameter                               | Conditions | Standard mode    |      | Fast mode |     | Unit          |
|----------------|---|------------|------------------|------|-----------|-----|---------------|
|                |   |            | Min              | Max  | Min       | Max |               |
| $t_{SCL(H)}$   | SCL clock high time                     | —          | 4.0              | —    | 0.6       | —   | $\mu\text{s}$ |
| $t_{SCL(L)}$   | SCL clock low time                      | —          | 4.7              | —    | 1.3       | —   | $\mu\text{s}$ |
| $t_{SU(SDA)}$  | SDA setup time                          | —          | 250              | —    | 100       | —   | ns            |
| $t_H(SDA)$     | SDA data hold time                      | —          | 0 <sup>(3)</sup> | 3450 | 0         | 900 | ns            |
| $t_R(SDA/SCL)$ | SDA and SCL rise time                   | —          | —                | 1000 | —         | 300 | ns            |
| $t_F(SDA/SCL)$ | SDA and SCL fall time                   | —          | —                | 300  | —         | 300 | ns            |
| $t_H(STA)$     | Start condition hold time               | —          | 4.0              | —    | 0.6       | —   | $\mu\text{s}$ |
| $t_{SU(STA)}$  | Repeated Start condition setup time     | —          | 4.7              | —    | 0.6       | —   | $\mu\text{s}$ |
| $t_{SU(STO)}$  | Stop condition setup time               | —          | 4.0              | —    | 0.6       | —   | $\mu\text{s}$ |
| $t_{BUFF}$     | Stop to Start condition time (bus free) | —          | 4.7              | —    | 1.3       | —   | $\mu\text{s}$ |

(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency,  $f_{PCLK1}$  must be at least 2 MHz. To ensure the fast mode I2C frequency,  $f_{PCLK1}$  must be at least 4 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

**Figure 4-5. I2C bus timing diagram**



## 4.16. USART characteristics

**Table 4-29. USART characteristics <sup>(1)</sup>**

| Symbol              | Parameter           | Conditions                  | Min   | Typ | Max | Unit |
|---------------------|---------------------|-----------------------------|-------|-----|-----|------|
| f <sub>SCK</sub>    | SCK clock frequency | f <sub>PCLKx</sub> = 48 MHz | —     | —   | 24  | MHz  |
| t <sub>SCK(H)</sub> | SCK clock high time | f <sub>PCLKx</sub> = 48MHz  | 20.83 | —   | —   | ns   |
| t <sub>SCK(L)</sub> | SCK clock low time  | f <sub>PCLKx</sub> = 48 MHz | 20.83 | —   | —   | ns   |

(1) Based on characterization, not tested in production.

## 4.17. TIMER characteristics

**Table 4-30. TIMER characteristics <sup>(1)</sup>**

| Symbol                 | Parameter   | Conditions                      | Min    | Max                       | Unit                   |
|------------------------|---|---------------------------------|--------|---------------------------|------------------------|
| t <sub>res</sub>       | Timer resolution time                                       | —                               | 1      | —                         | t <sub>TIMERxCLK</sub> |
|                        |   | f <sub>TIMERxCLK</sub> = 48 MHz | 20.8   | —                         | ns                     |
| f <sub>EXT</sub>       | Timer external clock frequency                              | —                               | 0      | f <sub>TIMERxCLK</sub> /2 | MHz                    |
|                        |   | f <sub>TIMERxCLK</sub> = 48 MHz | 0      | 24                        | MHz                    |
| RES                    | Timer resolution  | —                               | —      | 16                        | bit                    |
| t <sub>COUNTER</sub>   | 16-bit counter clock period when internal clock is selected | —                               | 1      | 65536                     | t <sub>TIMERxCLK</sub> |
|                        |   | f <sub>TIMERxCLK</sub> = 48 MHz | 0.0208 | 1365                      | μs                     |
| t <sub>MAX_COUNT</sub> | Maximum possible count                                      | —                               | —      | 65536 × 65536             | t <sub>TIMERxCLK</sub> |
|                        |   | f <sub>TIMERxCLK</sub> = 48 MHz | —      | 89.5                      | s                      |

(1) Guaranteed by design, not tested in production.

## 4.18. WDGT characteristics

**Table 4-31. FWDGT min/max timeout period at 40 kHz (IRC40K) <sup>(1)</sup>**

| Prescaler divider | PR[2:0] bits | Min timeout RLD[11:0] = 0x000 | Max timeout RLD[11:0] = 0xFFFF | Unit |
|-------------------|--------------|-------------------------------|--------------------------------|------|
| 1/4               | 000          | 0.025                         | 409.525                        | ms   |
| 1/8               | 001          | 0.025                         | 819.025                        |      |
| 1/16              | 010          | 0.025                         | 1638.025                       |      |
| 1/32              | 011          | 0.025                         | 3276.025                       |      |
| 1/64              | 100          | 0.025                         | 6552.025                       |      |
| 1/128             | 101          | 0.025                         | 13104.025                      |      |
| 1/256             | 110 or 111   | 0.025                         | 26208.025                      |      |

(1) Guaranteed by design, not tested in production.

**Table 4-32. WWDGT min-max timeout value at 48 MHz ( $f_{PCLK1}$ )<sup>(1)</sup>**

| Prescaler divider | PSC[1:0] | Min timeout value<br>CNT[6:0] = 0x40 | Unit | Max timeout value<br>CNT[6:0] = 0x7F | Unit |
|-------------------|----------|--------------------------------------|------|--------------------------------------|------|
| 1/1               | 00       | 85.33                                | μs   | 5.46                                 | ms   |
| 1/2               | 01       | 170.67                               |      | 10.92                                |      |
| 1/4               | 10       | 341.33                               |      | 21.85                                |      |
| 1/8               | 11       | 682.67                               |      | 43.69                                |      |

(1) Guaranteed by design, not tested in production.

## 4.19. Parameter conditions

Unless otherwise specified, all values given for  $V_{DD} = V_{DDA} = 3.3\text{ V}$ ,  $T_A = 25\text{ °C}$ .

## 5. Package information

### 5.1. LQFP64 package outline dimensions

Figure 5-1. LQFP64 package outline

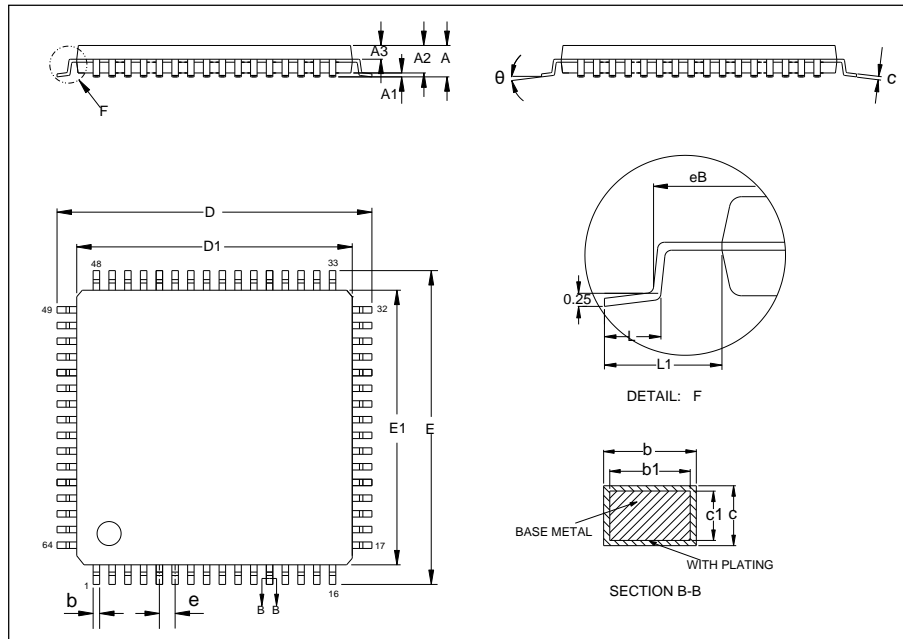


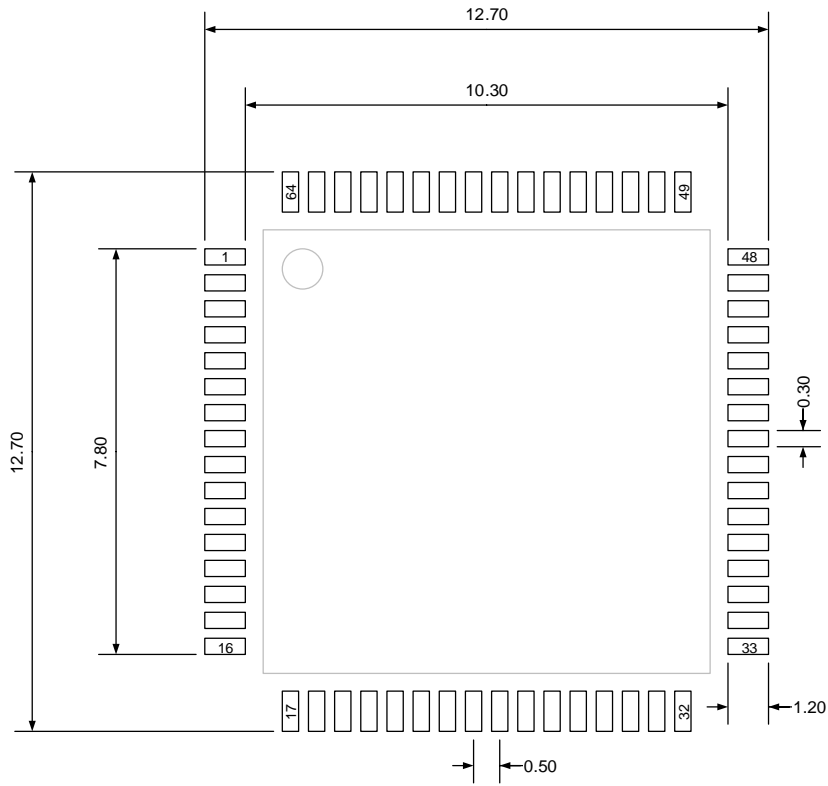
Table 5-1. LQFP64 package dimensions

| Symbol   | Min   | Typ   | Max   |
|----------|-------|-------|-------|
| A        | —     | —     | 1.60  |
| A1       | 0.05  | —     | 0.15  |
| A2       | 1.35  | 1.40  | 1.45  |
| A3       | 0.59  | 0.64  | 0.69  |
| b        | 0.18  | —     | 0.26  |
| b1       | 0.17  | 0.20  | 0.23  |
| c        | 0.13  | —     | 0.17  |
| c1       | 0.12  | 0.13  | 0.14  |
| D        | 11.80 | 12.00 | 12.20 |
| D1       | 9.90  | 10.00 | 10.10 |
| E        | 11.80 | 12.00 | 12.20 |
| E1       | 9.90  | 10.00 | 10.10 |
| e        | —     | 0.50  | —     |
| eB       | 11.25 | —     | 11.45 |
| L        | 0.45  | —     | 0.75  |
| L1       | —     | 1.00  | —     |
| $\theta$ | 0°    | —     | 7°    |



(Original dimensions are in millimeters)

Figure 5-2. LQFP64 recommended footprint



(Original dimensions are in millimeters)

## 5.2. LQFP48 package outline dimensions

Figure 5-3. LQFP48 package outline

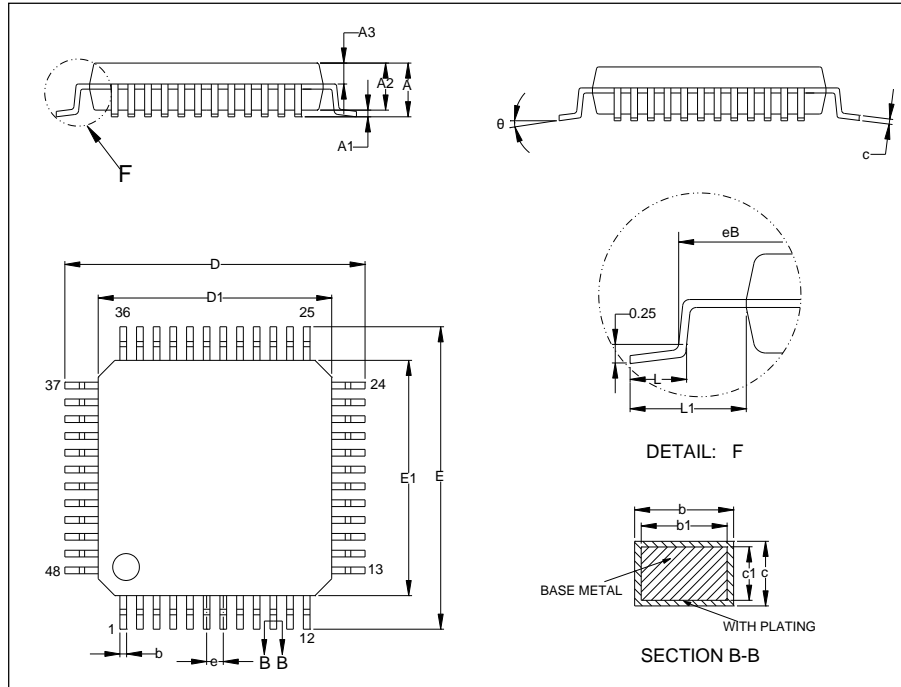
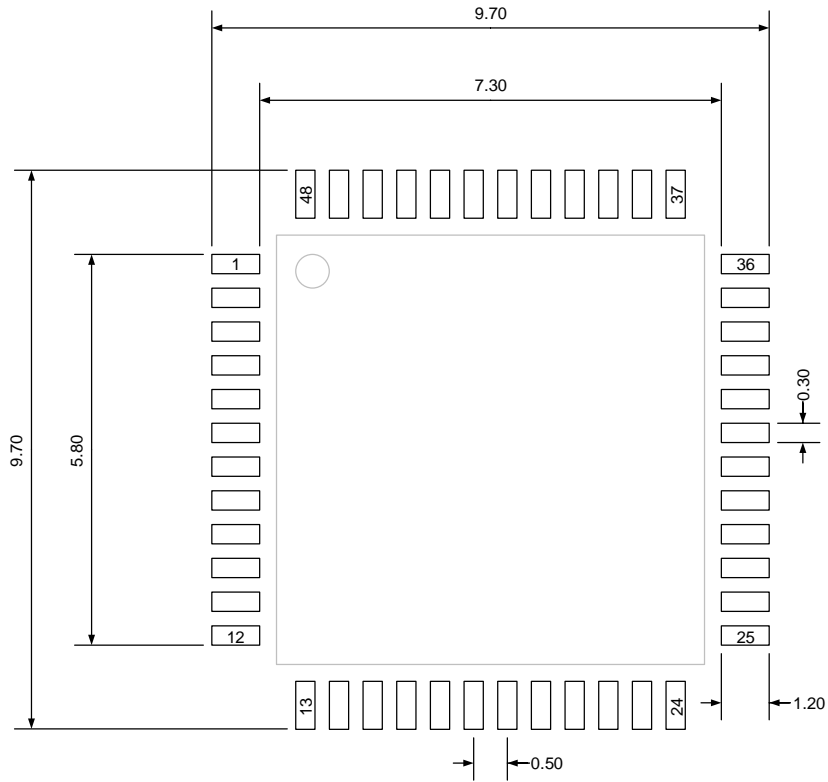


Table 5-2. LQFP48 package dimensions

| Symbol   | Min  | Typ  | Max  |
|----------|------|------|------|
| A        | —    | —    | 1.60 |
| A1       | 0.05 | —    | 0.15 |
| A2       | 1.35 | 1.40 | 1.45 |
| A3       | 0.59 | 0.64 | 0.69 |
| b        | 0.18 | —    | 0.26 |
| b1       | 0.17 | 0.20 | 0.23 |
| c        | 0.13 | —    | 0.17 |
| c1       | 0.12 | 0.13 | 0.14 |
| D        | 8.80 | 9.00 | 9.20 |
| D1       | 6.90 | 7.00 | 7.10 |
| E        | 8.80 | 9.00 | 9.20 |
| E1       | 6.90 | 7.00 | 7.10 |
| e        | —    | 0.50 | —    |
| eB       | 8.10 | —    | 8.25 |
| L        | 0.45 | —    | 0.75 |
| L1       | —    | 1.00 | —    |
| $\theta$ | 0°   | —    | 7°   |

(Original dimensions are in millimeters)

Figure 5-4. LQFP48 recommended footprint



(Original dimensions are in millimeters)

### 5.3. LQFP32 package outline dimensions

Figure 5-5. LQFP32 package outline

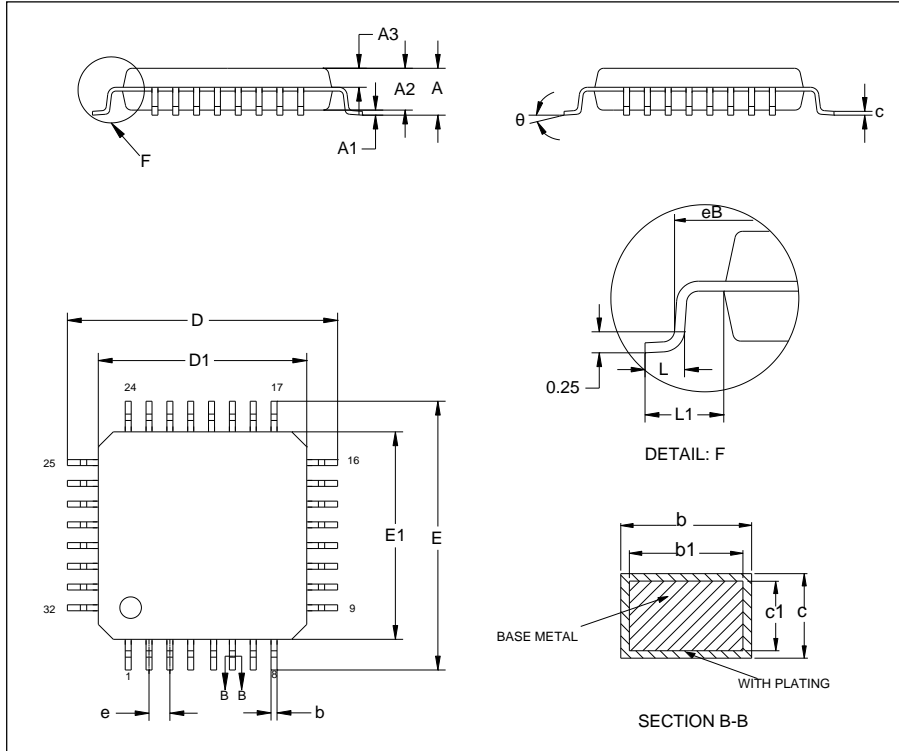
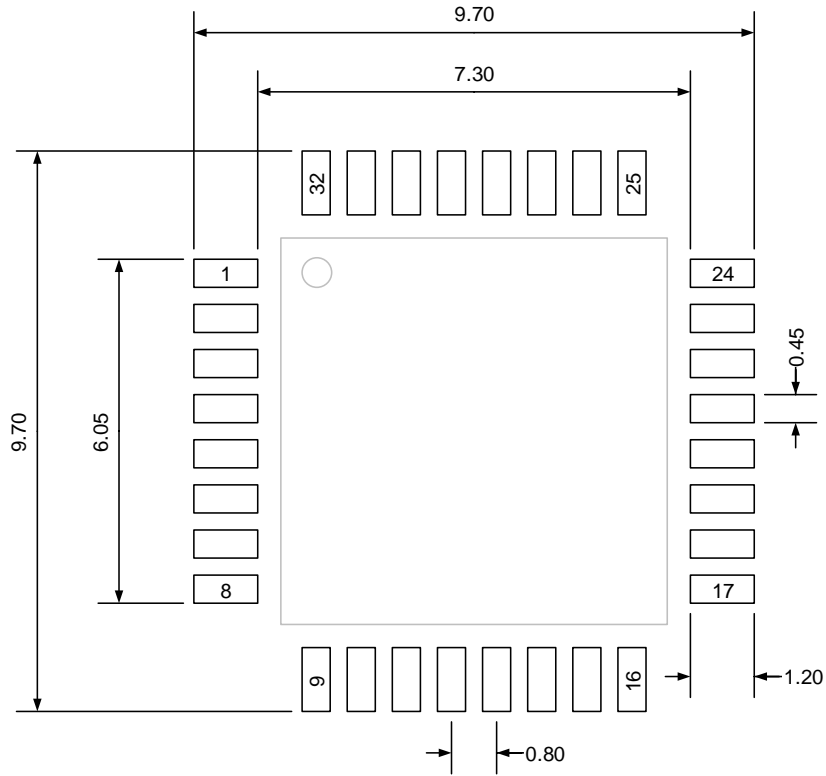


Table 5-3. LQFP32 package dimensions

| Symbol | Min  | Typ  | Max  |
|--------|------|------|------|
| A      | —    | —    | 1.60 |
| A1     | 0.05 | —    | 0.15 |
| A2     | 1.35 | 1.40 | 1.45 |
| A3     | 0.59 | 0.64 | 0.69 |
| b      | 0.33 | —    | 0.41 |
| b1     | 0.32 | 0.35 | 0.38 |
| c      | 0.13 | —    | 0.17 |
| c1     | 0.12 | 0.13 | 0.14 |
| D      | 8.80 | 9.00 | 9.20 |
| D1     | 6.90 | 7.00 | 7.10 |
| E      | 8.80 | 9.00 | 9.20 |
| E1     | 6.90 | 7.00 | 7.10 |
| e      | —    | 0.80 | —    |
| eB     | 8.10 | —    | 8.25 |
| L      | 0.45 | —    | 0.75 |
| L1     | —    | 1.00 | —    |
| θ      | 0°   | —    | 7°   |

(Original dimensions are in millimeters)

**Figure 5-6. LQFP32 recommended footprint**



(Original dimensions are in millimeters)

## 5.4. QFN32 package outline dimensions

Figure 5-7. QFN32 package outline

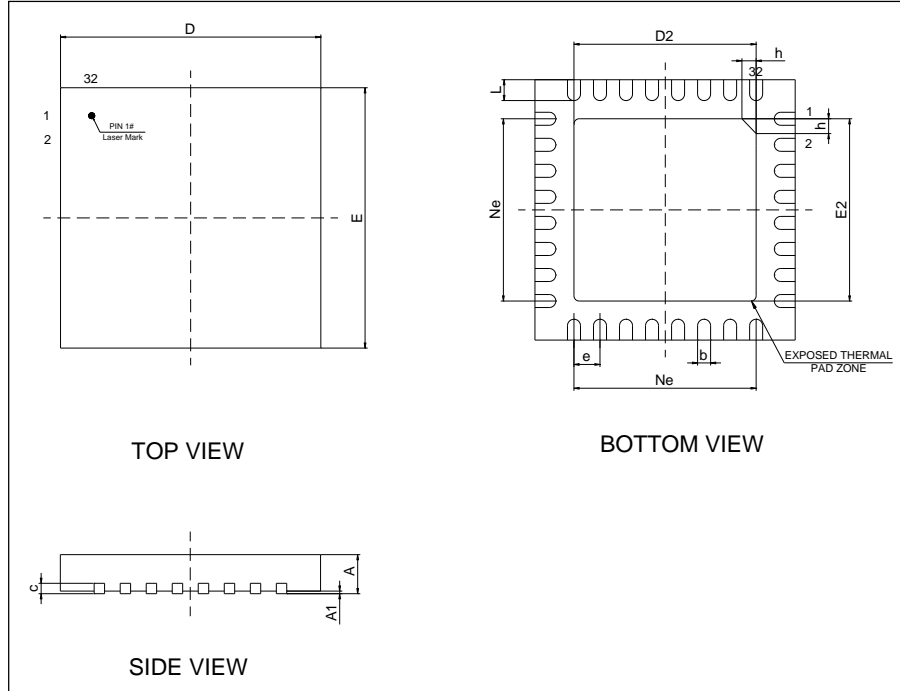
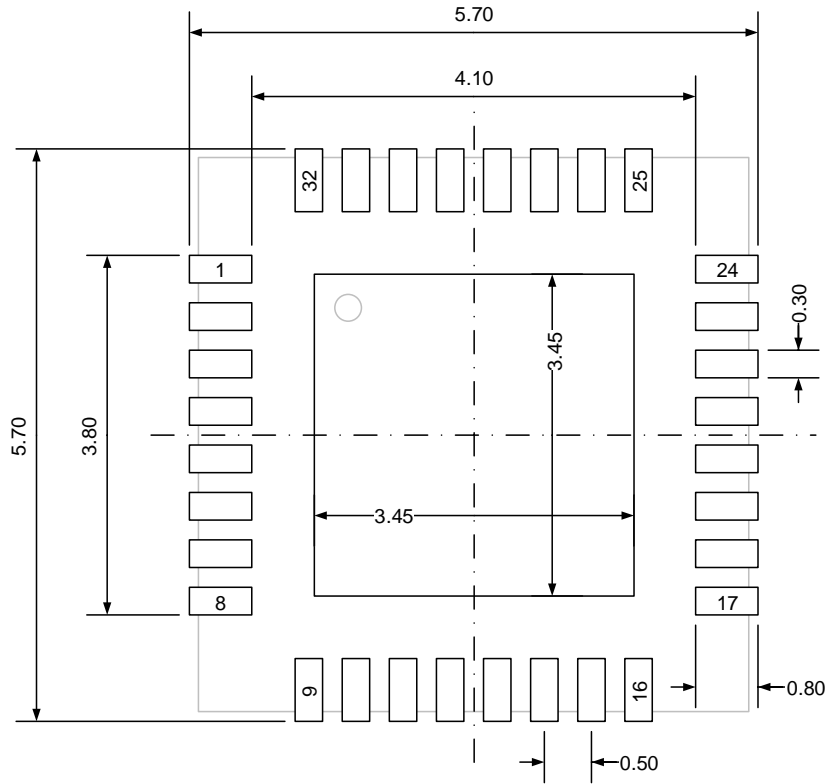


Table 5-4. QFN32 package dimensions

| Symbol | Min  | Typ  | Max  |
|--------|------|------|------|
| A      | 0.70 | 0.75 | 0.80 |
| A1     | 0    | 0.02 | 0.05 |
| b      | 0.18 | 0.25 | 0.30 |
| c      | 0.18 | 0.20 | 0.25 |
| D      | 4.90 | 5.00 | 5.10 |
| D2     | 3.40 | 3.50 | 3.60 |
| E      | 4.90 | 5.00 | 5.10 |
| E2     | 3.40 | 3.50 | 3.60 |
| e      | —    | 0.50 | —    |
| h      | 0.30 | 0.35 | 0.40 |
| L      | 0.35 | 0.40 | 0.45 |
| Ne     | —    | 3.50 | —    |

(Original dimensions are in millimeters)

Figure 5-8. QFN32 recommended footprint



(Original dimensions are in millimeters)

## 5.5. QFN28 package outline dimensions

Figure 5-9. QFN28 package outline

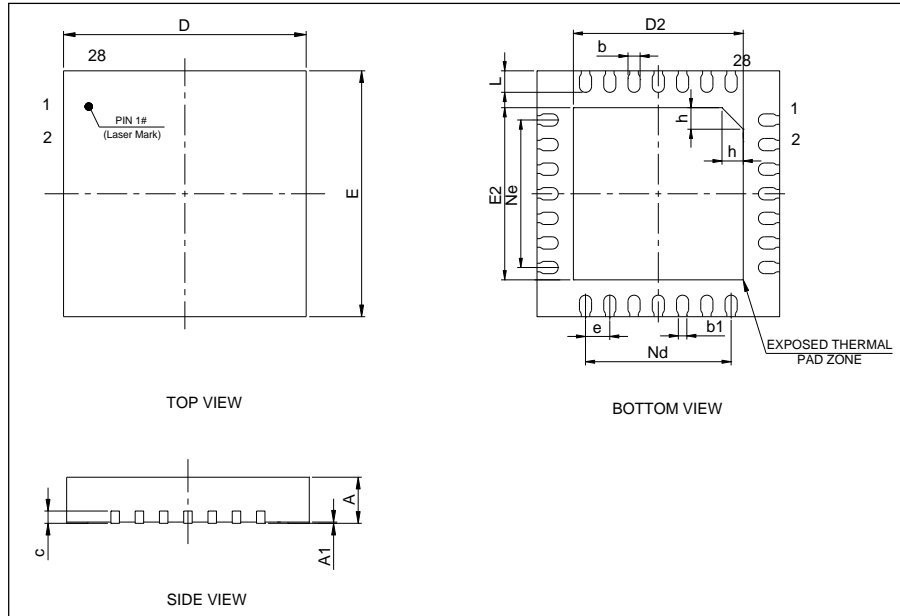


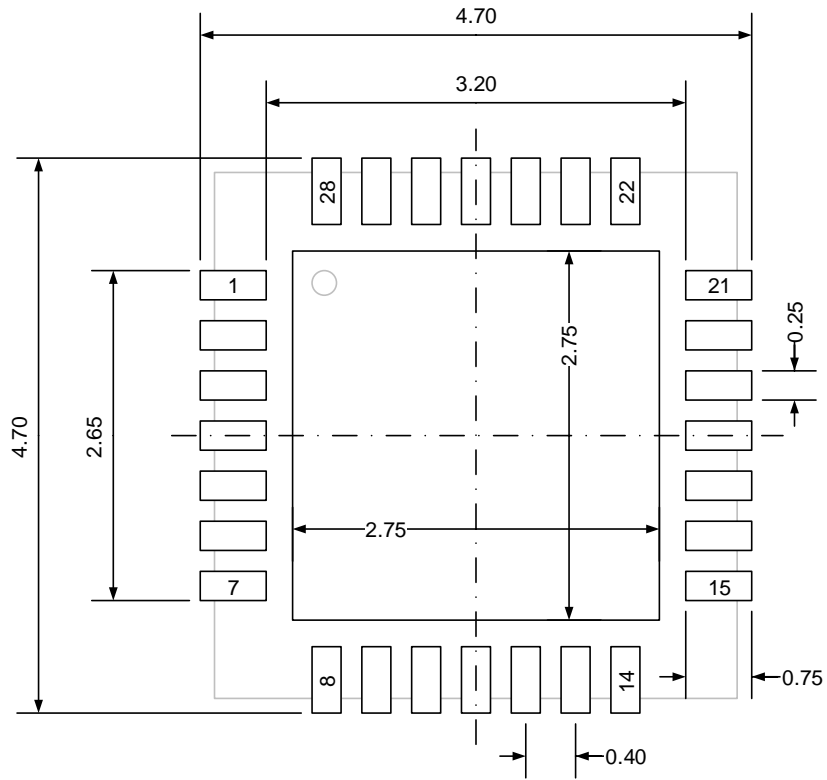
Table 5-5. QFN28 package dimensions

| Symbol | Min  | Typ  | Max  |
|--------|------|------|------|
| A      | 0.70 | 0.75 | 0.80 |
| A1     | 0    | 0.02 | 0.05 |
| b      | 0.15 | 0.20 | 0.25 |
| b1     | —    | 0.14 | —    |
| c      | 0.18 | 0.20 | 0.25 |
| D      | 3.90 | 4.00 | 4.10 |
| D2     | 2.70 | 2.80 | 2.90 |
| E      | 3.90 | 4.00 | 4.10 |
| E2     | 2.70 | 2.80 | 2.90 |
| e      | —    | 0.40 | —    |
| h      | 0.30 | 0.35 | 0.40 |
| L      | 0.30 | 0.35 | 0.40 |
| Nd     | —    | 2.40 | —    |
| Ne     | —    | 2.40 | —    |

(Original dimensions are in millimeters)



Figure 5-10. QFN28 recommended footprint



(Original dimensions are in millimeters)

## 5.6. TSSOP20 package outline dimensions

Figure 5-11. TSSOP20 package outline

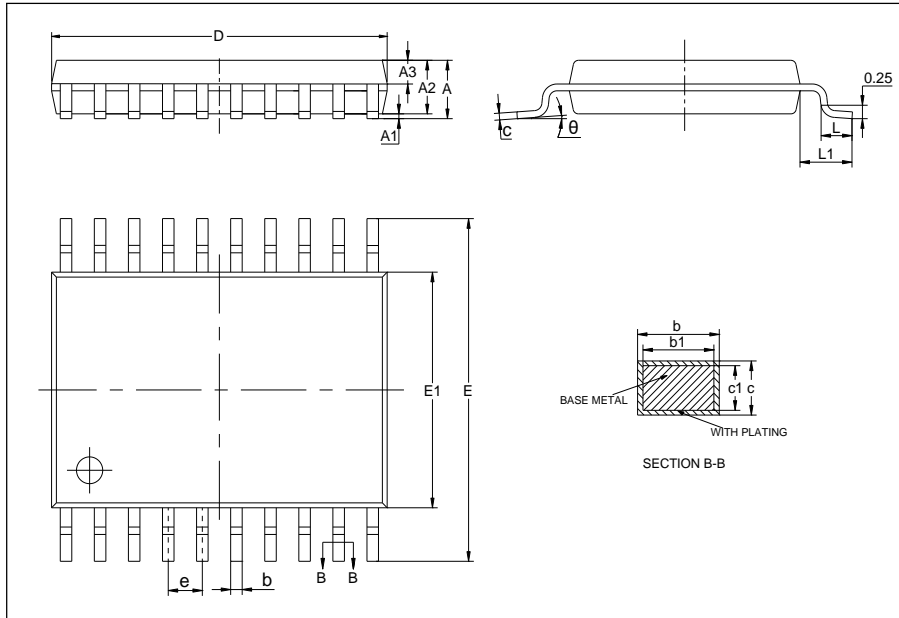
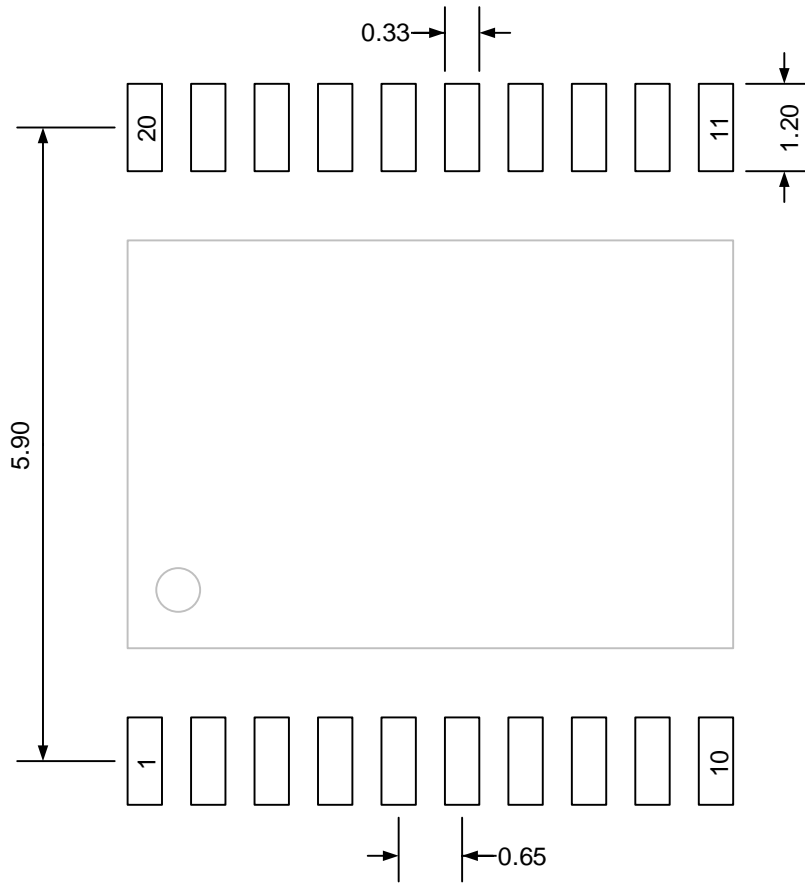


Table 5-6. TSSOP20 package dimensions

| Symbol   | Min  | Typ  | Max  |
|----------|------|------|------|
| A        | —    | —    | 1.20 |
| A1       | 0.05 | —    | 0.15 |
| A2       | 0.80 | 1.00 | 1.05 |
| A3       | 0.39 | 0.44 | 0.49 |
| b        | 0.20 | —    | 0.28 |
| b1       | 0.19 | 0.22 | 0.25 |
| c        | 0.13 | —    | 0.17 |
| c1       | 0.12 | 0.13 | 0.14 |
| D        | 6.40 | 6.50 | 6.60 |
| E        | 6.20 | 6.40 | 6.60 |
| E1       | 4.30 | 4.40 | 4.50 |
| e        | —    | 0.65 | —    |
| L        | 0.45 | 0.60 | 0.75 |
| L1       | —    | 1.00 | —    |
| $\theta$ | 0°   | —    | 8°   |

(Original dimensions are in millimeters)

Figure 5-12. TSSOP20 recommended footprint



(Original dimensions are in millimeters)

## 5.7. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “ $\theta$ ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

$\theta_{JA}$ : Thermal resistance, junction-to-ambient.

$\theta_{JB}$ : Thermal resistance, junction-to-board.

$\theta_{JC}$ : Thermal resistance, junction-to-case.

$\Psi_{JB}$ : Thermal characterization parameter, junction-to-board.

$\Psi_{JT}$ : Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5-1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5-2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5-3)$$

Where,  $T_J$  = Junction temperature.

$T_A$  = Ambient temperature

$T_B$  = Board temperature

$T_C$  = Case temperature which is monitoring on package surface

$P_D$  = Total power dissipation

$\theta_{JA}$  represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower  $\theta_{JA}$  can be considerate as better overall thermal performance.  $\theta_{JA}$  is generally used to estimate junction temperature.

$\theta_{JB}$  is used to measure the heat flow resistance between the chip surface and the PCB board.

$\theta_{JC}$  represents the thermal resistance between the chip surface and the package top case.  $\theta_{JC}$  is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

**Table 5-7. Package thermal characteristics<sup>(1)</sup>**

| Symbol        | Condition                    | Package | Value | Unit |
|---------------|------------------------------|---------|-------|------|
| $\theta_{JA}$ | Natural convection, 2S2P PCB | LQFP64  | 63.57 | °C/W |
|               |                              | LQFP48  | 64.40 |      |
|               |                              | LQFP32  | 66.11 |      |
|               |                              | QFN32   | 48.50 |      |
|               |                              | QFN28   | 66.07 |      |
|               |                              | TSSOP20 | 83.01 |      |
| $\theta_{JB}$ | Cold plate, 2S2P PCB         | LQFP64  | 44.40 | °C/W |

| Symbol        | Condition                    | Package | Value | Unit |
|---------------|------------------------------|---------|-------|------|
|               |                              | LQFP48  | 42.32 |      |
|               |                              | LQFP32  | 42.66 |      |
|               |                              | QFN32   | 28.32 |      |
|               |                              | QFN28   | 32.52 |      |
|               |                              | TSSOP20 | —     |      |
| $\theta_{JC}$ | Cold plate, 2S2P PCB         | LQFP64  | 21.98 | °C/W |
|               |                              | LQFP48  | 22.47 |      |
|               |                              | LQFP32  | 30.06 |      |
|               |                              | QFN32   | 24.07 |      |
|               |                              | QFN28   | 30.58 |      |
|               |                              | TSSOP20 | 22.92 |      |
| $\psi_{JB}$   | Natural convection, 2S2P PCB | LQFP64  | 44.64 | °C/W |
|               |                              | LQFP48  | 42.42 |      |
|               |                              | LQFP32  | 43.18 |      |
|               |                              | QFN32   | 28.93 |      |
|               |                              | QFN28   | 32.55 |      |
|               |                              | TSSOP20 | —     |      |
| $\psi_{JT}$   | Natural convection, 2S2P PCB | LQFP64  | 1.51  | °C/W |
|               |                              | LQFP48  | 1.74  |      |
|               |                              | LQFP32  | 4.56  |      |
|               |                              | QFN32   | 3.33  |      |
|               |                              | QFN28   | 3.27  |      |
|               |                              | TSSOP20 | —     |      |

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

## 6. Ordering information

**Table 6-1. Part ordering code for GD32F130xx devices**

| Ordering code  | Flash (KB) | Package | Package type | Temperature operating range  |
|----------------|------------|---------|--------------|------------------------------|
| GD32F130R8T6   | 64         | LQFP64  | Green        | Industrial<br>-40°C to +85°C |
| GD32F130C8T6   | 64         | LQFP48  | Green        | Industrial<br>-40°C to +85°C |
| GD32F130C6T6   | 32         | LQFP48  | Green        | Industrial<br>-40°C to +85°C |
| GD32F130C4T6   | 16         | LQFP48  | Green        | Industrial<br>-40°C to +85°C |
| GD32F130K8T6   | 64         | LQFP32  | Green        | Industrial<br>-40°C to +85°C |
| GD32F130K6T6   | 32         | LQFP32  | Green        | Industrial<br>-40°C to +85°C |
| GD32F130K4T6   | 16         | LQFP32  | Green        | Industrial<br>-40°C to +85°C |
| GD32F130K8U6   | 64         | QFN32   | Green        | Industrial<br>-40°C to +85°C |
| GD32F130K6U6   | 32         | QFN32   | Green        | Industrial<br>-40°C to +85°C |
| GD32F130K4U6   | 16         | QFN32   | Green        | Industrial<br>-40°C to +85°C |
| GD32F130G8U6TR | 64         | QFN28   | Green        | Industrial<br>-40°C to +85°C |
| GD32F130G6U6TR | 32         | QFN28   | Green        | Industrial<br>-40°C to +85°C |
| GD32F130G4U6TR | 16         | QFN28   | Green        | Industrial<br>-40°C to +85°C |
| GD32F130F8P6TR | 64         | TSSOP20 | Green        | Industrial<br>-40°C to +85°C |
| GD32F130F6P6TR | 32         | TSSOP20 | Green        | Industrial<br>-40°C to +85°C |
| GD32F130F4P6TR | 16         | TSSOP20 | Green        | Industrial<br>-40°C to +85°C |

## 7. Revision history

**Table 7-1. Revision history**

| Revision No. | Description   | Date          |
|--------------|---|---------------|
| 1.0          | 1. Initial Release.   | Mar.8, 2014   |
| 1.1          | 1. Characteristics values updated in <b><u>Table 4-3. Power consumption characteristics.</u></b>  | Oct.20, 2014  |
| 2.0          | 1. Characteristics of QFN32 package added in <b><u>Table 2-3. GD32F130R8 LQFP64 pin definitions</u></b> and <b><u>Table 5-2. QFN package dimensions.</u></b>  | Jan 15, 2015  |
| 2.1          | 1. Characteristics of TSSOP20 package added in <b><u>Table 2-1. GD32F130xx devices features and peripheral list.</u></b>  | Apr 24, 2016  |
| 3.0          | 1. Adapt To New Name Convention.  | Jan.24, 2018  |
| 3.1          | 1. Add LQFP32 Package.  | Apr.24, 2018  |
| 3.2          | 1. Modify 72MHz system frequency to 42MHz.  | Jul.25, 2019  |
| 3.3          | 1. Modify formats and descriptions.   | Nov.21, 2019  |
| 3.4          | 1. Update <b><u>Table 2-1. GD32F130xx devices features and peripheral list</u></b> and <b><u>Figure 2-4. GD32F130Kx LQFP32 pinouts.</u></b><br>2. Update <b><u>Table 4-3. Power consumption characteristics.</u></b>  | Jun.16.2021   |
| 3.5          | 1. Update <b><u>Table 4-1. Absolute maximum ratings<sup>(1)(4).</sup></u></b><br>2. Modify USART maximum communication speed from 9M to 6M.<br>3. Update electrical parameters in chapter <b><u>Electrical characteristics.</u></b>   | Jul. 12. 2022 |
| 3.6          | 1. Add notes for <b><u>Table 4-2. DC operating conditions</u></b> and <b><u>Table 4-7. Power consumption characteristics<sup>(2)(3)(4)(5)(6)</sup></u></b> , and update <b><u>Table 4-7. Power consumption characteristics<sup>(2)(3)(4)(5)(6)</sup></u></b> .<br>2. Update <b><u>Figure 4-5. I2C bus timing diagram.</u></b> | Sep. 27, 2022 |
| 3.7          | 1. Add the TR suffix after the Ordering information TSSOP20, QFN28  | Mar. 13, 2023 |
| 3.8          | 1. Add notes :more details refer to AN108 GD32F3x0 Hardware Development Guide.<br>2. Add the pin definitions format requires that a new line be added to the pin definitions  | Jun15. 2023   |
| 3.9          | 1. Add specific ability description to backup domain IO driver current<br>2. Convert all encapsulated POD plots to vector plots   | Dec.31, 2023  |

## Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the "Product"), is owned by the Company under the intellectual property laws and treaties of the People's Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as its suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products.

Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and Products and services described herein at any time, without notice.