

GigaDevice Semiconductor Inc.

GD32VW553-MD1

Wi-Fi Single Band 1x1 802.11b/g/n/ax + BLE 5.2

IoT Combo Module

Datasheet

Revision 1.0

(DEC. 2024)

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1. General Features

- Built-in QFN40 GD32VW553 chip, RISC-V 32-bit processor up to 160 MHz
- Built-in 4096 KB on-chip Flash memory and 320KB (288 KB + 32KB Shared) SRAM memory
- 802.11b/g/n/ax compatible
- 802.11i (WPA, WPA2, WPA3). Open, shared key, and pair-wise key authentication services
- Single antenna 1x1 stream in 20MHz channels
- Support of 802.11ax MCS up to MCS9 with a Max PHY rate of 114.7Mbps
- Bluetooth LE 5.2
- Support of BLE High-Speed 2M PHY and Long-Range modes (125 kbps, 500 kbps).
- Peripheral interfaces: 28 GPIOs, support of ADC, PWM, UART, I2C, SPI, QSPI
- Onboard PCB antenna for GD32VW553-MD1-IMHx, and external IPEX connector for the GD32VW553-MD1-EMHx
- Operating voltage: 3.0V ~ 3.6V
- Operating temperature: -40 ~ 85°C for grade 6 and -40 ~ 105°C for grade 7

2. General description

The GD32VW553-MD1 series modules are highly integrated 2.4GHz Wi-Fi and BLE modules, they are optimized modules designed for a broad array of smart devices for Internet of Things (IoT) applications especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike, optical module and so on.

The GD32VW553-MD1 series modules are currently available in four types, based on different antenna type and operating temperature.

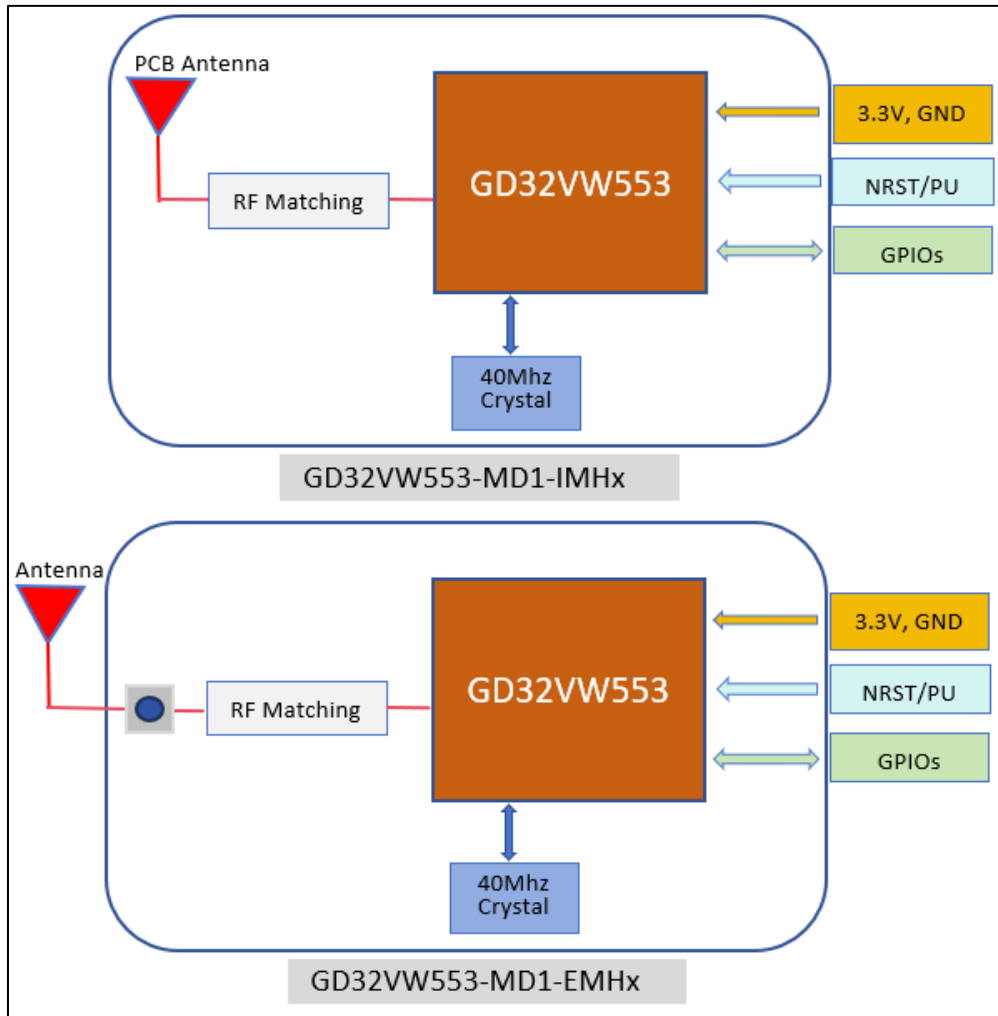
Table 2-1. Description of module types

Module Part Number	Flash	Operating Temperature	Antenna Type	Module Size(mm)
GD32VW553-MD1-IMH6	4MB	-40 ~ 85°C	Onboard	20 x 18 x 2.4
GD32VW553-MD1-IMH7		-40 ~ 105°C	Onboard	
GD32VW553-MD1-EMH6		-40 ~ 85°C	External	
GD32VW553-MD1-EMH7		-40 ~ 105°C	External	

3. Block diagram

An onboard PCB antenna is used for GD32VW553-MD1-IMHx, while an external antenna with an IPEX connector is used for GD32VW553-MD1-EMHx.

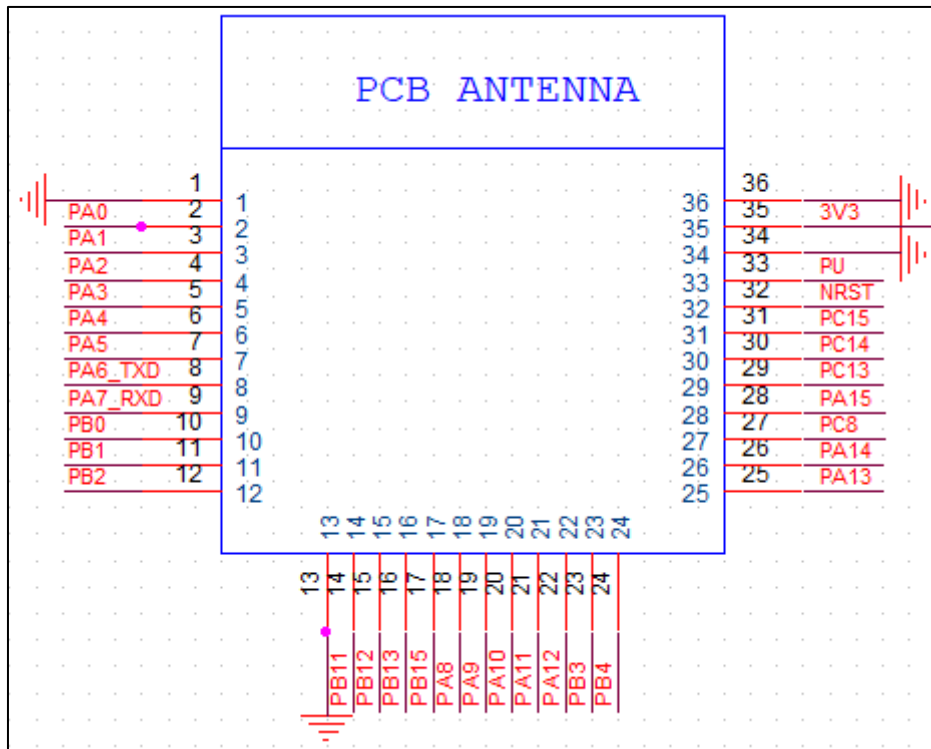
Figure 3-1. Block diagram



4. Pin definition

4.1. Pinouts

Figure 4-1. Pinouts from top view



4.2. Pin definitions

Table 4-1. Pin definitions

NO.	Name	Type	Function Description
1	GND	P	GND
2	PA0	I/O	Default: PA0 Alternate: USART0_TX, TIMER1_CH0, TIMER1_ETI, SPI_MOSI, UART1_CTS, TIMER0_ETI, EVENTOUT Additional: ADC_IN0, WAKEUP0, RTC_TAMP1
3	PA1	I/O	Default: PA1 Alternate: USART0_RX, TIMER1_CH1, SPI_MISO, UART1_RTS, EVENTOUT Additional: ADC_IN1
4	PA2	I/O	Default: PA2 Alternate: USART0_CTS, TIMER1_CH2, I2C0_SCL, SPI_SCK,

			TIMER0_CH0, UART1_TX, EVENTOUT Additional: ADC_IN2
5	PA3	I/O	Default: PA3 Alternate: USART0_RTS, TIMER1_CH3, I2C0_SDA, SPI_NSS, TIMER0_CH0_ON, UART1_RX, RTC_OUT, EVENTOUT Additional: ADC_IN3
6	PA4	I/O	Default: PA4 Alternate: UART1_TX, SPI_MOSI, QSPI_SCK, SPI_NSS, TIMER0_CH1, EVENTOUT Additional: ADC_IN4
7	PA5	I/O	Default: PA5 Alternate: UART1_RX, TIMER2_ETI, QSPI_CSN, SPI_MISO, SPI_SCK, TIMER0_CH1_ON, EVENTOUT Additional: ADC_IN5
8	PA6_TXD	I/O	Default: UART2_TX Alternate: TIMER2_CH0, QSPI_IO0, I2C1_SCL, SPI_MISO, SPI_SCK, TIMER0_CH1, TIMER1_CH1, EVENTOUT Additional: ADC_IN6
9	PA7_RXD	I/O	Default: UART2_RX Alternate: I2C1_SDA, TIMER0_CH0_ON, TIMER2_CH1, QSPI_IO1, SPI_NSS, SPI_MOSI, TIMER0_CH1_ON, TIMER1_CH2, EVENTOUT Additional: ADC_IN7, WAKUP2
10	PB0	I/O	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER0_CH0, TIMER0_CH2, UART1_TX, I2C0_SCL, TIMER2_ETI, TIMER16_CH0, UART2_CTS, TIMER0_BRKIN, EVENTOUT Additional: ADC_IN8
11	PB1	I/O	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER0_CH0_ON, TIMER2_CH2, UART1_RX, I2C0_SDA, TIMER16_CH0_ON, UART2_RTS, EVENTOUT Additional: BOOT1
12	PB2	I/O	Default: PB2 Alternate: TIMER1_CH3, TIMER2_CH3, UART1_CTS, TIMER0_ETI, TIMER16_BRKIN, EVENTOUT
13	GND	P	GND
14	PB11	I/O	Default: PB11 Alternate: CK_OUT1, TIMER1_CH2, TIMER0_CH1_ON, UART1_RTS, TIMER15_BRKIN, EVENTOUT
15	PB12	I/O	Default: PB12 Alternate: TIMER0_BRKIN, TIMER0_CH3, TIMER1_CH2, I2C1_SCL, EVENTOUT
16	PB13	I/O	Default: PB13 Alternate: TIMER0_CH0_ON, TIMER1_CH3, I2C1_SDA, TIMER15_CH0, EVENTOUT

17	PB15	I/O	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER2_CH0, I2C0_SCL, I2C1_SCL, UART1_TX, USART0_TX, IFRP_OUT, EVENTOUT
18	PA8	I/O	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, USART0_RX, UART1_RX, I2C0_SDA, I2C1_SDA, USART0_CK, TIMER15_CH0, RTC_OUT, TIMER0_CH2_ON, EVENTOUT
19	PA9	I/O	Default: PA9 Alternate: SPI_MOSI, TIMER0_CH1, QSPI_SCK, USART0_TX, TIMER15_CH0_ON, EVENTOUT
20	PA10	I/O	Default: PA10 Alternate: SPI_MISO, TIMER0_CH2, QSPI_CSN, TIMER16_CH0, USART0_RX, EVENTOUT
21	PA11	I/O	Default: PA11 Alternate: SPI_SCK, TIMER0_CH3, QSPI_IO0, TIMER16_BRKIN, TIMER1_CH3, EVENTOUT
22	PA12	I/O	Default: PA12 Alternate: TIMER0_ETI, TIMER0_CH3, QSPI_IO1, SPI_NSS, USART0_CK, TIMER1_CH2, TIMER16_CH0_ON, EVENTOUT Additional: WKUP3
23	PB3	I/O	Default: JTDO, PB3 Alternate: TIMER1_CH1, QSPI_IO2, USART0_RX, UART1_RX, TIMER15_BRKIN, EVENTOUT
24	PB4	I/O	Default: NJTRST, PB4 Alternate: TIMER1_CH0, TIMER1_ETI, QSPI_IO3, USART0_TX, UART1_TX, EVENTOUT
25	PA13	I/O	Default: JTMS, PA13 Alternate: I2C0_SMBA, I2C1_SCL, USART0_CTS, UART1_CTS, EVENTOUT
26	PA14	I/O	Default: JTCK, PA14 Alternate: I2C1_SMBA, I2C1_SDA, USART0_RTS, UART1_RTS, EVENTOUT
27	PC8	I/O	Default: PC8 Alternate: TIMER2_CH2, I2C0_SDA, I2C1_SDA, USART0_TX, UART1_TX, EVENTOUT Additional: BOOT0
28	PA15	I/O	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, I2C0_SCL, I2C1_SCL, USART0_RX, UART1_RX, EVENTOUT Additional: WKUP1
29	PC13	I/O	Default: PC13

			Alternate: USART0_CK, EVENTOUT Additional: RTC_TAMP_0, RTC_OUT, RTC_TS
30	PC14	I/O	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
31	PC15	I/O	Default: PC15 Alternate: IFRP_OUT, EVENTOUT Additional: OSC32OUT
32	NRST	I	Default: NRST
33	PU	I	Default: PU
34	GND	P	GND
35	3V3	P	3.3V(+/-0.3)
36	GND	P	GND

5. Wireless radio characteristics

5.1. Wi-Fi characteristics

Table 5-1. Wi-Fi characteristics

Features	Description		
WLAN Standard	IEEE 802.11 b/g/n/ax		
Range of frequency	2412 MHz ~ 2484 MHz		
channels	2.4GHz: Channel 1 ~ 14		
Transmitter characteristics	Rate	Typical value	Unit
Output Power (Pass 802.11 Mask & EVM spec.)	802.11b /1Mbps	23.9	dBm
	802.11b /11Mbps	23.9	
	802.11g /6Mbps	22.5	
	802.11g /54Mbps	19.3	
	802.11n, HT20 /MCS0	21.1	
	802.11n, HT20 /MCS7	18.6	
	802.11ax, HE20 /MCS0	21.3	
	802.11ax, HE20 /MCS9	16.4	
Receiver characteristics	Rate	Typical value	Unit
Sensitivity (Pass 802.11 PER spec.)	802.11b /1Mbps	-99.3	dBm
	802.11b /11Mbps	-91.1	
	802.11g /6Mbps	-94.7	
	802.11g /54Mbps	-78.3	
	802.11n, HT20 /MCS0	-94.6	
	802.11n, HT20 /MCS7	-75.7	
	802.11ax, HE20 /MCS0	-94.5	
	802.11ax, HE20 /MCS9	-69.1	
Maximum input Level (Pass 802.11 PER spec.)	802.11b /1Mbps	10	dBm
	802.11b /11Mbps	10	
	802.11g /6Mbps	10	
	802.11g /54Mbps	0.3	
	802.11n, HT20 /MCS0	10	
	802.11n, HT20 /MCS7	-1.0	
	802.11ax, HE20 /MCS0	10	
	802.11ax, HE20 /MCS9	-4.3	
Adjacent Channel Rejection (Pass 802.11 spec. Interference pattern by IQxel)	802.11b /1Mbps	50	dB
	802.11b /11Mbps	50	
	802.11g /6Mbps	30	

	802.11g /54Mbps	11	
	802.11n, HT20 /MCS0	29	
	802.11n, HT20 /MCS7	10	
	802.11ax, HE20 /MCS0	25	
	802.11ax, HE20 /MCS9	-1	

5.2. Bluetooth LE characteristics

Table 5-2. BLE characteristics

Features	Description	
Bluetooth LE Specification	Bluetooth LE V5.2	
Host interface	UART	
Range of frequency	2402 MHz ~ 2480 MHz	
channels	40	
Transmitter characteristics		
Transmitter Power Range	-24.0 ~ 15.0 dBm	
Receiver characteristics	Rate	Typical Value (dBm)
Receiver Sensitivity (@ PER=30.8%)	LE 1Mbps	-100.5
	LE 2Mbps	-97.5
	LE 125Kbps	-107.6
	LE 500Kbps	-101.6
Receiver Maximum input Level (@ PER=30.8%)	LE 1Mbps	10
	LE 2Mbps	10
	LE 125Kbps	10
	LE 500Kbps	10

6. Electrical Characteristics

6.1. Absolute maximum ratings

Table 6-1. Absolute maximum ratings

Symbol	MIN	MAX	Unit
Supply Voltage	-0.3	3.6	V
Storage Temperature	-40	125	deg.C

6.2. Operating conditions

Table 6-2. Operating conditions

Symbol	MIN	TYP	MAX	Unit
Supply Voltage	3.0	3.3	3.6	V
Operating Temperature (grade 6 module)	-40	25	85	deg.C
Operating Temperature (grade 7 module)	-40	25	105	deg.C

6.3. Power consumption

Table 6-3. Power consumption ⁽¹⁾⁽²⁾⁽³⁾

Power Mode	Description	Typical value	Unit
Wi-Fi Active	Tx 802.11b, 1Mbps, Pout = 18dBm	334.5	mA
	Tx 802.11b /11Mbps, Pout = 17dBm	322	
	Tx 802.11g /6Mbps, Pout = 18dBm	338.5	
	Tx 802.11g /54Mbps, Pout = 15dBm	304	
	Tx 802.11n, HT20 /MCS0, Pout = 18dBm	338	
	Tx 802.11n, HT20 /MCS7, Pout = 14dBm	295	
	Tx 802.11ax, HE20 /MCS0, Pout = 18dBm	337.5	
	Tx 802.11ax, HE20 /MCS9, Pout = 12dBm	273.5	
	Rx 802.11b, 1Mbps, Pin = -90dBm	97.5	
	Rx 802.11b /11Mbps, Pin = -80dBm	98.5	
	Rx 802.11g /6Mbps, Pin = -80dBm	99.5	
	Rx 802.11g /54Mbps, Pin = -70dBm	101.5	
	Rx 802.11n, HT20 /MCS0, Pin = -75dBm	99.5	
	Rx 802.11n, HT20 /MCS7, Pin = -65dBm	101.5	
	Rx 802.11ax, HE20 /MCS0, Pin = -75dBm	100	
	Rx 802.11ax, HE20 /MCS9, Pin = -60dBm	110.5	
BLE Active	Tx LE 1Mbps, Pout = -24dBm	124	mA

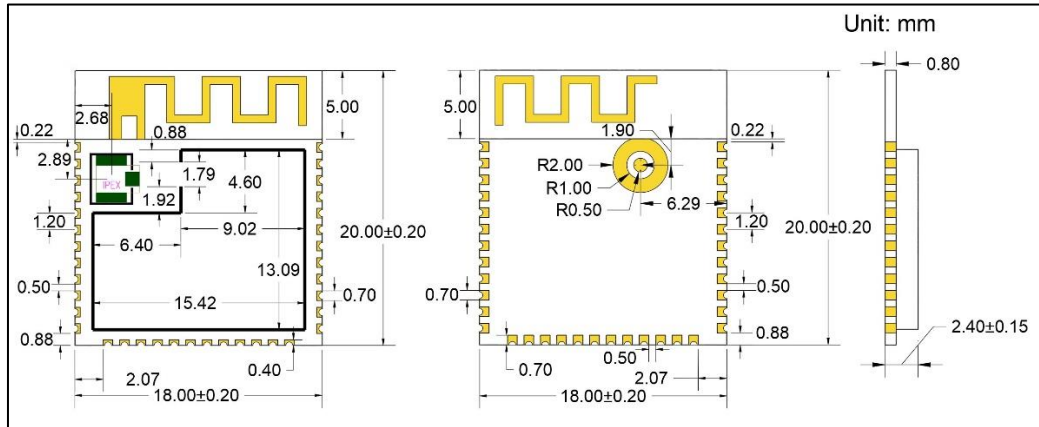
	Tx LE 1Mbps, Pout = 0dBm	136	
	Tx LE 1Mbps, Pout = 15dBm	256.5	
	Rx LE 1Mbps, Pin = -80dBm	94	
Wi-Fi Sleep	MCU in Run mode	39.1	mA
Mild Sleep	DTIM=1	1.82	mA
	DTIM=3	0.73	mA
	DTIM=10	0.4	mA

- (1) DC Power = 3.3 V, HXTAL = 40 MHz
- (2) Continuous Tx, Duty cycle = 100%.
- (3) The DTIM power consumption is equal to the average power consumption of multiple beacon intervals.

7. Size information

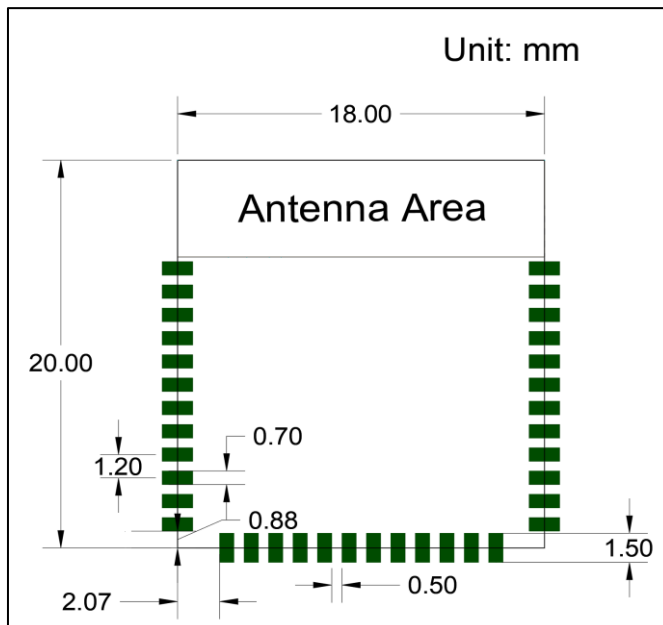
7.1. Physical dimensions

Figure 7-1. Physical dimensions



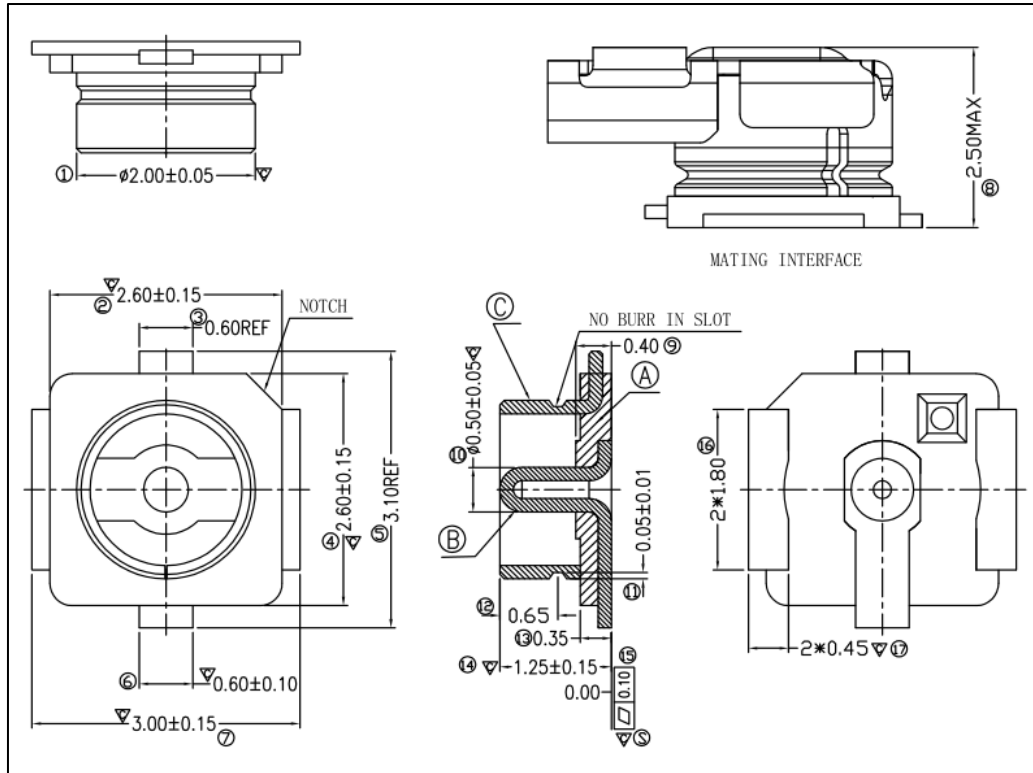
7.2. Layout recommendation

Figure 7-2. Layout recommendation



7.3. Dimensions of external antenna connector

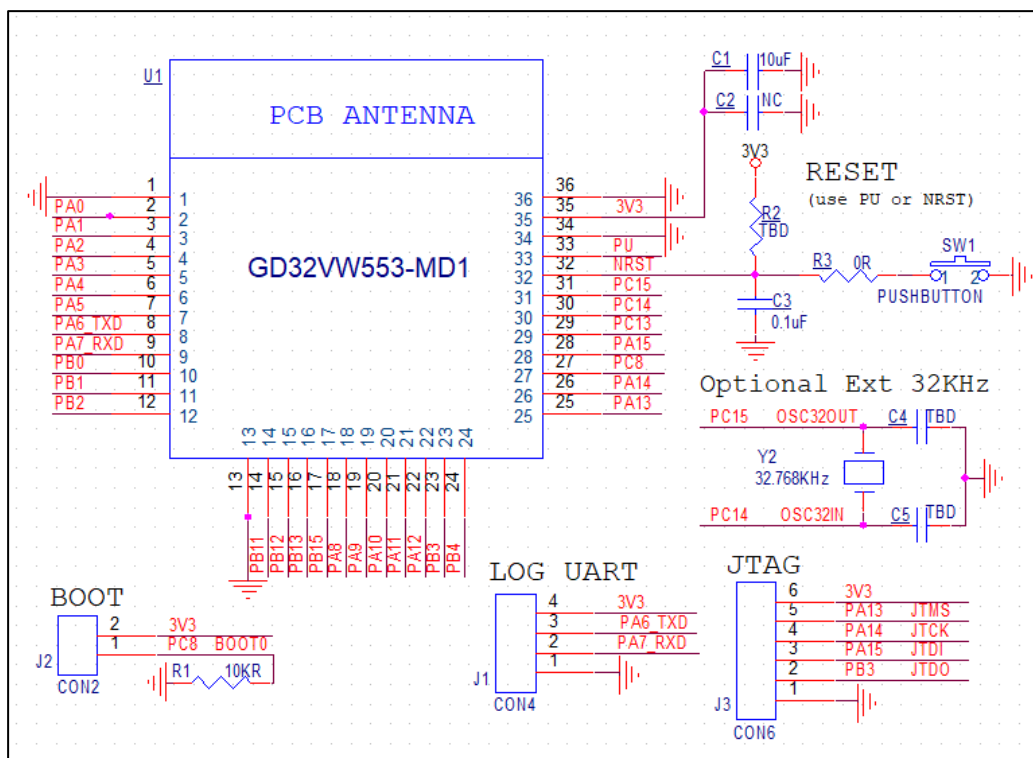
Figure 7-3. Dimensions of IPEX connector



8. Peripheral circuit reference design

Module pins PU and NRST are the power supply enable and reset pins respectively. The chip can operate only when both pins are pulled up. A 0.1uF filter capacitor and a 10K Ohm pull-up resistor have been placed in the module circuit for NRST and PU. If the GD32VW553 is used as a master MCU, it is recommended to use NRST as the enable pin with PU always pulled up. If the GD32VW553 is used as a slave device, it is recommended to use PU as the enable pin with NRST always pulled up. Besides, the log Uart and Jtag pins are recommended to be connected out.

Figure 8-1. Reference design



The power supply of 3.3V must provide a minimum of 500mA.

The selected pins for the boot mode are BOOT0 (PC8) and BOOT1 (PB1). Definitions of several modes are shown in the table below. Typically, flash boot mode is utilized, therefore BOOT0 needs to be pulled down on the motherboard.

Table 8-1. Boot mode selection

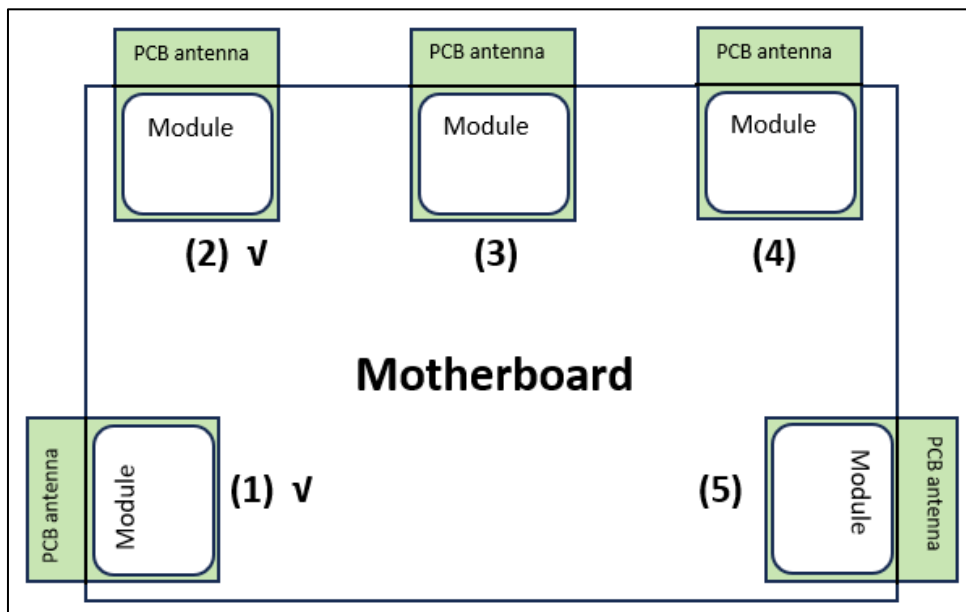
BOOT1	BOOT0	Start-up Mode
X	0	Flash
0	1	Legacy Bootloader
1	1	SRAM

9. Requirements for antenna placement

If using the onboard PCB antenna, the antenna area of the module needs to extend away from the motherboard. The distance between the PCB of the motherboard and other metal devices must have a minimum clearance of 15mm. The area below and above the onboard antenna area is required to be kept away from metal devices, sensors, interference sources, and other materials that may cause signal interference.

The recommended placement of the module is shown below.

Figure 9-1. Recommended Placement



10. Recommended reflow profile

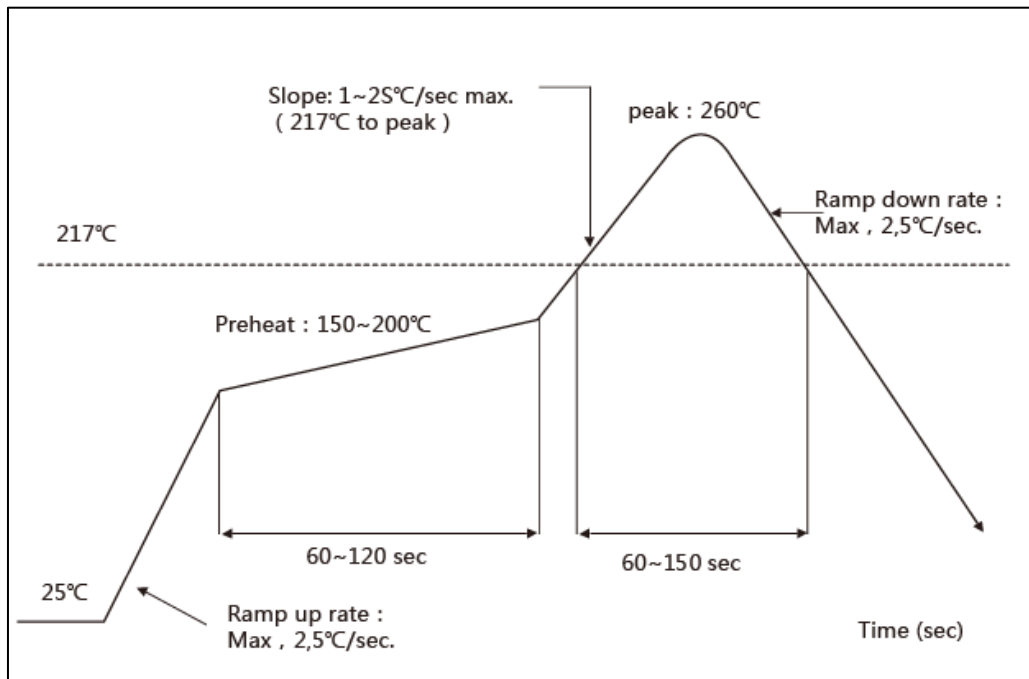
Referred to IPC/JEDEC standard

Peak Temperature: 260 ± 5 °C

5Time within 5°C of peak temperature: ≥ 10 s

Number of Times: 2 times

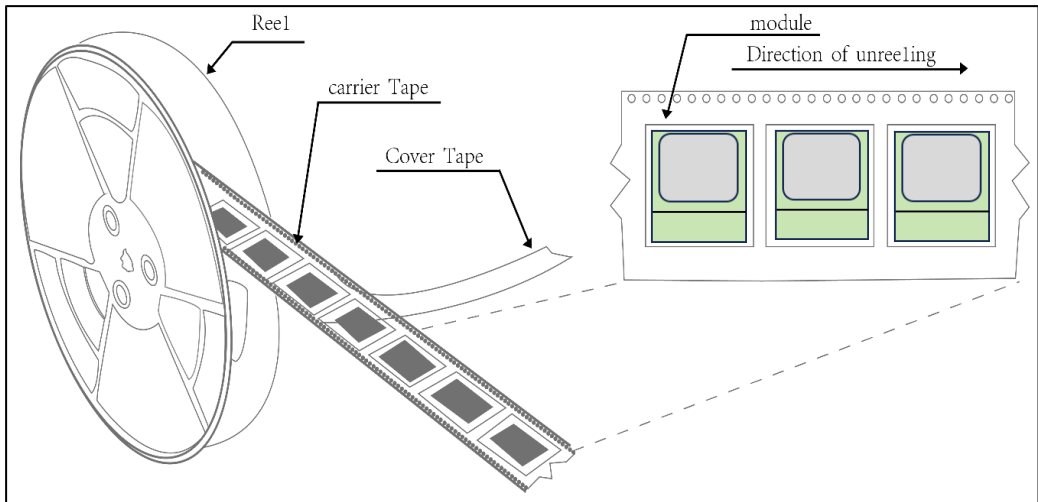
Figure 10-1. Recommended reflow profile



11. Package

11.1. Reel

Figure 11-1. Reel detail



12. Moisture sensitivity

The Module is a level 3 Moisture Sensitive Device, by the standard IPC/JEDEC J-STD-020. Special care must be provided to adhere to all of the requirements for using this class of component. Furthermore, the customer must allow for the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity (RH).
- b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.
- c) The maximum time between the opening of the sealed bag and the reflow process allowed is 168 hours if "IPC/JEDEC J-STD-033A paragraph 5.2" is respected.
- e) Baking is required if either conditions b) or c) are not respected.
- f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

13. Revision history

Table 13-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Dec.3 rd , 2024

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