# GigaDevice Semiconductor Inc.

# GD32E507xx
# Arm® Cortex®-M33 32-bit MCU

Datasheet

Revision 2.2

(Aug. 2026)

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# 1. General description

The GD32E507xx device belongs to the high performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M33 core. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The processor is based on the ARMv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32E507xx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at up to 180 MHz frequency with Flash accesses 0~4 waiting time to obtain maximum efficiency. It provides up to 512 KB embedded Flash memory and up to 128 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer two 12-bit ADCs, two DACs, three comparators, up to nine general 16-bit timers, a general 32-bit timer, two basic timers, two PWM advanced timers, as well as standard and advanced communication interfaces: up to three SPIs, three I2Cs, six USARTs, two I2Ss, an USBHS, an ENET and three CANs. Additional peripherals as trigonometric math unit (TMU), super high-resolution Timer (SHRTIMER), EXMC interface, Serial/Quad Parallel Interface (SQPI) are included.

The device operates from a 1.71 to 3.63 V power supply and available in -40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32E507xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike, optical module and so on.



# 2. Device overview

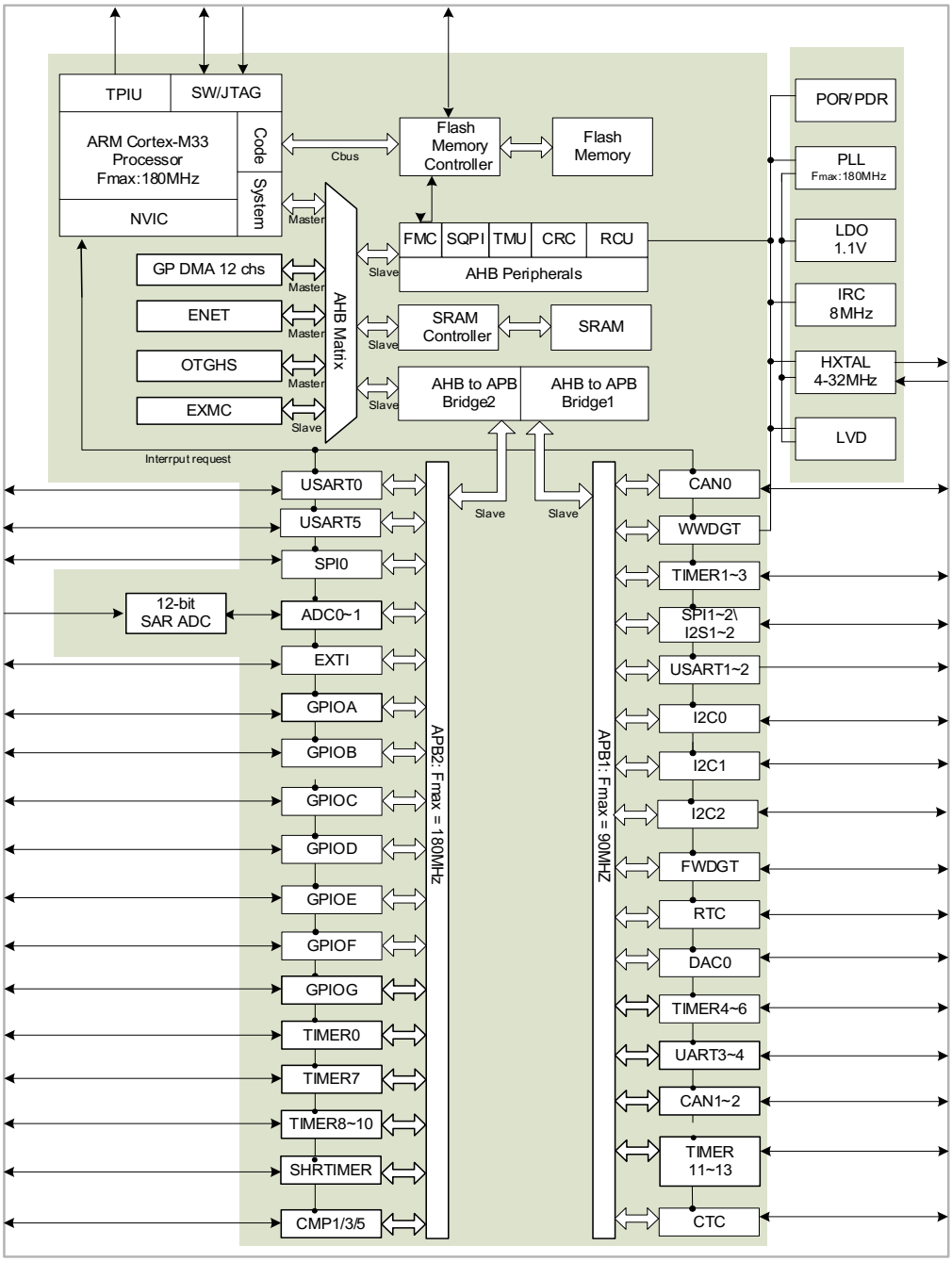
## 2.1. Device information

**Table 2-1. GD32E507xx devices features and peripheral list**

| Part Number | | GD32E507xx | | | | | |
|---|---|---|---|---|---|---|---|
| | | RC | RE | VC | VE | ZC | ZE |
| FLASH (KB) | | 256 | 512 | 256 | 512 | 256 | 512 |
| SRAM (KB) | | 96 | 128 | 96 | 128 | 96 | 128 |
| Timers | General timer(16-bit) | 3 (2-4) | 9 (2-4,8-13) | 3 (2-4) | 9 (2-4,8-13) | 3 (2-4) | 9 (2-4,8-13) |
| | General timer(32-bit) | 1 (1) | 1 (1) | 1 (1) | 1 (1) | 1 (1) | 1 (1) |
| | Advanced timer(16-bit) | 1 (0) | 2 (0,7) | 1 (0) | 2 (0,7) | 2 (0,7) | 2 (0,7) |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic timer(16-bit) | 2 (5-6) | 2 (5-6) | 2 (5-6) | 2 (5-6) | 2 (5-6) | 2 (5-6) |
| | SHRTIMER | 1 | 1 | 1 | 1 | 1 | 1 |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART | 4 (0-2,5) | 4 (0-2,5) | 4 (0-2,5) | 4 (0-2,5) | 4 (0-2,5) | 4 (0-2,5) |
| | UART | 2 (3-4) | 2 (3-4) | 2 (3-4) | 2 (3-4) | 2 (3-4) | 2 (3-4) |
| | I2C | 3 (0-2) | 3 (0-2) | 3 (0-2) | 3 (0-2) | 3 (0-2) | 3 (0-2) |
| | SPI/I2S | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) |
| | Ethernet | 1 | 1 | 1 | 1 | 1 | 1 |
| | CAN | 3 (0-2) | 3 (0-2) | 3 (0-2) | 3 (0-2) | 3 (0-2) | 3 (0-2) |
| | USBHS | 1 | 1 | 1 | 1 | 1 | 1 |
| GPIO | | 51 | 51 | 80 | 80 | 112 | 112 |
| EXMC | | 0 | 0 | 1 | 1 | 1 | 1 |
| DAC | Units | 1 | 1 | 1 | 1 | 1 | 1 |
| | Channels | 2 | 2 | 2 | 2 | 2 | 2 |
| CMP | | 3 | 3 | 3 | 3 | 3 | 3 |
| TMU | | 1 | 1 | 1 | 1 | 1 | 1 |
| ADC | Units | 2 | 2 | 2 | 2 | 2 | 2 |
| | Channels | 16 | 16 | 16 | 16 | 16 | 16 |
| Package | | LQFP64 | | LQFP100 | | LQFP144 | |

## 2.2. Block diagram

**Figure 2-1. GD32E507xx block diagram**



## 2.3. Pinouts and pin assignment

**Figure 2-2. GD32E507Zx LQFP144 pinouts**



**Figure 2-3. GD32E507Vx LQFP100 pinouts**

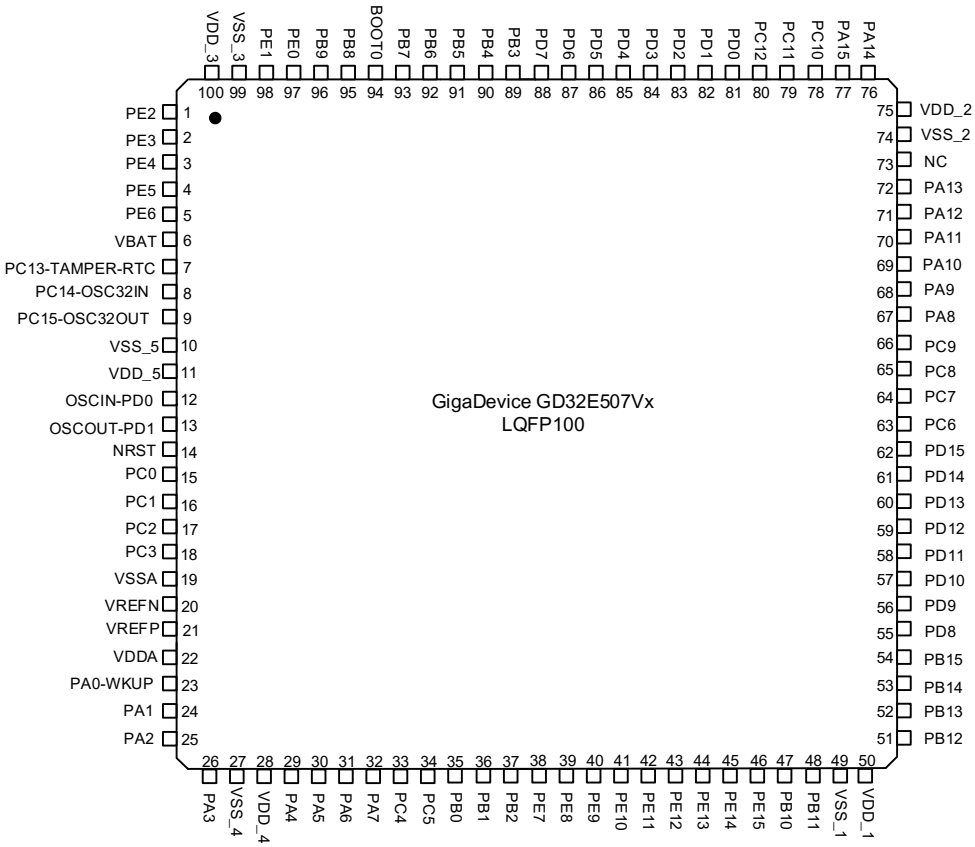
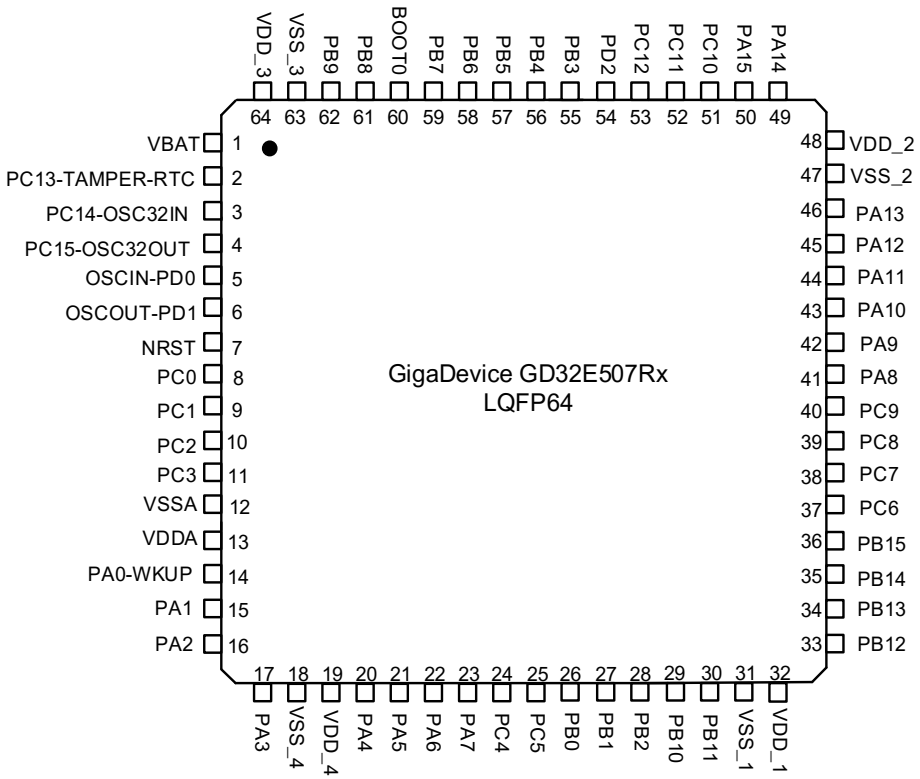


**Figure 2-4. GD32E507Rx LQFP64 pinouts**



## 2.4. Memory map

**Table 2-2. GD32E507xx memory map**

| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| External device | AHB3 | 0xC000 0000 – 0xDFFF FFFF | Reserved |
| | | 0xB000 0000 – 0xBFFF FFFF | SQPI_PSRAM(MEM) |
| | | 0xA000 1400 – 0xAFFF FFFF | Reserved |
| | | 0xA000 1000 – 0xA000 13FF | SQPI_PSRAM(REG) |
| | | 0xA000 0000 – 0xA000 0FFF | EXMC – SWREG |
| External RAM | | 0x9000 0000 – 0x9FFF FFFF | EXMC – PC CARD |
| | | 0x7000 0000 – 0x8FFF FFFF | EXMC – NAND |
| | | 0x6000 0000 – 0x6FFF FFFF | EXMC – NOR/PSRAM/SRAM |
| Peripheral | AHB1 | 0x5000 0000 – 0x5003 FFFF | USBHS |
| | | 0x4008 0400 – 0x4FFF FFFF | Reserved |
| | | 0x4008 0000 – 0x4008 03FF | TMU |
| | | 0x4004 0000 – 0x4007 FFFF | Reserved |
| | | 0x4002 BC00 – 0x4003 FFFF | Reserved |
| | | 0x4002 B000 – 0x4002 BBFF | Reserved |
| | | 0x4002 A000 – 0x4002 AFFF | Reserved |
| | | 0x4002 8000 – 0x4002 9FFF | ENET |
| | | 0x4002 6800 – 0x4002 7FFF | Reserved |
| | | 0x4002 6400 – 0x4002 67FF | Reserved |
| | | 0x4002 6000 – 0x4002 63FF | Reserved |
| | | 0x4002 5000 – 0x4002 5FFF | Reserved |
| | | 0x4002 4000 – 0x4002 4FFF | Reserved |
| | | 0x4002 3C00 – 0x4002 3FFF | Reserved |
| | | 0x4002 3800 – 0x4002 3BFF | Reserved |
| | | 0x4002 3400 – 0x4002 37FF | Reserved |
| | | 0x4002 3000 – 0x4002 33FF | CRC |
| | | 0x4002 2C00 – 0x4002 2FFF | Reserved |
| | | 0x4002 2800 – 0x4002 2BFF | Reserved |
| | | 0x4002 2400 – 0x4002 27FF | Reserved |
| | | 0x4002 2000 – 0x4002 23FF | FMC |
| | | 0x4002 1C00 – 0x4002 1FFF | Reserved |
| | | 0x4002 1800 – 0x4002 1BFF | Reserved |
| | | 0x4002 1400 – 0x4002 17FF | Reserved |
| | | 0x4002 1000 – 0x4002 13FF | RCU |
| | | 0x4002 0C00 – 0x4002 0FFF | Reserved |
| | | 0x4002 0800 – 0x4002 0BFF | Reserved |
| | | 0x4002 0400 – 0x4002 07FF | DMA1 |

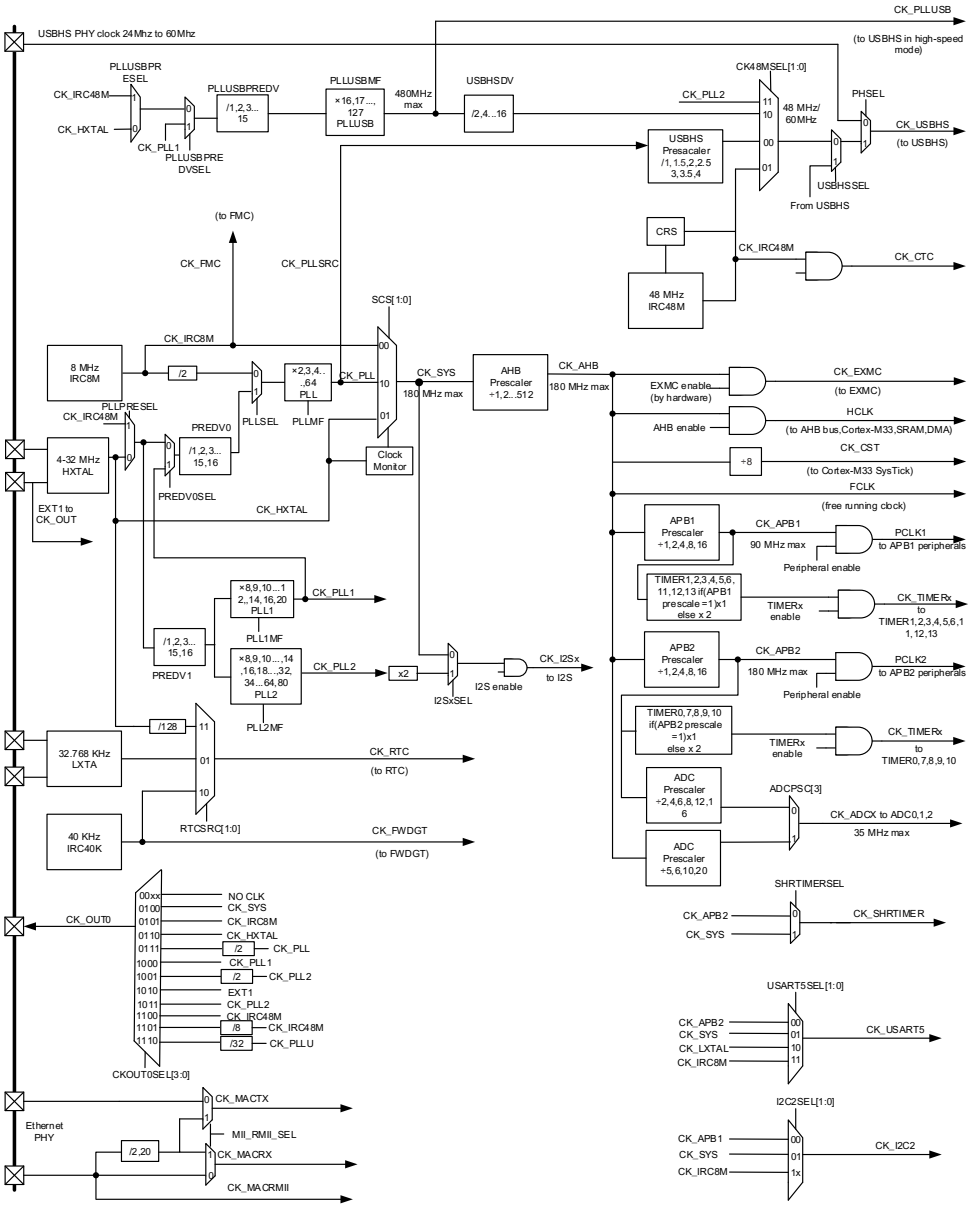
| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| | | 0x4002 0000 – 0x4002 03FF | DMA0 |
| | | 0x4001 8400 – 0x4001 FFFF | Reserved |
| | | 0x4001 8000 – 0x4001 83FF | Reserved |
| | APB2 | 0x4001 7C00 – 0x4001 7FFF | CMP |
| | | 0x4001 7800 – 0x4001 7BFF | Reserved |
| | | 0x4001 7400 – 0x4001 77FF | SHRTIMER |
| | | 0x4001 7000 – 0x4001 73FF | USART5 |
| | | 0x4001 6C00 – 0x4001 6FFF | Reserved |
| | | 0x4001 6800 – 0x4001 6BFF | Reserved |
| | | 0x4001 5C00 – 0x4001 67FF | Reserved |
| | | 0x4001 5800 – 0x4001 5BFF | Reserved |
| | | 0x4001 5400 – 0x4001 57FF | TIMER10 |
| | | 0x4001 5000 – 0x4001 53FF | TIMER9 |
| | | 0x4001 4C00 – 0x4001 4FFF | TIMER8 |
| | | 0x4001 4800 – 0x4001 4BFF | Reserved |
| | | 0x4001 4400 – 0x4001 47FF | Reserved |
| | | 0x4001 4000 – 0x4001 43FF | Reserved |
| | | 0x4001 3C00 – 0x4001 3FFF | Reserved |
| | | 0x4001 3800 – 0x4001 3BFF | USART0 |
| | | 0x4001 3400 – 0x4001 37FF | TIMER7 |
| | | 0x4001 3000 – 0x4001 33FF | SPI0 |
| | | 0x4001 2C00 – 0x4001 2FFF | TIMER0 |
| | | 0x4001 2800 – 0x4001 2BFF | ADC1 |
| | | 0x4001 2400 – 0x4001 27FF | ADC0 |
| | | 0x4001 2000 – 0x4001 23FF | GPIOG |
| | | 0x4001 1C00 – 0x4001 1FFF | GPIOF |
| | | 0x4001 1800 – 0x4001 1BFF | GPIOE |
| | | 0x4001 1400 – 0x4001 17FF | GPIOD |
| | | 0x4001 1000 – 0x4001 13FF | GPIOC |
| | | 0x4001 0C00 – 0x4001 0FFF | GPIOB |
| | | 0x4001 0800 – 0x4001 0BFF | GPIOA |
| | | 0x4001 0400 – 0x4001 07FF | EXTI |
| | | 0x4001 0000 – 0x4001 03FF | AFIO |
| | APB1 | 0x4000 CC00 – 0x4000 FFFF | Reserved |
| | | 0x4000 CC00 – 0x4000 CFFF | CAN2 |
| | | 0x4000 C800 – 0x4000 CBFF | CTC |
| | | 0x4000 C400 – 0x4000 C7FF | Reserved |
| | | 0x4000 C000 – 0x4000 C3FF | I2C2 |
| | | 0x4000 8C00 – 0x4000 BFFF | Reserved |
| | | 0x4000 8800 – 0x4000 8BFF | CAN2SRAM |
| | | 0x4000 8400 – 0x4000 87FF | USBSRAM_B |

| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| | | 0x4000 8000 – 0x4000 BFFF | Reserved |
| | | 0x4000 7C00 – 0x4000 7FFF | Reserved |
| | | 0x4000 7800 – 0x4000 7BFF | Reserved |
| | | 0x4000 7400 – 0x4000 77FF | DAC0 |
| | | 0x4000 7000 – 0x4000 73FF | PMU |
| | | 0x4000 6C00 – 0x4000 6FFF | BKP |
| | | 0x4000 6800 – 0x4000 6BFF | CAN1 |
| | | 0x4000 6400 – 0x4000 67FF | CAN0 |
| | | 0x4000 6000 – 0x4000 63FF | CAN SRAM 512 bytes |
| | | 0x4000 5C00 – 0x4000 5FFF | Reserved |
| | | 0x4000 5800 – 0x4000 5BFF | I2C1 |
| | | 0x4000 5400 – 0x4000 57FF | I2C0 |
| | | 0x4000 5000 – 0x4000 53FF | UART4 |
| | | 0x4000 4C00 – 0x4000 4FFF | UART3 |
| | | 0x4000 4800 – 0x4000 4BFF | USART2 |
| | | 0x4000 4400 – 0x4000 47FF | USART1 |
| | | 0x4000 4000 – 0x4000 43FF | I2S2_add |
| | | 0x4000 3C00 – 0x4000 3FFF | SPI2/I2S2 |
| | | 0x4000 3800 – 0x4000 3BFF | SPI1/I2S1 |
| | | 0x4000 3400 – 0x4000 37FF | I2S1_add |
| | | 0x4000 3000 – 0x4000 33FF | FWDGT |
| | | 0x4000 2C00 – 0x4000 2FFF | WWDGT |
| | | 0x4000 2800 – 0x4000 2BFF | RTC |
| | | 0x4000 2400 – 0x4000 27FF | Reserved |
| | | 0x4000 2000 – 0x4000 23FF | TIMER13 |
| | | 0x4000 1C00 – 0x4000 1FFF | TIMER12 |
| | | 0x4000 1800 – 0x4000 1BFF | TIMER11 |
| | | 0x4000 1400 – 0x4000 17FF | TIMER6 |
| | | 0x4000 1000 – 0x4000 13FF | TIMER5 |
| | | 0x4000 0C00 – 0x4000 0FFF | TIMER4 |
| | | 0x4000 0800 – 0x4000 0BFF | TIMER3 |
| | | 0x4000 0400 – 0x4000 07FF | TIMER2 |
| | | 0x4000 0000 – 0x4000 03FF | TIMER1 |
| SRAM | AHB | 0x2007 0000 – 0x3FFF FFFF | Reserved |
| | | 0x2006 0000 – 0x2006 FFFF | Reserved |
| | | 0x2003 0000 – 0x2005 FFFF | Reserved |
| | | 0x2002 0000 – 0x2002 FFFF | Reserved |
| | | 0x2000 0000 – 0x2001 FFFF | SRAM |
| Code | AHB | 0x1FFF F810 – 0x1FFF FFFF | Reserved |
| | | 0x1FFF F800 – 0x1FFF F80F | Option Bytes |
| | | 0x1FFF B000 – 0x1FFF F7FF | Boot loader |

| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| | | 0x1FFF 7800 – 0x1FFF AFFF | Reserved |
| | | 0x1FFF 7000 – 0x1FFF 77FF | OTP |
| | | 0x1FFF 0000 – 0x1FFF 6FFF | Reserved |
| | | 0x1FFE C010 – 0x1FFE FFFF | Reserved |
| | | 0x1FFE C000 – 0x1FFE C00F | Reserved |
| | | 0x1001 0000 – 0x1FFE BFFF | Reserved |
| | | 0x1000 0000 – 0x1000 FFFF | Reserved |
| | | 0x083C 0000 – 0x0FFF FFFF | Reserved |
| | | 0x0830 0000 – 0x083B FFFF | Reserved |
| | | 0x0808 0000 – 0x082F FFFF | Reserved |
| | | 0x0800 0000 – 0x0807 FFFF | Main Flash |
| | | 0x0030 0000 – 0x07FF FFFF | Reserved |
| | | 0x0010 0000 – 0x002F FFFF | Reserved |
| | | 0x0008 0000 – 0x000F FFFF | Reserved |
| | | 0x0002 0000 – 0x0007 FFFF | Aliased to Main Flash or Boot loader |
| | | 0x0000 0000 – 0x0001 FFFF | |

## 2.5. Clock tree

**Figure 2-5. GD32E507xx clock tree**




**Note:**

The TIMERs are clocked by the clock divided from CK_APB2 and CK_APB1. The frequency of TIMERs clock is equal to CK_APBx(APB prescaler is 1), twice the CK_APBx(APB prescaler is not 1).

**Legend:**

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillator

IRC40K: Internal 40K RC oscillator

IRC48M: Internal 48M RC oscillator

## 2.6. Pin definitions

### 2.6.1. GD32E507Zx LQFP144 pin definitions

**Table 2-3. GD32E507Zx LQFP144 pin definitions**

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PE2 | 1 | I/O | 5VT | Default: PE2<br>Alternate2: EXMC_A23 |
| PE3 | 2 | I/O | 5VT | Default: PE3<br>Alternate2: EXMC_A19 |
| PE4 | 3 | I/O | 5VT | Default: PE4<br>Alternate2: EXMC_A20 |
| PE5 | 4 | I/O | 5VT | Default: PE5<br>Alternate2: EXMC_A21<br>Remap: TIMER8_CH0(4) |
| PE6 | 5 | I/O | 5VT | Default: PE6<br>Alternate2: EXMC_A22, WKUP2<br>Remap: TIMER8_CH1(4) |
| VBAT | 6 | P | | Default: VBAT |
| PC13-TAMPER-RTC | 7 | I/O | | Default: PC13<br>Alternate2: TAMPER-RTC, WKUP1 |
| PC14-OSC32IN | 8 | I/O | | Default: PC14<br>Alternate2: OSC32IN |
| PC15-OSC32OUT | 9 | I/O | | Default: PC15<br>Alternate2: OSC32OUT |
| PF0 | 10 | I/O | 5VT | Default: PF0<br>Alternate2: EXMC_A0, SQPI_D0<br>Remap: CTC_SYNC |
| PF1 | 11 | I/O | 5VT | Default: PF1<br>Alternate2: EXMC_A1 |
| PF2 | 12 | I/O | 5VT | Default: PF2<br>Alternate2: EXMC_A2, SQPI_D2 |
| PF3 | 13 | I/O | 5VT | Default: PF3<br>Alternate2: EXMC_A3 |
| PF4 | 14 | I/O | 5VT | Default: PF4<br>Alternate2: EXMC_A4, SQPI_D1 |
| PF5 | 15 | I/O | 5VT | Default: PF5<br>Alternate2: EXMC_A5 |
| VSS_5 | 16 | P | | Default: VSS_5 |
| VDD_5 | 17 | P | | Default: VDD_5 |
| PF6 | 18 | I/O | | Default: PF6<br>Alternate2: EXMC_NIORD, SQPI_CSN<br>Remap: TIMER9_CH0(4) |

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PF7 | 19 | I/O | | Default: PF7<br>Alternate2: EXMC_NREG<br>Remap: TIMER10_CH0(4) |
| PF8 | 20 | I/O | | Default: PF8<br>Alternate2: EXMC_NIOWR, WKUP7, SQPI_CLK<br>Remap: TIMER12_CH0(4) |
| PF9 | 21 | I/O | | Default: PF9<br>Alternate2: EXMC_CD<br>Remap: TIMER13_CH0(4) |
| PF10 | 22 | I/O | | Default: PF10<br>Alternate2: EXMC_INTR, SQPI_D3 |
| OSCIN-PD0 | 23 | I | | Default: OSCIN<br>Remap: PD0 |
| OSCOUT-PD1 | 24 | O | | Default: OSCOUT<br>Remap: PD1 |
| NRST | 25 | I/O | | Default: NRST |
| PC0 | 26 | I/O | | Default: PC0<br>Alternate1: USBHS_ULPI_STP<br>Alternate2: ADC01_IN10 |
| PC1 | 27 | I/O | | Default: PC1<br>Alternate2: ADC01_IN11, ENET_MII_MDC, ENET_RMII_MDC |
| PC2 | 28 | I/O | | Default: PC2<br>Alternate1: USBHS_ULPI_DIR, I2S1_ADD_SD<br>Alternate2: ADC01_IN12, ENET_MII_TXD2 |
| PC3 | 29 | I/O | | Default: PC3<br>Alternate1: USBHS_ULPI_NXT<br>Alternate2: ADC01_IN13, ENET_MII_TX_CLK |
| VSSA | 30 | P | | Default: VSSA |
| VREFN | 31 | P | | Default: VREFN |
| VREFP | 32 | P | | Default: VREFP |
| VDDA | 33 | P | | Default: VDDA |
| PA0-WKUP | 34 | I/O | | Default: PA0<br>Alternate2: WKUP0, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, ENET_MII_CRS |
| PA1 | 35 | I/O | | Default: PA1<br>Alternate2: USART1_RTS, ADC01_IN1, TIMER4_CH1, TIMER1_CH1, ENET_MII_RX_CLK, ENET_RMII_REF_CLK |
| PA2 | 36 | I/O | | Default: PA2<br>Alternate1: CMP1_OUT<br>Alternate2: USART1_TX, TIMER4_CH2, ADC01_IN2, TIMER8_CH0(4), TIMER1_CH2, ENET_MII_MDIO, ENET_RMII_MDIO, SPI0_IO2, WKUP3, CMP1_IM6 |

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PA3 | 37 | I/O | | Default: PA3<br>Alternate1: USBHS_ULPI_D0<br>Alternate2: USART1_RX, TIMER4_CH3, ADC01_IN3, TIMER1_CH3, TIMER8_CH1(4), ENET_MII_COL, SPI0_IO3 |
| VSS_4 | 38 | P | | Default: VSS_4 |
| VDD_4 | 39 | P | | Default: VDD_4 |
| PA4 | 40 | I/O | | Default: PA4<br>Alternate2: SPI0_NSS, USART1_CK, DAC0_OUT0, ADC01_IN4, CMP1_IM4, CMP3_IM4, CMP5_IM4<br>Remap: SPI2_NSS, I2S2_WS |
| PA5 | 41 | I/O | | Default: PA5<br>Alternate1: USBHS_ULPI_CK<br>Alternate2: SPI0_SCK, ADC01_IN5, DAC0_OUT1, CMP1_IM5, CMP3_IM5, CMP5_IM5 |
| PA6 | 42 | I/O | | Default: PA6<br>Alternate2: SPI0_MISO, TIMER7_BRKIN, ADC01_IN6, TIMER2_CH0, TIMER12_CH0(4)<br>Remap: TIMER0_BRKIN |
| PA7 | 43 | I/O | | Default: PA7<br>Alternate2: SPI0_MOSI, TIMER7_CH0_ON, ADC01_IN7, TIMER2_CH1, TIMER13_CH0(4), ENET_MII_RX_DV, ENET_RMII_CRS_DV, CMP1_IP<br>Remap: TIMER0_CH0_ON |
| PC4 | 44 | I/O | | Default: PC4<br>Alternate2: ADC01_IN14, ENET_MII_RXD0, ENET_RMII_RXD0 |
| PC5 | 45 | I/O | | Default: PC5<br>Alternate2: ADC01_IN15, ENET_MII_RXD1, ENET_RMII_RXD1, WKUP4 |
| PB0 | 46 | I/O | | Default: PB0<br>Alternate1: USBHS_ULPI_D1<br>Alternate2: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON, ENET_MII_RXD2, CMP3_IP<br>Remap: TIMER0_CH1_ON |
| PB1 | 47 | I/O | | Default: PB1<br>Alternate1: CMP3_OUT, USBHS_ULPI_D2, SHRTIMER_SCOUT<br>Alternate2: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON, ENET_MII_RXD3<br>Remap: TIMER0_CH2_ON |
| PB2 | 48 | I/O | 5VT | Default: PB2, BOOT1<br>Alternate1: USBHS_ULPI_D4, SHRTIMER_SCIN<br>Alternate2: CMP3_IM7 |
| PF11 | 49 | I/O | 5VT | Default: PF11 |

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Alternate2: EXMC_NIOS16 |
| PF12 | 50 | I/O | 5VT | Default: PF12<br>Alternate2: EXMC_A6 |
| VSS_6 | 51 | P | | Default: VSS_6 |
| VDD_6 | 52 | P | | Default: VDD_6 |
| PF13 | 53 | I/O | 5VT | Default: PF13<br>Alternate2: EXMC_A7 |
| PF14 | 54 | I/O | 5VT | Default: PF14<br>Alternate2: EXMC_A8 |
| PF15 | 55 | I/O | 5VT | Default: PF15<br>Alternate2: EXMC_A9 |
| PG0 | 56 | I/O | 5VT | Default: PG0<br>Alternate2: EXMC_A10 |
| PG1 | 57 | I/O | 5VT | Default: PG1<br>Alternate2: EXMC_A11 |
| PE7 | 58 | I/O | 5VT | Default: PE7<br>Alternate2: EXMC_D4<br>Remap: TIMER0_ETI |
| PE8 | 59 | I/O | 5VT | Default: PE8<br>Alternate1: CMP1_OUT<br>Alternate2: EXMC_D5<br>Remap: TIMER0_CH0_ON |
| PE9 | 60 | I/O | 5VT | Default: PE9<br>Alternate1: CMP3_OUT<br>Alternate2: EXMC_D6<br>Remap: TIMER0_CH0 |
| VSS_7 | 61 | P | | Default: VSS_7 |
| VDD_7 | 62 | P | | Default: VDD_7 |
| PE10 | 63 | I/O | 5VT | Default: PE10<br>Alternate1: CMP5_OUT<br>Alternate2: EXMC_D7<br>Remap: TIMER0_CH1_ON |
| PE11 | 64 | I/O | 5VT | Default: PE11<br>Alternate1: CMP5_OUT<br>Alternate2: EXMC_D8<br>Remap: TIMER0_CH1 |
| PE12 | 65 | I/O | 5VT | Default: PE12<br>Alternate1: CMP3_OUT<br>Alternate2: EXMC_D9<br>Remap: TIMER0_CH2_ON |
| PE13 | 66 | I/O | 5VT | Default: PE13<br>Alternate1: CMP1_OUT<br>Alternate2: EXMC_D10<br>Remap: TIMER0_CH2 |
| PE14 | 67 | I/O | 5VT | Default: PE14 |

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Alternate2: EXMC_D11<br>Remap: TIMER0_CH3 |
| PE15 | 68 | I/O | 5VT | Default: PE15<br>Alternate2: EXMC_D12<br>Remap: TIMER0_BRKIN |
| PB10 | 69 | I/O | 5VT | Default: PB10<br>Alternate1: CAN2_RX, USBHS_ULPI_D3, SHRTIMER_FLT2<br>Alternate2: I2C1_SCL, USART2_TX, ENET_MII_RX_ER<br>Remap: TIMER1_CH2 |
| PB11 | 70 | I/O | 5VT | Default: PB11<br>Alternate1: CAN2_TX, USBHS_ULPI_D4, SHRTIMER_FLT3<br>Alternate2: I2C1_SDA, USART2_RX, ENET_MII_TX_EN, ENET_RMII_TX_EN, CMP5_IP<br>Remap: TIMER1_CH3 |
| VSS_1 | 71 | P | | Default: VSS_1 |
| VDD_1 | 72 | P | | Default: VDD_1 |
| PB12 | 73 | I/O | 5VT | Default: PB12<br>Alternate1: USBHS_ULPI_D5, SHRTIMER_ST2CH0<br>Alternate2: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, CAN1_RX, ENET_MII_TXD0, ENET_RMII_TXD0 |
| PB13 | 74 | I/O | 5VT | Default: PB13<br>Alternate1: USBHS_ULPI_D6, SHRTIMER_ST2CH1<br>Alternate2: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, CAN1_TX, ENET_MII_TXD1, ENET_RMII_TXD1, I2C1_TXFRAME |
| PB14 | 75 | I/O | 5VT | Default: PB14<br>Alternate1: SHRTIMER_ST3CH0, I2S1_ADD_SD<br>Alternate2: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0(4) |
| PB15 | 76 | I/O | 5VT | Default: PB15<br>Alternate1: SHRTIMER_ST3CH1<br>Alternate2: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1(4), WKUP6, CMP5_IM7 |
| PD8 | 77 | I/O | 5VT | Default: PD8<br>Alternate2: EXMC_D13<br>Remap: USART2_TX, ENET_MII_RX_DV, ENET_RMII_CRS_DV |
| PD9 | 78 | I/O | 5VT | Default: PD9<br>Alternate2: EXMC_D14<br>Remap: USART2_RX, ENET_MII_RXD0, ENET_RMII_RXD0 |

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PD10 | 79 | I/O | 5VT | Default: PD10<br>Alternate2: EXMC_D15<br>Remap: USART2_CK, ENET_MII_RXD1, ENET_RMII_RXD1 |
| PD11 | 80 | I/O | 5VT | Default: PD11<br>Alternate2: EXMC_A16/EXMC_CLE<br>Remap: USART2_CTS, ENET_MII_RXD2 |
| PD12 | 81 | I/O | 5VT | Default: PD12<br>Alternate2: EXMC_A17/EXMC_ALE<br>Remap: TIMER3_CH0, USART2_RTS, ENET_MII_RXD3 |
| PD13 | 82 | I/O | 5VT | Default: PD13<br>Alternate2: EXMC_A18<br>Remap: TIMER3_CH1 |
| VSS_8 | 83 | P | | Default: VSS_8 |
| VDD_8 | 84 | P | | Default: VDD_8 |
| PD14 | 85 | I/O | 5VT | Default: PD14<br>Alternate2: EXMC_D0<br>Remap: TIMER3_CH2 |
| PD15 | 86 | I/O | 5VT | Default: PD15<br>Alternate2: EXMC_D1<br>Remap: TIMER3_CH3, CTC_SYNC |
| PG2 | 87 | I/O | 5VT | Default: PG2<br>Alternate2: EXMC_A12 |
| PG3 | 88 | I/O | 5VT | Default: PG3<br>Alternate2: EXMC_A13 |
| PG4 | 89 | I/O | 5VT | Default: PG4<br>Alternate2: EXMC_A14, SQPI_CSN |
| PG5 | 90 | I/O | 5VT | Default: PG5<br>Alternate2: EXMC_A15 |
| PG6 | 91 | I/O | 5VT | Default: PG6<br>Alternate1: SHRTIMER_ST4CH0<br>Alternate2: EXMC_INT1, SQPI_D1 |
| PG7 | 92 | I/O | 5VT | Default: PG7<br>Alternate1: SHRTIMER_ST4CH1, USART5_CK<br>Alternate2: EXMC_INT2 |
| PG8 | 93 | I/O | 5VT | Default: PG8<br>Alternate2: SQPI_D2 |
| VSS_9 | 94 | P | | Default: VSS_9 |
| VDD_9 | 95 | P | | Default: VDD_9 |
| PC6 | 96 | I/O | 5VT | Default: PC6<br>Alternate1: SHRTIMER_EXEV9, CMP5_OUT, USART5_TX<br>Alternate2: I2S1_MCK, TIMER7_CH0<br>Remap: TIMER2_CH0 |

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PC7 | 97 | I/O | 5VT | Default: PC7<br>Alternate1: SHRTIMER_FLT4, USART5_RX<br>Alternate2: I2S2_MCK, TIMER7_CH1<br>Remap: TIMER2_CH1 |
| PC8 | 98 | I/O | 5VT | Default: PC8<br>Alternate1: SHRTIMER_ST4CH0, USART5_CK<br>Alternate2: TIMER7_CH2<br>Remap: TIMER2_CH2 |
| PC9 | 99 | I/O | 5VT | Default: PC9<br>Alternate1: SHRTIMER_ST4CH1, I2C2_SDA<br>Alternate2: TIMER7_CH3<br>Remap: TIMER2_CH3 |
| PA8 | 100 | I/O | 5VT | Default: PA8<br>Alternate1: SHRTIMER_ST0CH0, I2C2_SCL<br>Alternate2: USART0_CK, TIMER0_CH0, CK_OUT, USBHS_SOF, CTC_SYNC |
| PA9 | 101 | I/O | 5VT | Default: PA9<br>Alternate1: CAN2_RX, SHRTIMER_ST0CH1, I2C2_SMBA<br>Alternate2: USART0_TX, TIMER0_CH1, USBHS_VBUS |
| PA10 | 102 | I/O | 5VT | Default: PA10<br>Alternate1: CAN2_TX, CMP5_OUT, SHRTIMER_ST1CH0<br>Alternate2: USART0_RX, TIMER0_CH2, USBHS_ID |
| PA11 | 103 | I/O | | Default: PA11<br>Alternate1: SHRTIMER_ST1CH1, USART5_TX<br>Alternate2: USART0_CTS, CAN0_RX, TIMER0_CH3, USBHS_DM |
| PA12 | 104 | I/O | | Default: PA12<br>Alternate1: CMP1_OUT, SHRTIMER_FLT0, USART5_RX<br>Alternate2: USART0_RTS, CAN0_TX, TIMER0_ETI, USBHS_DP |
| PA13 | 105 | I/O | 5VT | Default: JTMS, SWDIO<br>Remap: PA13 |
| NC | 106 | | | - |
| VSS_2 | 107 | P | | Default: VSS_2 |
| VDD_2 | 108 | P | | Default: VDD_2 |
| PA14 | 109 | I/O | 5VT | Default: JTCK, SWCLK<br>Remap: PA14 |
| PA15 | 110 | I/O | 5VT | Default: JTDI<br>Alternate1: SHRTIMER_FLT1<br>Alternate2: SPI2_NSS, I2S2_WS<br>Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PC10 | 111 | I/O | 5VT | Default: PC10<br>Alternate1: I2C2_SCL<br>Alternate2: UART3_TX<br>Remap: USART2_TX, SPI2_SCK, I2S2_CK |
| PC11 | 112 | I/O | 5VT | Default: PC11<br>Alternate1: SHRTIMER_EXEV1, I2S2_ADD_SD<br>Alternate2: UART3_RX<br>Remap: USART2_RX, SPI2_MISO |
| PC12 | 113 | I/O | 5VT | Default: PC12<br>Alternate1: SHRTIMER_EXEV0<br>Alternate2: UART4_TX<br>Remap: USART2_CK, SPI2_MOSI, I2S2_SD |
| PD0 | 114 | I/O | 5VT | Default: PD0<br>Alternate2: EXMC_D2<br>Remap: CAN0_RX |
| PD1 | 115 | I/O | 5VT | Default: PD1<br>Alternate2: EXMC_D3<br>Remap: CAN0_TX |
| PD2 | 116 | I/O | 5VT | Default: PD2<br>Alternate2: TIMER2_ETI, UART4_RX |
| PD3 | 117 | I/O | 5VT | Default: PD3<br>Alternate2: EXMC_CLK<br>Remap: USART1_CTS |
| PD4 | 118 | I/O | 5VT | Default: PD4<br>Alternate1: SHRTIMER_FLT2<br>Alternate2: EXMC_NOE<br>Remap: USART1_RTS |
| PD5 | 119 | I/O | 5VT | Default: PD5<br>Alternate1: SHRTIMER_EXEV2<br>Alternate2: EXMC_NWE<br>Remap: USART1_TX |
| VSS_10 | 120 | | | Default: VSS_10 |
| VDD_10 | 121 | | | Default: VDD_10 |
| PD6 | 122 | I/O | 5VT | Default: PD6<br>Alternate2: EXMC_NWAIT<br>Remap: USART1_RX |
| PD7 | 123 | I/O | 5VT | Default: PD7<br>Alternate2: EXMC_NE0, EXMC_NCE1<br>Remap: USART1_CK |
| PG9 | 124 | I/O | 5VT | Default: PG9<br>Alternate1: USART5_RX<br>Alternate2: EXMC_NE1, EXMC_NCE2 |
| PG10 | 125 | I/O | 5VT | Default: PG10<br>Alternate1: SHRTIMER_FLT4<br>Alternate2: EXMC_NCE3_0, EXMC_NE2 |

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PG11 | 126 | I/O | 5VT | Default: PG11<br>Alternate1: SHRTIMER_EXEV3<br>Alternate2: EXMC_NCE3_1 |
| PG12 | 127 | I/O | 5VT | Default: PG12<br>Alternate1: SHRTIMER_EXEV4<br>Alternate2: EXMC_NE3 |
| PG13 | 128 | I/O | 5VT | Default: PG13<br>Alternate1: SHRTIMER_EXEV9<br>Alternate2: EXMC_A24 |
| PG14 | 129 | I/O | 5VT | Default: PG14<br>Alternate1: USART5_TX<br>Alternate2: EXMC_A25 |
| VSS_11 | 130 | P | | Default: VSS_11 |
| VDD_11 | 131 | P | | Default: VDD_11 |
| PG15 | 132 | I/O | 5VT | Default: PG15 |
| PB3 | 133 | I/O | 5VT | Default: JTDO<br>Alternate1: SHRTIMER_SCOUT, SHRTIMER_EXEV8<br>Alternate2: SPI2_SCK, I2S2_CK<br>Remap: TIMER1_CH1, PB3, SPI0_SCK, TRACESWO |
| PB4 | 134 | I/O | 5VT | Default: NJTRST<br>Alternate1: SHRTIMER_EXEV6, I2C2_SDA, I2S2_ADD_SD<br>Alternate2: SPI2_MISO, I2C0_TXFRAME<br>Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 135 | I/O | | Default: PB5<br>Alternate1: USBHS_ULPI_D7, SHRTIMER_EXEV5, I2C2_SCL<br>Alternate2: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ENET_MII_PPS_OUT, ENET_RMII_PPS_OUT, WKUP5<br>Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX |
| PB6 | 136 | I/O | 5VT | Default: PB6<br>Alternate1: SHRTIMER_SCIN, SHRTIMER_EXEV3<br>Alternate2: I2C0_SCL, TIMER3_CH0<br>Remap: USART0_TX, CAN1_TX, SPI0_IO2 |
| PB7 | 137 | I/O | 5VT | Default: PB7<br>Alternate1: SHRTIMER_EXEV2<br>Alternate2: I2C0_SDA , TIMER3_CH1, EXMC_NADV<br>Remap: USART0_RX, SPI0_IO3 |
| BOOT0 | 138 | I | | Default: BOOT0 |
| PB8 | 139 | I/O | 5VT | Default: PB8<br>Alternate1: SHRTIMER_EXEV7, I2C2_SDA<br>Alternate2: TIMER3_CH2, TIMER9_CH0(4), ENET_MII_TXD3<br>Remap: I2C0_SCL, CAN0_RX |

| GD32E507Zx LQFP144 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PB9 | 140 | I/O | 5VT | Default: PB9<br>Alternate1: CMP1_OUT, SHRTIMER_EXEV4<br>Alternate2: TIMER3_CH3, TIMER10_CH0(4)<br>Remap: I2C0_SDA, CAN0_TX |
| PE0 | 141 | I/O | 5VT | Default: PE0<br>Alternate1: CAN2_RX, SHRTIMER_SCIN<br>Alternate2: TIMER3_ETI, EXMC_NBL0 |
| PE1 | 142 | I/O | 5VT | Default: PE1<br>Alternate1: CAN2_TX, SHRTIMER_SCOUT<br>Alternate2: EXMC_NBL1 |
| VSS_3 | 143 | P | | Default: VSS_3 |
| VDD_3 | 144 | P | | Default: VDD_3 |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Alternate1: The specified function can be mapped to the specific pin by configuring AFIO_PCFA ~ AFIO_PCFG registers.

Alternate2: These functions can be enabled with correct GPIO and function module mode configurations.

Remap: A group of the specified module functions can be mapped to the specified pins by configuring AFIO_PCF0 ~ AFIO_PCF1 registers.

(4) Functions are available in GD32E507ZE devices.

### 2.6.2. GD32E507Vx LQFP100 pin definitions

**Table 2-4. GD32E507Vx LQFP100 pin definitions**

| GD32E507Vx LQFP100 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PE2 | 1 | I/O | 5VT | Default: PE2<br>Alternate2: EXMC_A23 |
| PE3 | 2 | I/O | 5VT | Default: PE3<br>Alternate2: EXMC_A19 |
| PE4 | 3 | I/O | 5VT | Default: PE4<br>Alternate2: EXMC_A20 |
| PE5 | 4 | I/O | 5VT | Default: PE5<br>Alternate2: EXMC_A21<br>Remap: TIMER8_CH0(4) |
| PE6 | 5 | I/O | 5VT | Default: PE6<br>Alternate2: EXMC_A22, WKUP2<br>Remap: TIMER8_CH1(4) |
| VBAT | 6 | P | | Default: VBAT |
| PC13-TAMPER-RTC | 7 | I/O | | Default: PC13<br>Alternate2: TAMPER-RTC, WKUP1 |
| PC14-OSC32IN | 8 | I/O | | Default: PC14<br>Alternate2: OSC32IN |
| PC15-OSC32OUT | 9 | I/O | | Default: PC15<br>Alternate2: OSC32OUT |
| VSS_5 | 10 | P | | Default: VSS_5 |
| VDD_5 | 11 | P | | Default: VDD_5 |
| OSCIN-PD0 | 12 | I | | Default: OSCIN<br>Remap: PD0 |
| OSCOUT-PD1 | 13 | O | | Default: OSCOUT<br>Remap: PD1 |
| NRST | 14 | I/O | | Default: NRST |
| PC0 | 15 | I/O | | Default: PC0<br>Alternate1: USBHS_ULPI_STP<br>Alternate2: ADC01_IN10 |
| PC1 | 16 | I/O | | Default: PC1<br>Alternate2: ADC01_IN11, ENET_MII_MDC, ENET_RMII_MDC |
| PC2 | 17 | I/O | | Default: PC2<br>Alternate1: USBHS_ULPI_DIR, I2S1_ADD_SD<br>Alternate2: ADC01_IN12, ENET_MII_TXD2 |
| PC3 | 18 | I/O | | Default: PC3<br>Alternate1: USBHS_ULPI_NXT<br>Alternate2: ADC01_IN13, ENET_MII_TX_CLK |
| VSSA | 19 | P | | Default: VSSA |
| VREFN | 20 | P | | Default: VREFN |

| GD32E507Vx LQFP100 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| VREFP | 21 | P | | Default: VREFP |
| VDDA | 22 | P | | Default: VDDA |
| PA0-WKUP | 23 | I/O | | Default: PA0<br>Alternate2: WKUP0, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI(4), ENET_MII_CRS |
| PA1 | 24 | I/O | | Default: PA1<br>Alternate2: USART1_RTS, ADC01_IN1, TIMER4_CH1, TIMER1_CH1, ENET_MII_RX_CLK, ENET_RMII_REF_CLK |
| PA2 | 25 | I/O | | Default: PA2<br>Alternate1: CMP1_OUT<br>Alternate2: USART1_TX, TIMER4_CH2, ADC01_IN2, TIMER8_CH0(4), TIMER1_CH2, ENET_MII_MDIO, ENET_RMII_MDIO, SPI0_IO2, WKUP3, CMP1_IM6 |
| PA3 | 26 | I/O | | Default: PA3<br>Alternate1: USBHS_ULPI_D0<br>Alternate2: USART1_RX, TIMER4_CH3, ADC01_IN3, TIMER1_CH3, TIMER8_CH1(4), ENET_MII_COL, SPI0_IO3 |
| VSS_4 | 27 | P | | Default: VSS_4 |
| VDD_4 | 28 | P | | Default: VDD_4 |
| PA4 | 29 | I/O | | Default: PA4<br>Alternate2: SPI0_NSS, USART1_CK, DAC0_OUT0, ADC01_IN4, CMP1_IM4, CMP3_IM4, CMP5_IM4<br>Remap: SPI2_NSS, I2S2_WS |
| PA5 | 30 | I/O | | Default: PA5<br>Alternate1: USBHS_ULPI_CK<br>Alternate2: SPI0_SCK, ADC01_IN5, DAC0_OUT1, CMP1_IM5, CMP3_IM5, CMP5_IM5 |
| PA6 | 31 | I/O | | Default: PA6<br>Alternate2: SPI0_MISO, TIMER7_BRKIN(4), ADC01_IN6, TIMER2_CH0, TIMER12_CH0(4)<br>Remap: TIMER0_BRKIN |
| PA7 | 32 | I/O | | Default: PA7<br>Alternate2: SPI0_MOSI, TIMER7_CH0_ON(4), ADC01_IN7, TIMER2_CH1, TIMER13_CH0(4), ENET_MII_RX_DV, ENET_RMII_CRS_DV, CMP1_IP<br>Remap: TIMER0_CH0_ON |
| PC4 | 33 | I/O | | Default: PC4<br>Alternate2: ADC01_IN14, ENET_MII_RXD0, ENET_RMII_RXD0 |
| PC5 | 34 | I/O | | Default: PC5<br>Alternate2: ADC01_IN15, ENET_MII_RXD1, ENET_RMII_RXD1, WKUP4 |

| GD32E507Vx LQFP100 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PB0 | 35 | I/O | | Default: PB0<br>Alternate1: USBHS_ULPI_D1<br>Alternate2: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON(4), ENET_MII_RXD2, CMP3_IP<br>Remap: TIMER0_CH1_ON |
| PB1 | 36 | I/O | | Default: PB1<br>Alternate1: CMP3_OUT, USBHS_ULPI_D2, SHRTIMER_SCOUT<br>Alternate2: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON(4), ENET_MII_RXD3<br>Remap: TIMER0_CH2_ON |
| PB2 | 37 | I/O | 5VT | Default: PB2, BOOT1<br>Alternate1: USBHS_ULPI_D4, SHRTIMER_SCIN<br>Alternate2: CMP3_IM7 |
| PE7 | 38 | I/O | 5VT | Default: PE7<br>Alternate2: EXMC_D4<br>Remap: TIMER0_ETI |
| PE8 | 39 | I/O | 5VT | Default: PE8<br>Alternate1: CMP1_OUT<br>Alternate2: EXMC_D5<br>Remap: TIMER0_CH0_ON |
| PE9 | 40 | I/O | 5VT | Default: PE9<br>Alternate1: CMP3_OUT<br>Alternate2: EXMC_D6<br>Remap: TIMER0_CH0 |
| PE10 | 41 | I/O | 5VT | Default: PE10<br>Alternate1: CMP5_OUT<br>Alternate2: EXMC_D7<br>Remap: TIMER0_CH1_ON |
| PE11 | 42 | I/O | 5VT | Default: PE11<br>Alternate1: CMP5_OUT<br>Alternate2: EXMC_D8<br>Remap: TIMER0_CH1 |
| PE12 | 43 | I/O | 5VT | Default: PE12<br>Alternate1: CMP3_OUT<br>Alternate2: EXMC_D9<br>Remap: TIMER0_CH2_ON |
| PE13 | 44 | I/O | 5VT | Default: PE13<br>Alternate1: CMP1_OUT<br>Alternate2: EXMC_D10<br>Remap: TIMER0_CH2 |
| PE14 | 45 | I/O | 5VT | Default: PE14<br>Alternate2: EXMC_D11<br>Remap: TIMER0_CH3 |
| PE15 | 46 | I/O | 5VT | Default: PE15 |

| GD32E507Vx LQFP100 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Alternate2: EXMC_D12<br>Remap: TIMER0_BRKIN |
| PB10 | 47 | I/O | 5VT | Default: PB10<br>Alternate1: CAN2_RX, USBHS_ULPI_D3, SHRTIMER_FLT2<br>Alternate2: I2C1_SCL, USART2_TX, ENET_MII_RX_ER<br>Remap: TIMER1_CH2 |
| PB11 | 48 | I/O | 5VT | Default: PB11<br>Alternate1: CAN2_TX, USBHS_ULPI_D4, SHRTIMER_FLT3<br>Alternate2: I2C1_SDA, USART2_RX, ENET_MII_TX_EN, ENET_RMII_TX_EN, CMP5_IP<br>Remap: TIMER1_CH3 |
| VSS_1 | 49 | P | | Default: VSS_1 |
| VDD_1 | 50 | P | | Default: VDD_1 |
| PB12 | 51 | I/O | 5VT | Default: PB12<br>Alternate1: USBHS_ULPI_D5, SHRTIMER_ST2CH0<br>Alternate2: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, CAN1_RX, ENET_MII_TXD0, ENET_RMII_TXD0 |
| PB13 | 52 | I/O | 5VT | Default: PB13<br>Alternate1: USBHS_ULPI_D6, SHRTIMER_ST2CH1<br>Alternate2: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, CAN1_TX, ENET_MII_TXD1, ENET_RMII_TXD1, I2C1_TXFRAME |
| PB14 | 53 | I/O | 5VT | Default: PB14<br>Alternate1: SHRTIMER_ST3CH0, I2S1_ADD_SD<br>Alternate2: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0(4) |
| PB15 | 54 | I/O | 5VT | Default: PB15<br>Alternate1: SHRTIMER_ST3CH1<br>Alternate2: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1(4), WKUP6, CMP5_IM7 |
| PD8 | 55 | I/O | 5VT | Default: PD8<br>Alternate2: EXMC_D13<br>Remap: USART2_TX, ENET_MII_RX_DV, ENET_RMII_CRS_DV |
| PD9 | 56 | I/O | 5VT | Default: PD9<br>Alternate2: EXMC_D14<br>Remap: USART2_RX, ENET_MII_RXD0, ENET_RMII_RXD0 |
| PD10 | 57 | I/O | 5VT | Default: PD10<br>Alternate2: EXMC_D15<br>Remap: USART2_CK, ENET_MII_RXD1, ENET_RMII_RXD1 |

| GD32E507Vx LQFP100 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| PD11 | 58 | I/O | 5VT | Default: PD11<br>Alternate2: EXMC_A16/EXMC_CLE<br>Remap: USART2_CTS, ENET_MII_RXD2 |
| PD12 | 59 | I/O | 5VT | Default: PD12<br>Alternate2: EXMC_A17/EXMC_ALE<br>Remap: TIMER3_CH0, USART2_RTS, ENET_MII_RXD3 |
| PD13 | 60 | I/O | 5VT | Default: PD13<br>Alternate2: EXMC_A18<br>Remap: TIMER3_CH1 |
| PD14 | 61 | I/O | 5VT | Default: PD14<br>Alternate2: EXMC_D0<br>Remap: TIMER3_CH2 |
| PD15 | 62 | I/O | 5VT | Default: PD15<br>Alternate2: EXMC_D1<br>Remap: TIMER3_CH3, CTC_SYNC |
| PC6 | 63 | I/O | 5VT | Default: PC6<br>Alternate1: SHRTIMER_EXEV9, CMP5_OUT, USART5_TX<br>Alternate2: I2S1_MCK, TIMER7_CH0(4)<br>Remap: TIMER2_CH0 |
| PC7 | 64 | I/O | 5VT | Default: PC7<br>Alternate1: SHRTIMER_FLT4, USART5_RX<br>Alternate2: I2S2_MCK, TIMER7_CH1(4)<br>Remap: TIMER2_CH1 |
| PC8 | 65 | I/O | 5VT | Default: PC8<br>Alternate1: SHRTIMER_ST4CH0, USART5_CK<br>Alternate2: TIMER7_CH2(4)<br>Remap: TIMER2_CH2 |
| PC9 | 66 | I/O | 5VT | Default: PC9<br>Alternate1: SHRTIMER_ST4CH1, I2C2_SDA<br>Alternate2: TIMER7_CH3(4)<br>Remap: TIMER2_CH3 |
| PA8 | 67 | I/O | 5VT | Default: PA8<br>Alternate1: SHRTIMER_ST0CH0, I2C2_SCL<br>Alternate2: USART0_CK, TIMER0_CH0, CK_OUT, USBHS_SOF, CTC_SYNC |
| PA9 | 68 | I/O | 5VT | Default: PA9<br>Alternate1: CAN2_RX, SHRTIMER_ST0CH1, I2C2_SMBA<br>Alternate2: USART0_TX, TIMER0_CH1, USBHS_VBUS |
| PA10 | 69 | I/O | 5VT | Default: PA10<br>Alternate1: CAN2_TX, CMP5_OUT, SHRTIMER_ST1CH0<br>Alternate2: USART0_RX, TIMER0_CH2, USBHS_ID |
| PA11 | 70 | I/O | | Default: PA11 |

| GD32E507Vx LQFP100 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Alternate1: SHRTIMER_ST1CH1, USART5_TX<br>Alternate2: USART0_CTS, CAN0_RX, TIMER0_CH3, USBHS_DM |
| PA12 | 71 | I/O | | Default: PA12<br>Alternate1: CMP1_OUT, SHRTIMER_FLT0, USART5_RX<br>Alternate2: USART0_RTS, CAN0_TX, TIMER0_ETI, USBHS_DP |
| PA13 | 72 | I/O | 5VT | Default: JTMS, SWDIO<br>Remap: PA13 |
| NC | 73 | | | - |
| VSS_2 | 74 | P | | Default: VSS_2 |
| VDD_2 | 75 | P | | Default: VDD_2 |
| PA14 | 76 | I/O | 5VT | Default: JTCK, SWCLK<br>Remap: PA14 |
| PA15 | 77 | I/O | 5VT | Default: JTDI<br>Alternate1: SHRTIMER_FLT1<br>Alternate2: SPI2_NSS, I2S2_WS<br>Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 78 | I/O | 5VT | Default: PC10<br>Alternate1: I2C2_SCL<br>Alternate2: UART3_TX<br>Remap: USART2_TX, SPI2_SCK, I2S2_CK |
| PC11 | 79 | I/O | 5VT | Default: PC11<br>Alternate1: SHRTIMER_EXEV1, I2S2_ADD_SD<br>Alternate2: UART3_RX<br>Remap: USART2_RX, SPI2_MISO |
| PC12 | 80 | I/O | 5VT | Default: PC12<br>Alternate1: SHRTIMER_EXEV0<br>Alternate2: UART4_TX<br>Remap: USART2_CK, SPI2_MOSI, I2S2_SD |
| PD0 | 81 | I/O | 5VT | Default: PD0<br>Alternate2: EXMC_D2<br>Remap: CAN0_RX |
| PD1 | 82 | I/O | 5VT | Default: PD1<br>Alternate2: EXMC_D3<br>Remap: CAN0_TX |
| PD2 | 83 | I/O | 5VT | Default: PD2<br>Alternate2: TIMER2_ETI, UART4_RX |
| PD3 | 84 | I/O | 5VT | Default: PD3<br>Alternate2: EXMC_CLK<br>Remap: USART1_CTS |
| PD4 | 85 | I/O | 5VT | Default: PD4<br>Alternate1: SHRTIMER_FLT2<br>Alternate2: EXMC_NOE |

| GD32E507Vx LQFP100 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Remap: USART1_RTS |
| PD5 | 86 | I/O | 5VT | Default: PD5<br>Alternate1: SHRTIMER_EXEV2<br>Alternate2: EXMC_NWE<br>Remap: USART1_TX |
| PD6 | 87 | I/O | 5VT | Default: PD6<br>Alternate2: EXMC_NWAIT<br>Remap: USART1_RX |
| PD7 | 88 | I/O | 5VT | Default: PD7<br>Alternate2: EXMC_NE0, EXMC_NCE1<br>Remap: USART1_CK |
| PB3 | 89 | I/O | 5VT | Default: JTDO<br>Alternate1: SHRTIMER_SCOUT, SHRTIMER_EXEV8<br>Alternate2: SPI2_SCK, I2S2_CK<br>Remap: TIMER1_CH1, PB3, SPI0_SCK, TRACESWO |
| PB4 | 90 | I/O | 5VT | Default: NJTRST<br>Alternate1: SHRTIMER_EXEV6, I2C2_SDA,<br>I2S2_ADD_SD<br>Alternate2: SPI2_MISO, I2C0_TXFRAME<br>Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 91 | I/O | | Default: PB5<br>Alternate1: USBHS_ULPI_D7, SHRTIMER_EXEV5,<br>I2C2_SCL<br>Alternate2: I2C0_SMBA, SPI2_MOSI, I2S2_SD,<br>ENET_MII_PPS_OUT, ENET_RMII_PPS_OUT, WKUP5<br>Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX |
| PB6 | 92 | I/O | 5VT | Default: PB6<br>Alternate1: SHRTIMER_SCIN, SHRTIMER_EXEV3<br>Alternate2: I2C0_SCL, TIMER3_CH0<br>Remap: USART0_TX, CAN1_TX, SPI0_IO2 |
| PB7 | 93 | I/O | 5VT | Default: PB7<br>Alternate1: SHRTIMER_EXEV2<br>Alternate2: I2C0_SDA , TIMER3_CH1, EXMC_NADV<br>Remap: USART0_RX, SPI0_IO3 |
| BOOT0 | 94 | I | | Default: BOOT0 |
| PB8 | 95 | I/O | 5VT | Default: PB8<br>Alternate1: SHRTIMER_EXEV7, I2C2_SDA<br>Alternate2: TIMER3_CH2, TIMER9_CH0(4),<br>ENET_MII_TXD3<br>Remap: I2C0_SCL, CAN0_RX |
| PB9 | 96 | I/O | 5VT | Default: PB9<br>Alternate1: CMP1_OUT, SHRTIMER_EXEV4<br>Alternate2: TIMER3_CH3, TIMER10_CH0(4)<br>Remap: I2C0_SDA, CAN0_TX |
| PE0 | 97 | I/O | 5VT | Default: PE0 |

| GD32E507Vx LQFP100 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Alternate1: CAN2_RX, SHRTIMER_SCIN<br>Alternate2: TIMER3_ETI, EXMC_NBL0 |
| PE1 | 98 | I/O | 5VT | Default: PE1<br>Alternate1: CAN2_TX, SHRTIMER_SCOUT<br>Alternate2: EXMC_NBL1 |
| VSS_3 | 99 | P | | Default: VSS_3 |
| VDD_3 | 100 | P | | Default: VDD_3 |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Alternate1: The specified function can be mapped to the specific pin by configuring AFIO_PCFA ~ AFIO_PCFG registers.

Alternate2: These functions can be enabled with correct GPIO and function module mode configurations.

Remap: A group of the specified module functions can be mapped to the specified pins by configuring AFIO_PCF0 ~ AFIO_PCF1 registers.

(4) Functions are available in GD32E507VE devices.

### 2.6.3. GD32E507Rx LQFP64 pin definitions

**Table 2-5. GD32E507Rx LQFP64 pin definitions**

| GD32E507Rx LQFP64 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| VBAT | 1 | P | | Default: VBAT |
| PC13-TAMPER-RTC | 2 | I/O | | Default: PC13<br>Alternate2: TAMPER-RTC, WKUP1 |
| PC14-OSC32IN | 3 | I/O | | Default: PC14<br>Alternate2: OSC32IN |
| PC15-OSC32OUT | 4 | I/O | | Default: PC15<br>Alternate2: OSC32OUT |
| OSCIN-PD0 | 5 | I/O | | Default: OSCIN<br>Remap: PD0 |
| OSCOUT-PD1 | 6 | I/O | | Default: OSCOUT<br>Remap: PD1 |
| NRST | 7 | I/O | | Default: NRST |
| PC0 | 8 | I/O | | Default: PC0<br>Alternate1: USBHS_ULPI_STP<br>Alternate2: ADC01_IN10 |
| PC1 | 9 | I/O | | Default: PC1<br>Alternate2: ADC01_IN11, ENET_MII_MDC, ENET_RMII_MDC |
| PC2 | 10 | I/O | | Default: PC2<br>Alternate1: USBHS_ULPI_DIR, I2S1_ADD_SD<br>Alternate2: ADC01_IN12, ENET_MII_TXD2 |
| PC3 | 11 | I/O | | Default: PC3<br>Alternate1: USBHS_ULPI_NXT<br>Alternate2: ADC01_IN13, ENET_MII_TX_CLK |
| VSSA | 12 | P | | Default: VSSA |
| VDDA | 13 | P | | Default: VDDA |
| PA0-WKUP | 14 | I/O | | Default: PA0<br>Alternate2: WKUP0, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI(4), ENET_MII_CRS |
| PA1 | 15 | I/O | | Default: PA1<br>Alternate2: USART1_RTS, ADC01_IN1, TIMER4_CH1, TIMER1_CH1, ENET_MII_RX_CLK, ENET_RMII_REF_CLK |
| PA2 | 16 | I/O | | Default: PA2<br>Alternate1: CMP1_OUT<br>Alternate2: USART1_TX, TIMER4_CH2, ADC01_IN2, TIMER8_CH0(4), TIMER1_CH2, ENET_MII_MDIO, ENET_RMII_MDIO, SPI0_IO2, WKUP3, CMP1_IM6 |
| PA3 | 17 | I/O | | Default: PA3 |

| GD32E507Rx LQFP64 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Alternate1: USBHS_ULPI_D0<br>Alternate2: USART1_RX, TIMER4_CH3, ADC01_IN3, TIMER1_CH3, TIMER8_CH1(4), ENET_MII_COL, SPI0_IO3 |
| VSS_4 | 18 | P | | Default: VSS_4 |
| VDD_4 | 19 | P | | Default: VDD_4 |
| PA4 | 20 | I/O | | Default: PA4<br>Alternate2: SPI0_NSS, USART1_CK, DAC0_OUT0, ADC01_IN4, CMP1_IM4, CMP3_IM4, CMP5_IM4<br>Remap: SPI2_NSS, I2S2_WS |
| PA5 | 21 | I/O | | Default: PA5<br>Alternate1: USBHS_ULPI_CK<br>Alternate2: SPI0_SCK, ADC01_IN5, DAC0_OUT1, CMP1_IM5, CMP3_IM5, CMP5_IM5 |
| PA6 | 22 | I/O | | Default: PA6<br>Alternate2: SPI0_MISO, TIMER7_BRKIN(4), ADC01_IN6, TIMER2_CH0, TIMER12_CH0(4)<br>Remap: TIMER0_BRKIN |
| PA7 | 23 | I/O | | Default: PA7<br>Alternate2: SPI0_MOSI, TIMER7_CH0_ON(4), ADC01_IN7, TIMER2_CH1, TIMER13_CH0(4), ENET_MII_RX_DV, ENET_RMII_CRS_DV, CMP1_IP<br>Remap: TIMER0_CH0_ON |
| PC4 | 24 | I/O | | Default: PC4<br>Alternate2: ADC01_IN14, ENET_MII_RXD0, ENET_RMII_RXD0 |
| PC5 | 25 | I/O | | Default: PC5<br>Alternate2: ADC01_IN15, ENET_MII_RXD1, ENET_RMII_RXD1, WKUP4 |
| PB0 | 26 | I/O | | Default: PB0<br>Alternate1: USBHS_ULPI_D1<br>Alternate2: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON(4), ENET_MII_RXD2, CMP3_IP<br>Remap: TIMER0_CH1_ON |
| PB1 | 27 | I/O | | Default: PB1<br>Alternate1: CMP3_OUT, USBHS_ULPI_D2, SHRTIMER_SCOUT<br>Alternate2: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON(4), ENET_MII_RXD3<br>Remap: TIMER0_CH2_ON |
| PB2 | 28 | I/O | 5VT | Default: PB2, BOOT1<br>Alternate1: USBHS_ULPI_D4, SHRTIMER_SCIN<br>Alternate2: CMP3_IM7 |
| PB10 | 29 | I/O | 5VT | Default: PB10 |

| GD32E507Rx LQFP64 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Alternate1: CAN2_RX, USBHS_ULPI_D3, SHRTIMER_FLT2<br>Alternate2: I2C1_SCL, USART2_TX, ENET_MII_RX_ER<br>Remap: TIMER1_CH2 |
| PB11 | 30 | I/O | 5VT | Default: PB11<br>Alternate1: CAN2_TX, USBHS_ULPI_D4, SHRTIMER_FLT3<br>Alternate2: I2C1_SDA, USART2_RX, ENET_MII_TX_EN, ENET_RMII_TX_EN, CMP5_IP<br>Remap: TIMER1_CH3 |
| VSS_1 | 31 | P | | Default: VSS_1 |
| VDD_1 | 32 | P | | Default: VDD_1 |
| PB12 | 33 | I/O | 5VT | Default: PB12<br>Alternate1: USBHS_ULPI_D5, SHRTIMER_ST2CH0<br>Alternate2: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, CAN1_RX, ENET_MII_TXD0, ENET_RMII_TXD0 |
| PB13 | 34 | I/O | 5VT | Default: PB13<br>Alternate1: USBHS_ULPI_D6, SHRTIMER_ST2CH1<br>Alternate2: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, CAN1_TX, ENET_MII_TXD1, ENET_RMII_TXD1, I2C1_TXFRAME |
| PB14 | 35 | I/O | 5VT | Default: PB14<br>Alternate1: SHRTIMER_ST3CH0, I2S1_ADD_SD<br>Alternate2: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0(4) |
| PB15 | 36 | I/O | 5VT | Default: PB15<br>Alternate1: SHRTIMER_ST3CH1<br>Alternate2: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1(4), WKUP6, CMP5_IM7 |
| PC6 | 37 | I/O | 5VT | Default: PC6<br>Alternate1: SHRTIMER_EXEV9, CMP5_OUT, USART5_TX<br>Alternate2: I2S1_MCK, TIMER7_CH0(4)<br>Remap: TIMER2_CH0 |
| PC7 | 38 | I/O | 5VT | Default: PC7<br>Alternate1: SHRTIMER_FLT4, USART5_RX<br>Alternate2: I2S2_MCK, TIMER7_CH1(4)<br>Remap: TIMER2_CH1 |
| PC8 | 39 | I/O | 5VT | Default: PC8<br>Alternate1: SHRTIMER_ST4CH0, USART5_CK<br>Alternate2: TIMER7_CH2(4)<br>Remap: TIMER2_CH2 |
| PC9 | 40 | I/O | 5VT | Default: PC9<br>Alternate1: SHRTIMER_ST4CH1, I2C2_SDA |

| GD32E507Rx LQFP64 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Alternate2: TIMER7_CH3(4)<br>Remap: TIMER2_CH3 |
| PA8 | 41 | I/O | 5VT | Default: PA8<br>Alternate1: SHRTIMER_ST0CH0, I2C2_SCL<br>Alternate2: USART0_CK, TIMER0_CH0, CK_OUT, USBHS_SOF, CTC_SYNC |
| PA9 | 42 | I/O | 5VT | Default: PA9<br>Alternate1: CAN2_RX, SHRTIMER_ST0CH1, I2C2_SMBA<br>Alternate2: USART0_TX, TIMER0_CH1, USBHS_VBUS |
| PA10 | 43 | I/O | 5VT | Default: PA10<br>Alternate1: CAN2_TX, CMP5_OUT, SHRTIMER_ST1CH0<br>Alternate2: USART0_RX, TIMER0_CH2, USBHS_ID |
| PA11 | 44 | I/O | | Default: PA11<br>Alternate1: SHRTIMER_ST1CH1, USART5_TX<br>Alternate2: USART0_CTS, CAN0_RX, TIMER0_CH3, USBHS_DM |
| PA12 | 45 | I/O | | Default: PA12<br>Alternate1: CMP1_OUT, SHRTIMER_FLT0, USART5_RX<br>Alternate2: USART0_RTS, CAN0_TX, TIMER0_ETI, USBHS_DP |
| PA13 | 46 | I/O | 5VT | Default: JTMS, SWDIO<br>Remap: PA13 |
| VSS_2 | 47 | P | | Default: VSS_2 |
| VDD_2 | 48 | P | | Default: VDD_2 |
| PA14 | 49 | I/O | 5VT | Default: JTCK, SWCLK<br>Remap: PA14 |
| PA15 | 50 | I/O | 5VT | Default: JTDI<br>Alternate1: SHRTIMER_FLT1<br>Alternate2: SPI2_NSS, I2S2_WS<br>Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 51 | I/O | 5VT | Default: PC10<br>Alternate1: I2C2_SCL<br>Alternate2: UART3_TX<br>Remap: USART2_TX, SPI2_SCK, I2S2_CK |
| PC11 | 52 | I/O | 5VT | Default: PC11<br>Alternate1: SHRTIMER_EXEV1, I2S2_ADD_SD<br>Alternate2: UART3_RX<br>Remap: USART2_RX, SPI2_MISO |
| PC12 | 53 | I/O | 5VT | Default: PC12<br>Alternate1: SHRTIMER_EXEV0<br>Alternate2: UART4_TX<br>Remap: USART2_CK, SPI2_MOSI, I2S2_SD |
| PD2 | 54 | I/O | 5VT | Default: PD2 |

| GD32E507Rx LQFP64 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description(3)** |
| | | | | Alternate2: TIMER2_ETI, UART4_RX |
| PB3 | 55 | I/O | 5VT | Default: JTDO<br>Alternate1: SHRTIMER_SCOUT, SHRTIMER_EXEV8<br>Alternate2: SPI2_SCK, I2S2_CK<br>Remap: TIMER1_CH1, PB3, SPI0_SCK, TRACESWO |
| PB4 | 56 | I/O | 5VT | Default: NJTRST<br>Alternate1: SHRTIMER_EXEV6, I2C2_SDA, I2S2_ADD_SD<br>Alternate2: SPI2_MISO, I2C0_TXFRAME<br>Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 57 | I/O | | Default: PB5<br>Alternate1: USBHS_ULPI_D7, SHRTIMER_EXEV5, I2C2_SCL<br>Alternate2: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ENET_MII_PPS_OUT, ENET_RMII_PPS_OUT, WKUP5<br>Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX |
| PB6 | 58 | I/O | 5VT | Default: PB6<br>Alternate1: SHRTIMER_SCIN, SHRTIMER_EXEV3<br>Alternate2: I2C0_SCL, TIMER3_CH0<br>Remap: USART0_TX, CAN1_TX, SPI0_IO2 |
| PB7 | 59 | I/O | 5VT | Default: PB7<br>Alternate1: SHRTIMER_EXEV2<br>Alternate2: I2C0_SDA , TIMER3_CH1<br>Remap: USART0_RX, SPI0_IO3 |
| BOOT0 | 60 | I | | Default: BOOT0 |
| PB8 | 61 | I/O | 5VT | Default: PB8<br>Alternate1: SHRTIMER_EXEV7, I2C2_SDA<br>Alternate2: TIMER3_CH2, TIMER9_CH0(4), ENET_MII_TXD3<br>Remap: I2C0_SCL, CAN0_RX |
| PB9 | 62 | I/O | 5VT | Default: PB9<br>Alternate1: CMP1_OUT, SHRTIMER_EXEV4<br>Alternate2: TIMER3_CH3, TIMER10_CH0(4)<br>Remap: I2C0_SDA, CAN0_TX |
| VSS_3 | 63 | P | | Default: VSS_3 |
| VDD_3 | 64 | P | | Default: VDD_3 |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Alternate1: The specified function can be mapped to the specific pin by configuring AFIO_PCFA ~ AFIO_PCFG registers.

Alternate2: These functions can be enabled with correct GPIO and function module mode configurations.

Remap: A group of the specified module functions can be mapped to the specified pins

by configuring AFIO_PCF0 ~ AFIO_PCF1 registers.

(4) Functions are available in GD32E507RE devices.

# 3. Functional description

## 3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption.

32-bit Arm® Cortex®-M33 processor core

- Up to 180 MHz operation frequency
- Ultra-low power, energy-efficient operation
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M33 processor is based on the ARMv8 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit (BPU)
- Data Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Memory Protection Unit (MPU)
- Floating Point Unit (FPU)
- DSP Extension (DSP)

## 3.2. Embedded memory

- Up to 512 Kbytes of Flash memory
- Up to 128 Kbytes of SRAM

512 Kbytes of inner Flash and 128 Kbytes of inner SRAM at most is available for storing programs and data, and Flash is accessed (Read) at CPU clock speed with 0~4 waiting time. *Table 2-2. GD32E507xx memory map* shows the memory map of the GD32E507xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

## 3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 1.71 to 3.63 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 180 MHz/180 MHz/90 MHz. See ***Figure 2-5. GD32E507xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.56 V and down to 1.52V. The device remains in reset mode when $V_{DD}$ is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- $V_{DD}$ range: 1.71 to 3.63 V, external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ range: 1.71 to 3.63 V, external analog power supplies for ADC, reset blocks, RCs and PLL.
- $V_{BAK}$ range: 1.71 to 3.63 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

## 3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PD5 and PD6) or USB (PA9, PA11 and PA12).

To ensure system reliability and stability, it is recommended not to connect peripherals that may generate interference signals (such as sensor outputs, watchdog chips, buttons, etc.) to the above-mentioned pins during the hardware design stage, in order to avoid affecting the

normal function of the Bootloader and causing abnormal outputs to the connected peripherals.

**Note:** When booting from system memory, the USART RX pins (PA10/ PD6) are in input level detection mode. Therefore, unused USART RX pins (PA10/PD6) need to be kept at a stable logic level to prevent false triggering.

## 3.5. Power saving modes

The MCU supports five kinds of power saving modes to achieve even lower power consumption. They are Sleep, Deep-sleep, Deep-sleep 1, Deep-sleep 2 and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the $V_{CORE}$ domain are off, and all of IRC8M, IRC48M, HXTAL and PLLs are disabled. The contents of SRAM and registers are preserved. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, LVD output, USB wakeup, Ethernet wakeup, I2C2 wakeup and USART5 wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Deep-sleep 1** mode
  In Deep-sleep 1 mode, all clocks in the $V_{CORE}$ domain are off, and all of IRC8M, IRC48M, HXTAL and PLLs are disabled. The power of COREOFF1 domain is cut off. The contents of registers in COREOFF1 domain are lost. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep 1 mode including the 16 external lines, the RTC alarm, LVD output, USB wakeup, Ethernet wakeup, I2C2 wakeup and USART5 wakeup. Waking up from Deep-sleep 1 mode needs an additional delay to power on COREOFF1 domain. When exiting the deep-sleep 1 mode, the IRC8M is selected as the system clock.
- **Deep-sleep 2** mode
  In Deep-sleep 2 mode, all clocks in the $V_{CORE}$ domain are off, and all of IRC8M, IRC48M, HXTAL and PLLs are disabled. The power of COREOFF0/COREOFF1 domain is cut off. The contents of SRAM except for the first 32K and registers in COREOFF0/COREOFF1 domain are lost. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, LVD output, USB wakeup, Ethernet wakeup, I2C2 wakeup and USART5 wakeup. Waking up from Deep-sleep 2 mode needs an additional delay to power on COREOFF1 domain. Waking up from Deep-sleep 2 mode needs an additional delay to power on COREOFF0/COREOFF1 domain. When exiting the deep-sleep 2 mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole $V_{CORE}$ domain is power off, the LDO is shut down, and all of

IRC8M, IRC48M, HXTAL and PLL are disabled. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pins.

## 3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.5 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: $V_{REF-}$ to $V_{REF+}$
- Temperature sensor

Two 12-bit 2.5 MSPS multi-channel ADCs are integrated in the device. It has a total of 18 multiplexed channels: up to 16 external channels, 1 channel for internal temperature sensor ($V_{SENSE}$) and 1 channel for internal reference voltage ($V_{REFINT}$). The input voltage range is between $V_{REF-}$ and $V_{REF+}$. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx), the advanced timers (TIMER0 and TIMER7) and SHRTIMER with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC and DAC, the ADC/DAC independent external reference voltage should be connected to $V_{REF+}$/$V_{REF-}$ pins. According to the different packages, $V_{REF+}$ pin can be connected to $V_{DDA}$ pin, or external reference voltage, $V_{REF-}$ pin must be connected to $V_{SSA}$ pin. The $V_{REF+}$ pin is only available on no less than 100-pin packages, or else the $V_{REF+}$ pin is not available and internally connected to $V_{DDA}$. The $V_{REF-}$ pin is only available on no less than 100-pin packages, or else the $V_{REF-}$ pin is not available and internally connected to $V_{SSA}$.

## 3.7. Digital to analog converter (DAC)

- Two 12-bit DACs with independent output channels
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC is used to generate variable analog outputs. The DAC channels can be triggered by the timer, SHRTIMER or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is $V_{REF+}$.

## 3.8. DMA

- 7 channels for DMA0 controller and 5 channels for DMA1 controller
- Peripherals supported: Timers, SHRTIMER, ADCs, DACs, SPIs, I2Cs, USARTs and I2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

## 3.9. General-purpose inputs/outputs (GPIOs)

- Up to 112 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 112 general purpose I/O pins (GPIO) in GD32E507xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15 and PG0 ~ PG15 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (Afs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

## 3.10. Timers and PWM generation

- Two 16-bit advanced timer (TIMER0, TIMER7), one 32-bit general timer (TIMER1), up to nine 16-bit general timers (TIMER2 ~ TIMER4, TIMER8 ~ TIMER13), and two 16-bit basic timer (TIMER5, TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0, TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center- aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIMER2 ~ TIMER4 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIMER8 ~ TIMER13 is based on a 16-bit auto-reload up counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 &TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32E507xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep, deep-sleep 1, deep-sleep 2 and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

## 3.11. Real time clock (RTC)

- 32-bit programmable counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wakeup event

The real time clock is an independent timer which provides a set of continuously running

counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

## 3.12. Inter-integrated circuit (I2C)

I2C0 and I2C1:

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- SMBus 2.0 and PMBus compatible
- Supports SAM_V mode

I2C2:

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- SMBus 3.0 and PMBus 1.3 compatible
- Wakeup from Deep-sleep mode on address match

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

## 3.13. Serial peripheral interface (SPI)

- Up to three SPI interfaces
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad-SPI configuration available in master mode (only in SPI0)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI0.

## 3.14. Universal synchronous asynchronous receiver transmitter (USART)

USART0~2, UART3~4:

- Maximum speed up to 22.5 Mbits/s for USART0
- Maximum speed up to 11.25 Mbits/s for USART1~2, UART3~4
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

USART5:

- Maximum speed up to 22.5 Mbits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface
- Dual clock domain
- Wake up from Deep-sleep mode

The USART (USART0, USART1, USART2, USART5) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

## 3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32E507xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequency from 8 KHz to 192 KHz is supported.

## 3.16. Universal serial bus High-Speed interface (USBHS)

- One USB device/host/OTG high-speed interface with frequency up to 480Mbit/s.
- Include a USB PHY with OTG protocol supported

USB High-Speed (USBHS) controller provides a USB-connection solution for portable devices. USBHS supports both host and device modes, as well as OTG mode with HNP (Host

Negotiation Protocol) and SRP (Session Request Protocol). USBHS contains an embedded USB PHY internal which can be configured as High-Speed or Full-Speed. USBHS supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system. For Full-Speed operation, battery charging detection (BCD), attach detection protocol (ADP), and link power management (LPM) are also supported.

## 3.17. Controller area network (CAN)

- Three CAN interfaces supports the CAN protocols version 2.0A and B, ISO11891-1:2015 specification with baud rates up to 1 Mbit/s when classical frames.

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three messages depth for reception. The CAN0 and CAN1 provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others. The CAN2 independently provides 14 scalable/configurable identifier filter banks in GD32E50x CL.

## 3.18. Ethernet (ENET)

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 16 with 25 MHz output and RMII up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

## 3.19. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and PC card
- Up to 16-bit data bus
- Support to interface with Motorola 6800 and Intel 8080 type LCD directly

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip

selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory except NAND Flash and PC card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

## 3.20. Comparators (CMP)

- Three fast rail-to-rail low-power comparators with software configurable
- Programmable reference voltage (internal or external I/O)

Three Comparators (CMP) are implemented within the devices. They can work either standalone (all terminal are available on I/Os) or together with the timers. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

## 3.21. Trigonometric Math Unit (TMU)

- Operation data support IEEE 32-Bit Single Precision Floating-Point Format

The Trigonometric Math Unit (TMU) is a fully configurable block that execute common trigonometric and arithmetic operations. The TMU calculation unit can be used to calculate total 9 kinds of operations. For mode 0 and 1, operation finishes in 4 clock cycles. For others mode, 7 clock cycles is needed.

## 3.22. Super High-Resolution Timer (SHRTIMER)

- High- precision timing units: Master_TIMER, Slave_TIMERx (x=0..4).
- Synchronization outputs: synchronize external resources as master.
- Synchronization inputs: be synchronized as a slaver.
- Bunch mode controller to handle light-load operation.
- 6 DMA request: Master_TIMER requests, Slave_TIMERx (x=0..4) requests.

SHRTIMER has a high-precision counting clock and can be used for high-precision timing. It can generate 10 high precision and flexible digital signals to control motor or be used for power management applications. It has multiple internal signals connected to the ADC and DAC. It can be used for control and monitoring purposes. It can handle various fault input for safe purposes.

## 3.23. Serial/Quad Parallel Interface (SQPI)

- SQPI controller support configuring output clock frequency which is divided by HCLK.
- SQPI controller support no address phase and data phase operation which is named special command by the controller.
- SQPI controller support 256MB external memory space.

Logic memory address range: 0xB000_0000 – 0xBFFF_FFFF.

- SQPI controller support 6 types mode for different combination of command, address, waitcycle, and data phase.

Serial/Quad Parallel Interface (SQPI) is a controller for external serial/dual/quad parallel interface memory peripheral. For example: SQPI-PSRAM and SQPI-FLASH. With this controller, users can use external SQPI interface memory as SRAM simply.

## 3.24. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

## 3.25. Package and operation temperature

- LQFP144 (GD32E507Zx), LQFP100 (GD32E507Vx) and LQFP64 (GD32E507Rx).
- Operation temperature range: -40°C to +85°C (industrial level)

# 4. Electrical characteristics

## 4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly over the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4-1. Absolute maximum ratings(1)(4)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | External voltage range(2) | $V_{SS}$ – 0.3 | $V_{SS}$ + 3.63 | V |
| $V_{DDA}$ | External analog supply voltage | $V_{SSA}$ – 0.3 | $V_{SSA}$ + 3.63 | V |
| $V_{BAT}$ | External battery supply voltage | $V_{SS}$ – 0.3 | $V_{SS}$ + 3.63 | V |
| $V_{IN}$ | Input voltage on 5V tolerant pin(3) | $V_{SS}$ – 0.3 | $V_{DD}$ + 3.63 | V |
| | Input voltage on other I/O | $V_{SS}$ – 0.3 | 3.63 | V |
| $\|\Delta V_{DDx}\|$ | Variations between different VDD power pins | - | 50 | mV |
| $\|V_{SSx}-V_{SS}\|$ | Variations between different ground pins | - | 50 | mV |
| $I_{IO}$ | Maximum current for GPIO pins | - | +/-25 | mA |
| $I_{IOS}$ | Maximum current for multiple IO(5) | - | 100 | mA |
| $T_A$ | Operating temperature range | -40 | +85 | °C |
| $P_D$ | Power dissipation at $T_A$ = 85°C of LQFP144 | - | 820 | mW |
| | Power dissipation at $T_A$ = 85°C of LQFP100 | - | 813 | |
| | Power dissipation at $T_A$ = 85°C of LQFP64 | - | 733 | |
| $T_{STG}$ | Storage temperature range | -65 | +150 | °C |
| $T_J$ | Maximum junction temperature | - | 125 | °C |

(1) Guaranteed by design, not tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) $V_{IN}$ maximum value cannot exceed 5.5 V.
(4) It is recommended that $V_{DD}$ and $V_{DDA}$ are powered by the same source. The maximum difference between $V_{DD}$ and $V_{DDA}$ does not exceed 300 mV during power-up and operation.
(5) $T_J$ = 110°C.

## 4.2. Operating conditions characteristics

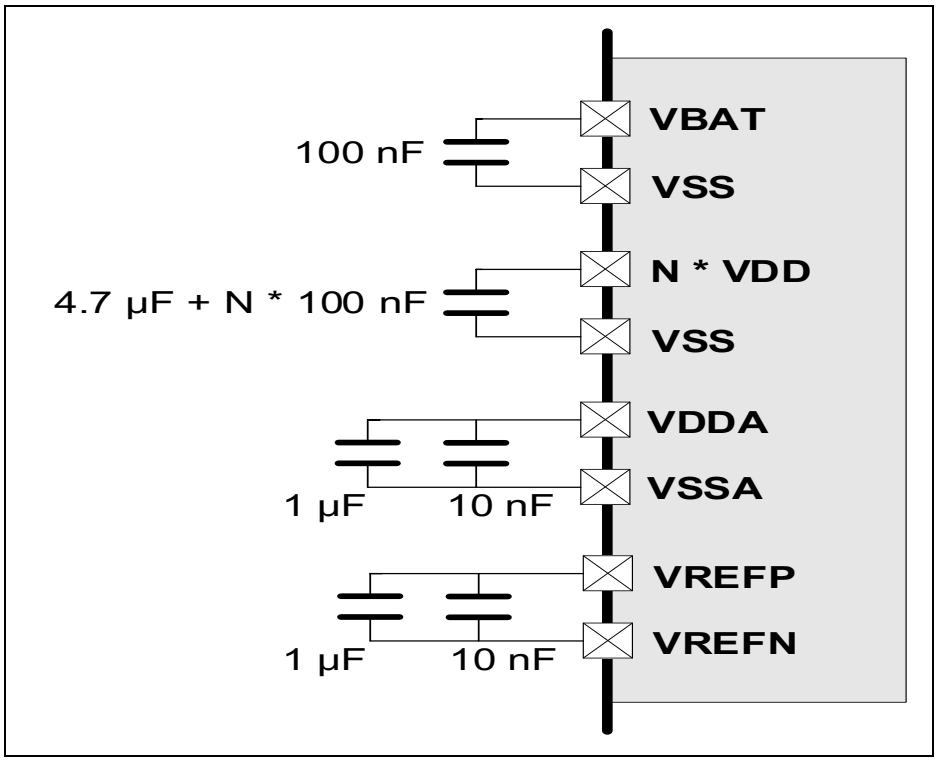
**Table 4-2. DC operating conditions**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | - | 1.71 | 3.3 | 3.63 | V |
| $V_{DDA}$ | Analog supply voltage, $f_{ADCMAX}$ = 35 MHz | - | 2.4 | 3.3 | 3.63 | V |
| | Analog supply voltage, $f_{ADCMAX}$ = 14 MHz | | 1.71 | - | 3.63 | |
| $V_{BAT}$ | Battery supply voltage | - | 1.71(2) | - | 3.63 | V |
| $V_{CORE}$ | Core logic supply voltage powered by internal voltage regulator | - | - | 1.1 | - | V |

(1) Based on characterization, not tested in production.

(2) In the application which $V_{BAT}$ supply the backup domains, if the VBAT voltage drops below the minimum value, when $V_{DD}$ is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

**Figure 4-1. Recommended power supply decoupling capacitors(1)(2)**




(1) The VREFP and VREFN pins are only available on no less than 100-pin packages, or else the VREFP and VREFN pins are not available and internally connected to VDDA and VSSA pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

**Table 4-3. Clock frequency(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | AHB clock frequency | - | - | 180 | MHz |
| $f_{APB1}$ | APB1 clock frequency | - | - | 90 | MHz |
| $f_{APB2}$ | APB2 clock frequency | - | - | 180 | MHz |

(1) Guaranteed by design, not tested in production.

**Table 4-4. Operating conditions at Power up/ Power down(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | - | 0 | ∞ | µs/ V |
| | $V_{DD}$ fall time rate | | 50 | ∞ | |

(1) Guaranteed by design, not tested in production.

**Table 4-5. Start-up timings of Operating conditions(1)(2)(3)**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| $t_{start-up}$ | Start-up time | Clock source from HXTAL | 608 | μs |
| | | Clock source from IRC8M | 74 | |

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

(3) PLL is off.

**Table 4-6. Power saving mode wakeup timings characteristics(1)(2)**

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $t_{Sleep}$ | Wakeup from Sleep mode | 1.7 | μs |
| $t_{Deep-sleep}$ | Wakeup from Deep-sleep mode (LDO On) | 3.1 | |
| | Wakeup from Deep-sleep mode (LDO in low power mode) | 3.1 | |
| | Wakeup from Deep-sleep mode1 (LDO in low power and low driver mode) | 4.3 | |
| | Wakeup from Deep-sleep mode2 (LDO in low power and low driver mode) | 11.7 | |
| $t_{Standby}$ | Wakeup from Standby mode | 77.2 | |

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: $V_{DD}$ = $V_{DDA}$ = 3.3 V, IRC8M = System clock = 8 MHz.

## 4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

**Table 4-7. Power consumption characteristics(2)(3)(4)(5)(6)**

| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}+I_{DDA}$ | Supply current (Run mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals enabled | - | 59.8 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals disabled | - | 26.1 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 160 MHz, All peripherals enabled | - | 53.6 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 160 MHz, All peripherals disabled | - | 23.5 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled | - | 41 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled | - | 18.2 | - | mA |

| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled | - | 37.2 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled | - | 16.6 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals enabled | - | 33.4 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals disabled | - | 15 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals enabled | - | 25.7 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals disabled | - | 11.8 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals enabled | - | 18 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals disabled | - | 7.96 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals enabled | - | 14 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals disabled | - | 6.49 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 24 MHz, All peripherals enabled | - | 9.73 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 24 MHz, All peripherals disabled | - | 4.83 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals enabled | - | 7.2 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals disabled | - | 3.9 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, | - | 4.62 | - | mA |

| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | System clock = 8 MHz, All peripherals enabled | | | | |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals disabled | - | 2.9 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, IRC = 8 MHz, System clock = 8 MHz, All peripherals enabled | - | 3.1 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, IRC = 8 MHz, System clock = 8 MHz, All peripherals disabled | - | 1.7 | - | mA |
| | Supply current (Sleep mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 180 MHz, CPU clock off, All peripherals enabled | - | 47.8 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 180 MHz, CPU clock off, All peripherals disabled | - | 9.5 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 160 MHz, CPU clock off, All peripherals enabled | - | 42.8 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 160 MHz, CPU clock off, All peripherals disabled | - | 8.7 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals enabled | - | 32.8 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals disabled | - | 7.07 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals enabled | - | 29.8 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals disabled | - | 6.57 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals enabled | - | 26.7 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals disabled | - | 6.1 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals enabled | - | 20.7 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, | - | 5.1 | - | mA |

| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | System Clock = 72 MHz, CPU clock off, All peripherals disabled | | | | |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals enabled | - | 14.5 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals disabled | - | 4.1 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals enabled | - | 11.4 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals disabled | - | 3.6 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 24 MHz, CPU clock off, All peripherals enabled | - | 8.3 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 24 MHz, CPU clock off, All peripherals disabled | - | 3.1 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 16 MHz, CPU clock off, All peripherals enabled | - | 6.2 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 16 MHz, CPU clock off, All peripherals disabled | - | 2.7 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 8 MHz, CPU clock off, All peripherals enabled | - | 4.2 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, HXTAL = 25 MHz, System Clock = 8 MHz, CPU clock off, All peripherals disabled | - | 2.4 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, IRC = 8 MHz, System Clock = 8 MHz, CPU clock off, All peripherals enabled | - | 2.8 | - | mA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, IRC = 8 MHz, System Clock = 8 MHz, CPU clock off, All peripherals disabled | - | 1.1 | - | mA |
| | Supply current (Deep-Sleep mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in normal power and normal driver mode, IRC40K off, RTC off | - | 461.33 | - | µA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in low power and normal driver mode, IRC40K off, RTC off | - | 413.00 | - | µA |

| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in normal power and low driver mode, IRC40K off, RTC off | - | 258.00 | - | μA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off | - | 210.67 | - | μA |
| | Supply current (Deep-Sleep 1 mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off | - | 163.33 | - | μA |
| | Supply current (Deep-Sleep 2 mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off | - | 68.00 | - | μA |
| | Supply current (Standby mode) | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LXTAL off, IRC40K on, RTC on | - | 3.79 | - | μA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LXTAL off, IRC40K on, RTC off | - | 3.58 | - | μA |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, LXTAL off, IRC40K off, RTC off | - | 3.08 | - | μA |
| $I_{BAT}$ | Battery supply current (Backup mode) | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 3.63 V, LXTAL on with external crystal, RTC on, LXTAL High driving | - | 1.95 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving | - | 1.82 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL High driving | - | 1.67 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 1.71 V, LXTAL on with external crystal, RTC on, LXTAL High driving | - | 1.59 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 3.63 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | - | 1.53 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | - | 1.40 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | - | 1.25 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 1.71 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | - | 1.18 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 3.63 V, LXTAL on | - | 1.12 | - | μA |

| Symbol | Parameter | Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| | | with external crystal, RTC on, LXTAL Medium Low driving | | | | |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving | - | 0.99 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving | - | 0.84 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 1.71 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving | - | 0.77 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 3.63 V, LXTAL on with external crystal, RTC on, LXTAL Low driving | - | 1.00 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving | - | 0.87 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Low driving | - | 0.72 | - | μA |
| | | $V_{DD}$ off, $V_{DDA}$ off, $V_{BAT}$ = 1.71 V, LXTAL on with external crystal, RTC on, LXTAL Low driving | - | 0.63 | - | μA |

(1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all values given for $T_A$ = 25 ℃ and test result is mean value.
(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.
(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.
(5) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.
(6) All GPIOs are configured as analog mode except standby mode.

Figure 4-2. Typical supply current consumption in Run mode

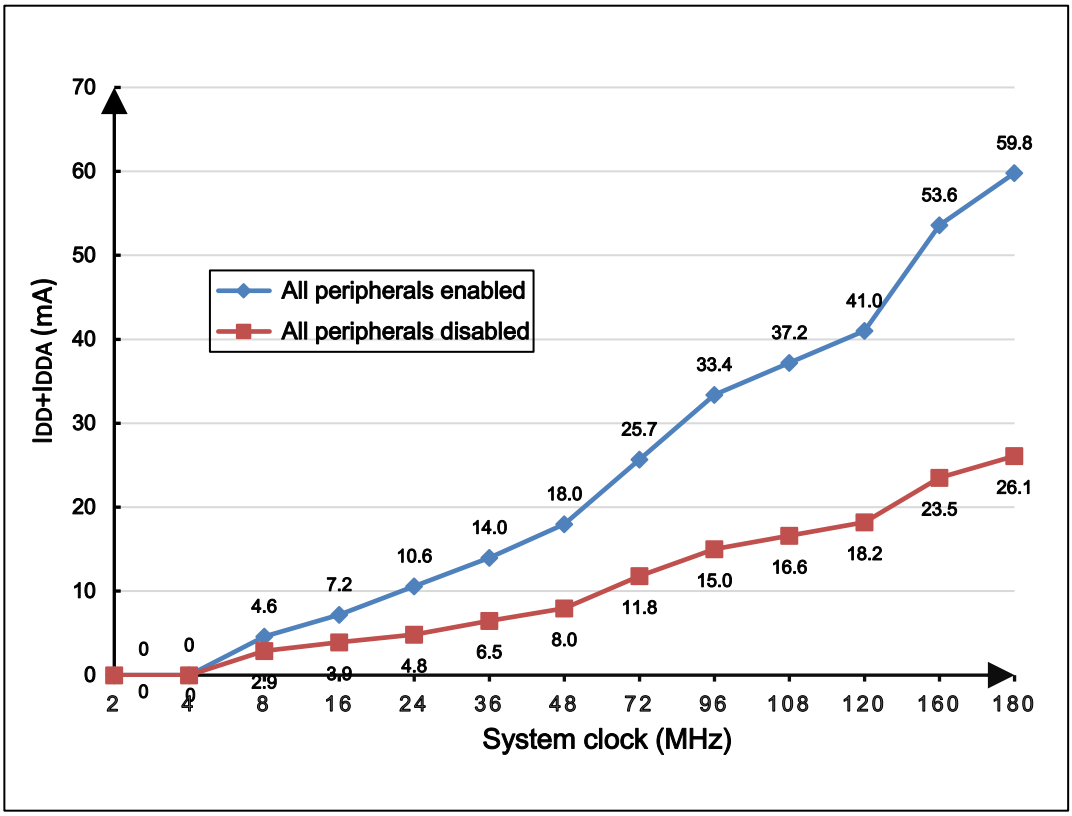
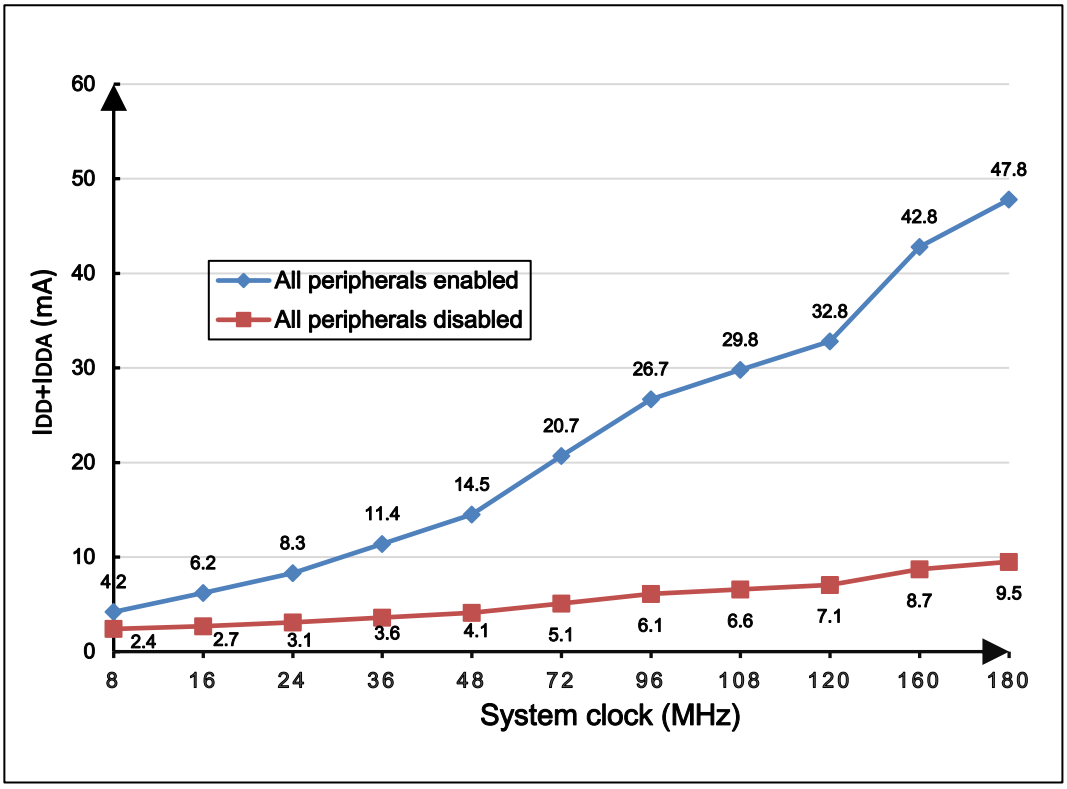



Figure 4-3. Typical supply current consumption in Sleep mode



## 4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in *Table 4-8. EMS characteristics*(1), based on the EMS levels and classes compliant with IEC 61000 series standard.

**Table 4-8. EMS characteristics**(1)

| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| $V_{ESD}$ | Contact / Air mode high voltage stressed on few special I/O pins | $V_{DD}$ = 3.3 V, $T_A$ = 25 °C LQFP144, $f_{HCLK}$ = 180 MHz conforms to IEC 61000-4-2 | 3A |
| $V_{FTB}$ | Fast transient high voltage burst stressed on Power and GND | $V_{DD}$ = 3.3 V, $T_A$ = 25 °C LQFP144, $f_{HCLK}$ = 180 MHz conforms to IEC 61000-4-4 | 4A |

(1) Based on characterization, not tested in production.

EMI (Electromagnetic Interference) emission test result is given in the *Table 4-9. EMI characteristics*(1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

**Table 4-9. EMI characteristics**(1)

| Symbol | Parameter | Conditions | Tested frequency band | Max vs. [$f_{HXTAL}/f_{HCLK}$] 8/180 MHz | Unit |
|---|---|---|---|---|---|
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = +23 °C, LQFP144, $f_{HCLK}$ = 180 MHz, conforms to SAE J1752-3:2017 | 0.15 MHz to 30 MHz | -7.58 | dBµV |
| | | | 30 MHz to 130 MHz | 3.35 | |
| | | | 130 MHz to 1 GHz | 4.25 | |

(1) Based on characterization, not tested in production.

## 4.5. Power supply supervisor characteristics

**Table 4-10. Power supply supervisor characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{LVD}$(1) | Low voltage Detector level selection | LVDT<2:0> = 000(rising edge) | - | 2.19 | - | V |
| | | LVDT<2:0> = 000(falling edge) | - | 2.08 | - | |
| | | LVDT<2:0> = 001(rising edge) | - | 2.33 | - | |
| | | LVDT<2:0> = 001(falling edge) | - | 2.22 | - | |
| | | LVDT<2:0> = 010(rising edge) | - | 2.48 | - | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | LVDT<2:0> = 010(falling edge) | - | 2.36 | - | |
| | | LVDT<2:0> = 011(rising edge) | - | 2.62 | - | |
| | | LVDT<2:0> = 011(falling edge) | - | 2.51 | - | |
| | | LVDT<2:0> = 100(rising edge) | - | 2.75 | - | |
| | | LVDT<2:0> = 100(falling edge) | - | 2.65 | - | |
| | | LVDT<2:0> = 101(rising edge) | - | 2.9 | - | |
| | | LVDT<2:0> = 101(falling edge) | - | 2.79 | - | |
| | | LVDT<2:0> = 110(rising edge) | - | 3.04 | - | |
| | | LVDT<2:0> = 110(falling edge) | - | 2.93 | - | |
| | | LVDT<2:0> = 111(rising edge) | - | 3.19 | - | |
| | | LVDT<2:0> = 111(falling edge) | - | 3.07 | - | |
| $V_{LVDhyst}$(2) | LVD hysteresis | - | - | 100 | - | mV |
| $V_{POR}$(1) | Power on reset threshold | - | - | 1.56 | - | V |
| $V_{PDR}$(1) | Power down reset threshold | - | - | 1.52 | - | V |
| $V_{PDRhyst}$(2) | PDR hysteresis | - | - | 40 | - | mV |
| $V_{BOR3}$(2) | Brownout level 3 threshold | Falling edge | - | 2.8 | - | V |
| | | Rising edge | - | 2.9 | - | V |
| $V_{BOR2}$(2) | Brownout level 2 threshold | Falling edge | - | 2.5 | - | V |
| | | Rising edge | - | 2.6 | - | V |
| $V_{BOR1}$(2) | Brownout level 1 threshold | Falling edge | - | 2.2 | - | V |
| | | Rising edge | - | 2.3 | - | V |
| $V_{BORhyst}$(2) | BOR hysteresis | - | - | 100 | - | mV |
| $t_{RSTTEMPO}$(2) | Reset temporization | - | - | 2.88 | - | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

## 4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

**Table 4-11. ESD characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$=25 °C; ESDA/JEDEC JS-001-2017 | - | 6000 | - | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$=25 °C; ESDA/JEDEC JS-002-2018 | - | 1000 | - | V |

(1) Based on characterization, not tested in production.

**Table 4-12. Static latch-up characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LU | I-test | $T_A$=25 °C; JESD78E | - | 200 | - | mA |
| | $V_{supply}$ over voltage | | - | 5.4 | - | V |

(1) Based on characterization, not tested in production.

## 4.7. External clock characteristics

**Table 4-13. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HXTAL}$(1) | Crystal or ceramic frequency | 1.71 V <= $V_{DD}$ <= 3.63 V | 4 | 8 | 32 | MHz |
| $R_F$(2) | Feedback resistor | $V_{DD}$ = 3.3 V | - | 400 | - | kΩ |
| $C_{HXTAL}$(2)(3) | Recommended load capacitance on OSCIN and OSCOUT | - | - | 20 | 30 | pF |
| $Ducy_{(HXTAL)}$(2) | Crystal or ceramic duty cycle | - | 30 | 50 | 70 | % |
| $g_m$(2) | Oscillator transconductance | Startup | - | 25 | - | mA/V |
| $I_{DDHXTAL}$(1) | Crystal or ceramic operating current | $V_{DD}$ = 3.3 V, $f_{HCLK}$ = $f_{IRC8M}$ = 8 MHz $T_A$ = 25 °C | - | 0.42 | - | mA |
| $t_{SUHXTAL}$(1) | Crystal or ceramic startup time | $V_{DD}$ = 3.3 V, $f_{HCLK}$ = $f_{IRC8M}$ = 8 MHz $T_A$ = 25 °C | - | 2 | - | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{HXTAL1}$ = $C_{HXTAL2}$ = 2*($C_{LOAD}$ – $C_S$), For $C_{HXTAL1}$ and $C_{HXTAL2}$, it is recommended matching capacitance on OSCIN and OSCOUT. For $C_{LOAD}$, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For $C_S$, it is PCB and MCU pin stray capacitance.

**Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HXTAL_ext}$(1) | External clock source or oscillator frequency | 1.71 V <= $V_{DD}$ <= 3.63 V | 1 | - | 50 | MHz |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{HXTALH}$(2) | OSCIN input pin high level voltage | $V_{DD}$ = 3.3 V | 0.7 $V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HXTALL}$(2) | OSCIN input pin low level voltage | | $V_{SS}$ | - | 0.3 $V_{DD}$ | V |
| $t_{H/L(HXTAL)}$(2) | OSCIN high or low time | - | 5 | - | - | ns |
| $t_{R/F(HXTAL)}$(2) | OSCIN rise or fall time | - | - | - | 10 | ns |
| $C_{IN}$(2) | OSCIN input capacitance | - | - | 5 | - | pF |
| $Ducy_{(HXTAL)}$(2) | Duty cycle | - | 40 | - | 60 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LXTAL}$(1) | Crystal or ceramic frequency | $V_{DD}$ = 3.3 V | - | 32.768 | - | kHz |
| $C_{LXTAL}$(2)(3) | Recommended matching capacitance on OSC32IN and OSC32OUT | - | - | 10 | - | pF |
| $Ducy_{(LXTAL)}$(2) | Crystal or ceramic duty cycle | - | 30 | - | 70 | % |
| $g_m$(2) | Oscillator transconductance | Lower driving capability | - | 4 | - | µA/V |
| | | Medium low driving capability | - | 6 | - | |
| | | Medium high driving capability | - | 12 | - | |
| | | Higher driving capability | - | 18 | - | |
| $I_{DDLXTAL}$(1) | Crystal or ceramic operating current | LXTALDRI[1:0] = 00 | - | 0.7 | - | µA |
| | | LXTALDRI[1:0] = 01 | - | 0.8 | - | |
| | | LXTALDRI[1:0] = 10 | - | 1.2 | - | |
| | | LXTALDRI[1:0] = 11 | - | 1.6 | - | |
| $t_{SULXTAL}$(1)(4) | Crystal or ceramic startup time | - | - | 2 | - | s |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} – C_S)$, For $C_{LXTAL1}$ and $C_{LXTAL2}$, it is recommended matching capacitance on SC32IN and OSC32OUT. For $C_{LOAD}$, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For $C_S$, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

**Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LXTAL_ext}$(1) | External clock source or oscillator frequency | $V_{DD}$ = 3.3 V | - | 32.768 | 1000 | kHz |
| $V_{LXTALH}$(2) | OSC32IN input pin high level voltage | - | 0.7 $V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LXTALL}$(2) | OSC32IN input pin low level voltage | - | $V_{SS}$ | - | 0.3 $V_{DD}$ | |
| $t_{H/L(LXTAL)}$(2) | OSC32IN high or low time | - | 450 | - | - | ns |
| $t_{R/F(LXTAL)}$(2) | OSC32IN rise or fall time | - | - | - | 50 | |
| $C_{IN}$(2) | OSC32IN input capacitance | - | - | 5 | - | pF |
| $Ducy_{(LXTAL)}$(2) | Duty cycle | - | 30 | 50 | 70 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

## 4.8. Internal clock characteristics

**Table 4-17. High speed internal clock (IRC8M) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC8M}$ | High Speed Internal Oscillator (IRC8M) frequency | $V_{DD}$ = $V_{DDA}$ = 3.3 V | - | 8 | - | MHz |
| $ACC_{IRC8M}$ | IRC8M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = -40 °C ~ +85 °C(1) | -2.5 | - | +2.5 | % |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = 0 °C ~ +85 °C(1) | -1.8 | - | +1.8 | % |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = 25 °C | -1.0 | - | +1.0 | % |
| | IRC8M oscillator Frequency accuracy, User trimming step(1) | - | - | 0.5 | - | % |
| $Ducy_{IRC8M}$(2) | IRC8M oscillator duty cycle | $V_{DD}$ = $V_{DDA}$ = 3.3 V | 45 | 50 | 55 | % |
| $I_{DDAIRC8M}$(1) | IRC8M oscillator operating current | $V_{DD}$ = $V_{DDA}$ = 3.3 V, | - | 80 | - | μA |
| $t_{SUIRC8M}$(1) | IRC8M oscillator startup time | $V_{DD}$ = $V_{DDA}$ = 3.3 V, | - | 1.5 | - | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-18. Low speed internal clock (IRC40K) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC40K}$(1) | Low Speed Internal oscillator (IRC40K) frequency | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = -40 °C ~ +85 °C | 20 | 40 | 45 | kHz |
| $I_{DDAIRC40K}$(2) | IRC40K oscillator operating current | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ = $f_{HXTAL_PLL}$ = 180 MHz $T_A$ = 25 °C | - | 0.4 | - | μA |
| $t_{SUIRC40K}$(2) | IRC40K oscillator startup time | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ = $f_{HXTAL_PLL}$ = 180 MHz $T_A$ = 25 °C | - | 80 | - | μs |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

**Table 4-19. High speed internal clock (IRC48M) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC48M}$ | High Speed Internal Oscillator (IRC48M) frequency | $V_{DD}$ = 3.3 V | - | 48 | - | MHz |
| $ACC_{IRC48M}$ | IRC48M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = -40 °C ~ +85 °C(1) | -4.0 | - | +5.0 | % |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = 0 °C ~ +85 °C (1) | -3.0 | - | +3.0 | % |
| | | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = 25 °C | -2.0 | - | +2.0 | % |
| | IRC48M oscillator Frequency accuracy, User trimming step(1) | - | - | 0.12 | - | % |
| $D_{IRC48M}$(2) | IRC48M oscillator duty cycle | $V_{DD}$ = $V_{DDA}$ = 3.3 V | 45 | 50 | 55 | % |
| $I_{DDAIRC48M}$(1) | IRC48M oscillator operating current | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ = $f_{HXTAL_PLL}$ = 180 MHz | - | 286.9 | - | μA |
| $t_{SUIRC48M}$(1) | IRC48M oscillator startup time | $V_{DD}$ = $V_{DDA}$ = 3.3 V, $f_{HCLK}$ = $f_{HXTAL_PLL}$ = 180 MHz | - | 3.68 | - | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

## 4.9. PLL characteristics

**Table 4-20. PLL characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$(1) | PLL input clock frequency | - | 2 | - | 16 | MHz |
| $f_{PLLOUT}$(2) | PLL output clock frequency | - | 16 | - | 180 | MHz |
| $f_{VCO}$(2) | PLL VCO output clock frequency | - | 32 | - | 360 | MHz |
| $t_{LOCK}$(2) | PLL lock time | - | - | - | 300 | μs |
| $I_{DDA}$(1)(3) | Current consumption on $V_{DDA}$ | VCO freq = 360 MHz | - | 700 | - | μA |
| $I_{DD}$(1)(3) | Current consumption on $V_{DD}$ | VCO freq = 360 MHz | - | 500 | - | μA |
| $Jitter_{PLL}$(1)(4) | Cycle to cycle Jitter (rms) | System clock | - | 40 | - | ps |
| | Cycle to cycle Jitter (peak to peak) | | - | 400 | - | |

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) System clock = IRC8M = 8 MHz, PLL clock source = IRC8M/2 = 4 MHz, $f_{PLLOUT}$ = 180 MHz.
(4) Value given with main PLL running.

**Table 4-21. PLL1 characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$(1) | PLL input clock frequency | - | 2 | - | 16 | MHz |
| $f_{PLLOUT}$(2) | PLL output clock frequency | - | 16 | - | 100 | MHz |
| $f_{VCO}$(2) | PLL VCO output clock frequency | - | 32 | - | 180 | MHz |
| $t_{LOCK}$(2) | PLL lock time | - | - | - | 300 | μs |
| $I_{DDA}$(1) | Current consumption on $V_{DDA}$ | VCO freq = 180 MHz | - | 400 | - | μA |
| $I_{DD}$(1) | Current consumption on $V_{DD}$ | VCO freq = 180 MHz | - | 250 | - | μA |
| $Jitter_{PLL}$(1) | Cycle to cycle Jitter | - | - | 40 | - | ps |

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

**Table 4-22. PLL2 characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$(1) | PLL input clock frequency | - | 2 | - | 16 | MHz |
| $f_{PLLOUT}$(2) | PLL output clock frequency | - | 16 | - | 180 | MHz |
| $f_{VCO}$(2) | PLL VCO output clock frequency | - | 32 | - | 360 | MHz |
| $t_{LOCK}$(2) | PLL lock time | - | - | - | 300 | μs |
| $I_{DDA}$(1) | Current consumption on $V_{DDA}$ | VCO freq = 360 MHz | - | 700 | - | μA |
| $I_{DD}$(1) | Current consumption on $V_{DD}$ | VCO freq = 360 MHz | - | 500 | - | μA |
| $Jitter_{PLL}$(1) | Cycle to cycle Jitter | - | - | 40 | - | ps |

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

**Table 4-23. PLLUSB characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$(1) | PLL input clock frequency | - | 4 | - | 30 | MHz |
| $f_{PLLOUT}$(2) | PLL output clock frequency | - | - | 480 | - | MHz |
| $t_{LOCK}$(2) | PLL lock time | - | - | 100 | 150 | μs |
| $Jitter_{PLL}$(2) | Cycle to cycle Jitter | System clock | - | 40 | - | ps |
| | Cycle to cycle Jitter (peak to peak) | | - | 400 | - | |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-24. PLL spread spectrum clock generation (SSCG) characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{mod}$ | Modulation frequency | - | - | - | 10 | KHz |
| mdamp | Peak modulation amplitude | - | - | - | 2 | % |
| MODCNT* MODSTEP | - | - | - | - | $2^{15}$-1 | - |

(1) Guaranteed by design, not tested in production.

***Equation 1***: SSCG configuration equation:

$MODCNT=round(f_{PLLIN}/4/f_{mod})$

$MODSTEP = round(mdamp*PLLN*2^{15}/(MODCNT*100))$

The formula above (***Equation 1***) is SSCG configuration equation.

## 4.10. Memory characteristics

**Table 4-25. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min(1) | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| $PE_{CYC}$ | Number of guaranteed program /erase cycles before failure (Endurance) | $T_A$ = -40 °C ~ +85 °C | 100 | - | - | kcycles |
| $t_{RET}$ | Data retention time | $T_A$ = 85 °C after up to 0 kcycle(2) | 25 | - | - | years |
| | | $T_A$ = 85 °C after up to 10 kcycles(2) | 15 | - | - | |
| $t_{PROG}$ | Word programming time | $T_A$ = -40 °C ~ +85 °C | - | 37.5 | - | μs |
| $t_{ERASE}$ | Page erase time | $T_A$ = -40 °C ~ +85 °C | - | 11 | - | ms |
| $t_{MERASE}$ | Mass erase time | $T_A$ = -40 °C ~ +85 °C | - | 12 | - | ms |

(1) Based on characterization, not tested in production.

(2) Cycling performed over the whole temperature range.

## 4.11. NRST pin characteristics

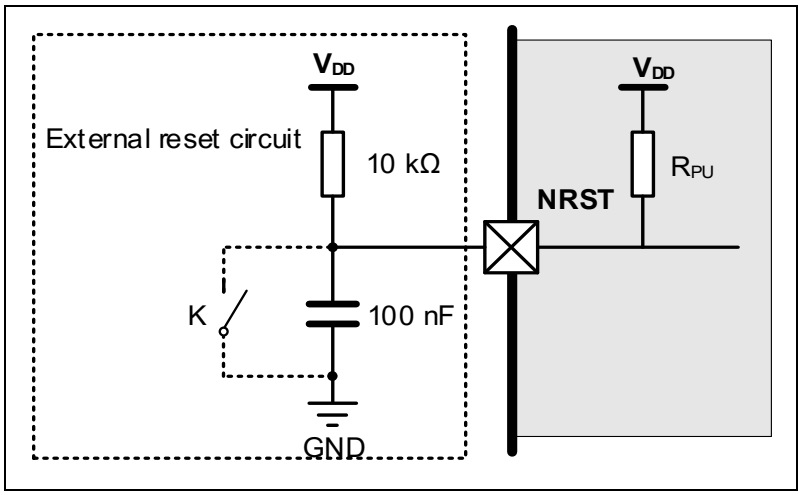
**Table 4-26. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | $V_{DD}$ = $V_{DDA}$ = 1.71 V | - | - | 0.35 $V_{DD}$ | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | | 0.65 $V_{DD}$ | - | - | |
| $V_{hyst}$(1) | Schmidt trigger Voltage hysteresis | | - | 120 | - | mV |
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | $V_{DD}$ = $V_{DDA}$ = 3.3 V | - | - | 0.35 $V_{DD}$ | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | | 0.65 $V_{DD}$ | - | - | |
| $V_{hyst}$(1) | Schmidt trigger Voltage hysteresis | | - | 180 | - | mV |
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | $V_{DD}$ = $V_{DDA}$ = 3.63 V | - | - | 0.35 $V_{DD}$ | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | | 0.65 $V_{DD}$ | - | - | |
| $V_{hyst}$(1) | Schmidt trigger Voltage hysteresis | | - | 200 | - | mV |
| $R_{pu}$(2) | Pull-up equivalent resistor | - | - | 40 | - | kΩ |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Figure 4-4. Recommended external NRST pin circuit(1)**




(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

## 4.12. GPIO characteristics

**Table 4-27. I/O port DC characteristics(1)(3)**

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Standard IO Low level input voltage | | 1.71 V <= $V_{DD}$ = $V_{DDA}$ <= 3.63 V | - | - | 0.35 $V_{DD}$ | V |
| | 5V-tolerant IO Low level input voltage | | 1.71 V <= $V_{DD}$ = $V_{DDA}$ <= 3.63 V | - | - | 0.35 $V_{DD}$ | V |
| $V_{IH}$ | Standard IO High level input voltage | | 1.71 V <= $V_{DD}$ = $V_{DDA}$ <= 3.63 V | 0.65 $V_{DD}$ | - | - | V |
| | 5V-tolerant IO High level input voltage | | 1.71 V <= $V_{DD}$ = $V_{DDA}$ <= 3.63 V | 0.65 $V_{DD}$ | - | - | V |
| $V_{OL}$ | Low level output voltage for an IO Pin ($I_{IO}$ = +8 mA) | | $V_{DD}$ = 1.71V | - | - | 0.19 | V |
| | | | $V_{DD}$ = 3.3 V | - | - | 0.12 | |
| | | | $V_{DD}$ = 3.63V | - | - | 0.11 | |
| $V_{OL}$ | Low level output voltage for an IO Pin ($I_{IO}$ = +20 mA) | | $V_{DD}$ = 1.71V | - | - | 0.61 | V |
| | | | $V_{DD}$ = 3.3 V | - | - | 0.3 | |
| | | | $V_{DD}$ = 3.63V | - | - | 0.29 | |
| $V_{OH}$ | High level output voltage for an IO Pin ($I_{IO}$ = +8 mA) | | $V_{DD}$ = 1.71V | 1.48 | - | - | V |
| | | | $V_{DD}$ = 3.3 V | 3.17 | - | - | |
| | | | $V_{DD}$ = 3.63V | 3.47 | - | - | |
| $V_{OH}$ | High level output voltage for an IO Pin ($I_{IO}$ = +20 mA) | | $V_{DD}$ = 1.71V | - | - | - | V |
| | | | $V_{DD}$ = 3.3 V | 2.96 | - | - | |
| | | | $V_{DD}$ = 3.63V | 3.26 | - | - | |
| $R_{PU}$(2) | Internal pull-up resistor | All pins | - | - | 40 | - | kΩ |
| | | PA10 | - | - | 10 | - | |
| $R_{PD}$(2) | Internal pull-down resistor | All pins | - | - | 40 | - | kΩ |
| | | PA10 | - | - | 10 | - | |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current(typical source capability:3 mA shared between these Ios, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

**Table 4-28. I/O port AC characteristics(1)(2)**

| GPIOx_Mdy[1:0] bit value(3) | Parameter | Conditions | Max | Unit |
|---|---|---|---|---|
| GPIOx_CTL->Mdy[1:0]=10 (IO_Speed = 2 MHz) | Maximum frequency(4) | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 10 pF | 4 | MHz |
| | | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 30 pF | 3 | |
| | | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 50 pF | 2 | |
| GPIOx_CTL->Mdy[1:0] = 01 (IO_Speed = 10 MHz) | Maximum frequency(4) | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 10 pF | 60 | MHz |
| | | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 30 pF | 30 | |
| | | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 50 pF | 12 | |
| GPIOx_CTL->Mdy[1:0]=11 | Maximum | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 10 pF | 100 | MHz |

| GPIOx_Mdy[1:0] bit value(3) | Parameter | Conditions | Max | Unit |
|---|---|---|---|---|
| (IO_Speed = 50 MHz) | frequency(4) | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 30 pF | 80 | |
| | | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 50 pF | 60 | |
| GPIOx_CTL->Mdy[1:0]=11 and GPIOx_SPDy=1 (IO_Speed = MAX) | Maximum frequency(4) | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 10 pF | 120 | MHz |
| | | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 30 pF | 100 | |
| | | 1.8 <= $V_{DD}$ <= 3.63 V, $C_L$ = 50 pF | 80 | |

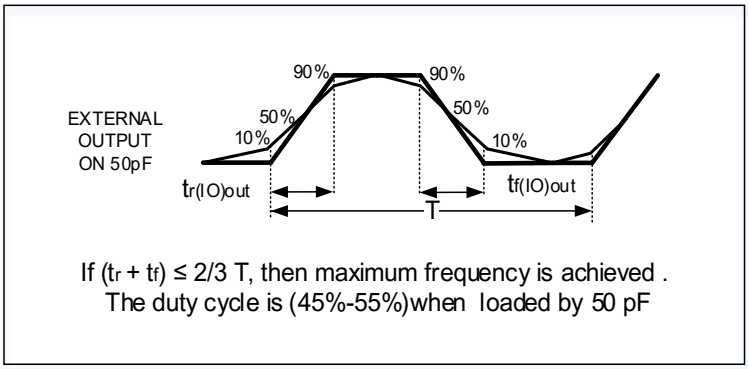
(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all test results given for $T_A$ = 25 ℃.

(3) The I/O speed is configured using the GPIOx_CTL -> Mdy[1:0] bits. Refer to the GD32E50x user manual which is selected to set the GPIO port output speed.

(4) The maximum frequency is defined in *Figure 4-5. I/O port AC characteristics definition*, and maximum frequency cannot exceed 180 MHz.

**Figure 4-5. I/O port AC characteristics definition**




## 4.13. Temperature sensor characteristics

**Table 4-29. Temperature sensor characteristics(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.8 | - | 3.63 | V |
| $V_{DDA}$ | Analog supply voltage | 1.8 | - | 3.63 | |
| $V_{REFP}$ | Positive Reference Voltage | 1.8 | - | $V_{DDA}$ | |
| $V_{REFN}$ | Negative Reference Voltage | - | $V_{SSA}$ | - | |
| $T_L$ | VSENSE linearity with temperature | - | +/-1.5 | - | ℃ |
| Avg_Slope | Average slope | - | 4.1 | - | mV/℃ |
| $V_{25}$ | Voltage at 25 ℃ | - | 1.45 | - | V |
| $t_{S_temp}$(2) | ADC sampling time when reading the temperature | - | 17.1 | - | μs |

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

## 4.14. ADC characteristics

**Table 4-30. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$(1) | Operating voltage | - | 1.71 | 3.3 | 3.63 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$(1) | ADC input voltage range | - | 0 | - | $V_{REFP}$ | V |
| $V_{REFINT}$(2) | Internal Reference Voltage | $T_J$=-40℃~105℃ | 1.1 | 1.2 | 1.3 | V |
| $V_{REFP}$(2)(3) | Positive Reference Voltage | - | 1.71 | - | $V_{DDA}$ | V |
| $V_{REFN}$(2) | Negative Reference Voltage | - | - | $V_{SSA}$ | - | V |
| $f_{ADC}$(1) | ADC clock | $V_{DDA}$ = 1.71 V to 2.4 V | 0.1 | - | 14 | MHz |
| | | $V_{DDA}$ = 2.4 V to 3.63 V | 0.1 | - | 35 | MHz |
| $f_S$(1) | Sampling rate | 12-bit | 0.007 | - | 2.5 | MSPS |
| | | 10-bit | 0.008 | - | 2.92 | |
| | | 8-bit | 0.01 | - | 3.5 | |
| | | 6-bit | 0.013 | - | 4.38 | |
| $V_{AIN}$(1) | Analog input voltage | 16 external; 2 internal | 0 | - | $V_{DDA}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 2* | - | - | 175.8 | kΩ |
| $R_{ADC}$(2) | Input sampling switch resistance | - | - | - | 0.5 | kΩ |
| $C_{ADC}$(2) | Input sampling capacitance | No pin/pad capacitance included | - | - | 4 | pF |
| $t_{CAL}$(2) | Calibration time | $f_{ADC}$ = 35 MHz | - | 15.94 | - | μs |
| $t_s$(2) | Sampling time | $f_{ADC}$ = 35 MHz | 0.043 | - | 6.84 | μs |
| $t_{CONV}$(2) | Total conversion time(including sampling time) | 12-bit | - | 14 | - | 1/$f_{ADC}$ |
| | | 10-bit | - | 12 | - | |
| | | 8-bit | - | 10 | - | |
| | | 6-bit | - | 8 | - | |
| $t_{SU}$(2) | Startup time | - | - | - | 1 | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $V_{REFP}$ should always be equal to or less than $V_{DDA}$, especially during power up.

***Equation 2:***

$R_{AIN}$ max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 4-31. ADC $R_{AIN}$ max for $f_{ADC}$ = 35 MHz**

| $T_s$ (cycles) | $t_s$ (μs) | $R_{AIN\ max}$ (kΩ) |
|---|---|---|
| 1.5 | 0.043 | 0.6 |
| 7.5 | 0.21 | 5.0 |
| 13.5 | 0.39 | 9.4 |
| 28.5 | 0.81 | 20.5 |
| 41.5 | 1.19 | 30.0 |
| 55.5 | 1.59 | 40.0 |
| 71.5 | 2.04 | 52.0 |
| 239.5 | 6.84 | 175.8 |

**Table 4-32. ADC dynamic accuracy at $f_{ADC}$ = 14 MHz $V_{DDA}$ = 1.8 V(1)**

| Symbol | Parameter | Test conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ = 14 MHz<br>$V_{DDA}$ = $V_{REFP}$ = 1.8 V<br>Input Frequency = 20 kHz<br>Temperature = 25 ℃ | Single ended | 10.4 | 10.8 | - | bits |
| | | | Differential | 10.9 | 11.3 | - | |
| SNDR | Signal-to-noise and distortion ratio | | Single ended | 64.4 | 66.8 | - | dB |
| | | | Differential | 67.5 | 69.9 | - | |
| SNR | Signal-to-noise ratio | | Single ended | 64.5 | 66.9 | - | |
| | | | Differential | 67.6 | 70.2 | - | |
| THD | Total harmonic distortion | | Single ended | - | -81 | -78 | |
| | | | Differential | - | -82 | -79 | |

(1) Based on characterization, not tested in production.

**Table 4-33. ADC dynamic accuracy at $f_{ADC}$ = 35 MHz $V_{DDA}$ = 3.3 V(1)**

| Symbol | Parameter | Test conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ = 35 MHz<br>$V_{DDA}$ = $V_{REFP}$ =3.3 V<br>Input Frequency = 20 kHz<br>Temperature = 25 ℃ | Single ended | 10.7 | 11.1 | - | bits |
| | | | Differential | 11 | 11.4 | - | |
| SNDR | Signal-to-noise and distortion ratio | | Single ended | 66.2 | 68.6 | - | dB |
| | | | Differential | 68.2 | 70.6 | - | |
| SNR | Signal-to-noise ratio | | Single ended | 66 | 68.8 | - | |
| | | | Differential | 68 | 71 | - | |
| THD | Total harmonic distortion | | Single ended | - | -82 | -78 | |
| | | | Differential | - | -83 | -79 | |

(1) Based on characterization, not tested in production.

**Table 4-34. ADC dynamic accuracy at $f_{ADC}$ = 35 MHz $V_{DDA}$ = 2.4 V(1)**

| Symbol | Parameter | Test conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ = 35 MHz<br>$V_{DDA}$ = $V_{REFP}$ =2.4 V<br>Input Frequency = 20 kHz<br>Temperature = 25 ℃ | Single ended | 10.6 | 11 | - | bits |
| | | | Differential | 11 | 11.4 | - | |
| SNDR | Signal-to-noise and distortion ratio | | Single ended | 66 | 68.3 | - | dB |
| | | | Differential | 68 | 70.4 | - | |
| SNR | Signal-to-noise ratio | | Single ended | 65 | 68.5 | - | |
| | | | Differential | 67 | 70.8 | - | |
| THD | Total harmonic distortion | | Single ended | - | -82 | -78 | |
| | | | Differential | - | -83 | -79 | |

(1) Based on characterization, not tested in production.

**Table 4-35. ADC static accuracy at $f_{ADC}$ = 14 MHz $V_{DDA}$ = 1.8 V(1)**

| Symbol | Parameter | Test conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Offset | Offset error | $f_{ADC}$ = 14 MHz<br>$V_{DDA}$ = $V_{REFP}$ = 1.8 V<br>Temperature = 25 ℃ | Single ended | +/-0.5 | +/-1 | LSB |
| | | | Differential | +/-0.5 | +/-1 | |
| DNL | Differential linearity error | | Single ended | +/-0.5 | +/-1 | |
| | | | Differential | +/-0.6 | +/-1 | |
| INL | Integral linearity error | | Single ended | +/-0.6 | +/-1 | |
| | | | Differential | +/-0.8 | +/-1.5 | |

(1) Based on characterization, not tested in production.

**Table 4-36. ADC static accuracy at $f_{ADC}$ = 35 MHz $V_{DDA}$ = 3.3 V(1)**

| Symbol | Parameter | Test conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Offset | Offset error | $f_{ADC}$ = 35 MHz<br>$V_{DDA}$ = $V_{REFP}$ = 3.3 V<br>Temperature = 25 ℃ | Single ended | +/-0.5 | +/-1 | LSB |
| | | | Differential | +/-0.5 | +/-1 | |
| DNL | Differential linearity error | | Single ended | +/-0.5 | +/-0.8 | |
| | | | Differential | +/-0.7 | +/-1 | |
| INL | Integral linearity error | | Single ended | +/-0.7 | +/-1 | |
| | | | Differential | +/-0.9 | +/-1.5 | |

(1) Based on characterization, not tested in production.

**Table 4-37. ADC static accuracy at $f_{ADC}$ = 35 MHz $V_{DDA}$ = 2.4 V(1)**

| Symbol | Parameter | Test conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Offset | Offset error | $f_{ADC}$ = 35 MHz<br>$V_{DDA}$ = $V_{REFP}$ = 2.4 V<br>Temperature = 25 ℃ | Single ended | +/-0.5 | +/-1 | LSB |
| | | | Differential | +/-0.5 | +/-1 | |
| DNL | Differential linearity error | | Single ended | +/-0.5 | +/-0.8 | |
| | | | Differential | +/-0.6 | +/-1 | |
| INL | Integral linearity error | | Single ended | +/-0.6 | +/-1 | |
| | | | Differential | +/-0.8 | +/-1.5 | |

(1) Based on characterization, not tested in production.

## 4.15. DAC characteristics

**Table 4-38. DAC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$(1) | Operating voltage | - | 1.8 | 3.3 | 3.63 | V |
| $V_{REFP}$(2) | Positive Reference Voltage | - | 1.8 | - | $V_{DDA}$ | V |
| $V_{REFN}$(2) | Negative Reference Voltage | - | - | $V_{SSA}$ | - | V |
| $R_{LOAD}$(2) | Load resistance | Resistive load with buffer ON | 5 | - | - | kΩ |
| Ro(2) | Impedance output with buffer OFF | - | - | - | 15 | kΩ |
| $C_{LOAD}$(2) | Load capacitance | No pin/pad capacitance included | - | - | 50 | pF |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer ON | - | 0.2 | - | - | V |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer ON | - | - | - | VDDA -0.2 | V |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer OFF | - | - | 0.5 | - | mV |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer OFF | - | - | - | VREF -1LSB | V |
| $I_{DDA}$(1) | DAC current consumption in quiescent mode | With no load, middle code(0x800) on the input, $V_{REFP}$ = 3.63 V | - | 400 | - | uA |
| | | With no load, worst code(0xF1C) on the input, $V_{REFP}$ = 3.63 V | - | 450 | - | uA |
| $I_{DDVREFP}$(1) | DAC current consumption in quiescent mode | With no load, middle code(0x800) on the input, $V_{REFP}$ = 3.63 V | - | 100 | - | uA |
| | | With no load, worst code(0xF1C) on the input, $V_{REFP}$ = 3.63 V | - | 150 | - | uA |
| DNL(1) | Differential non-linearity error | DAC in 12-bit mode | - | - | +/-2 | LSB |
| INL(1) | Integral non-linearity | DAC in 12-bit mode | - | - | +/-4 | LSB |
| Offset(1) | Offset error | DAC in 12-bit mode | - | - | 10 | LSB |
| GE(1) | Gain error | DAC in 12-bit mode | - | - | 0.5 | % |
| $T_{setting}$(1) | Settling time | $C_{LOAD}$ <= 50 pF, $R_{LOAD}$ >= 5 kΩ | - | - | 0.5 | μs |
| $T_{wakeup}$(2) | Wakeup from off state | - | - | - | 5 | μs |
| Update rate(2) | Max frequency for a correct DAC_OUT change from code i to i+/-1LSBs | $C_{LOAD}$ <= 50 pF, $R_{LOAD}$ >= 5 kΩ | - | - | 4 | MS/s |
| PSRR(2) | Power supply rejection ratio | - | 55 | 80 | - | dB |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | (to $V_{DDA}$) | | | | | |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

## 4.16. Comparators characteristics

**Table 4-39. CMP characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SU}$ | Setup Time | - | - | 5.5 | - | μs |
| $V_{OS}$ | Offset Voltage | - | - | 2 | - | mV |
| $t_D$ | Propagation delay | $V_{STEP}$ = 200 mV | - | 24 | - | ns |
| | | Full Range | - | 30 | - | |
| $I_{VDD}$ | Current consumption | - | - | 360 | - | μA |
| $I_{LEAK}$ | Leakage Current | - | - | 1 | - | nA |

(1) Guaranteed by design, not tested in production.

## 4.17. Trigonometric Math Unit (TMU) characteristics

The TMU unit has 9 different operation modes.

**Table 4-40. TMU supported instructions characteristics(1)**

| Mode Number | Operation | Cycles |
|---|---|---|
| 0 | R0 =x * 2π | 4 |
| 1 | R0 = x/2π | 4 |
| 2 | R0 = $\sqrt{x}$ | 7 |
| 3 | R0 =sin (x) | 7 |
| 4 | R0 = cos (x) | 7 |
| 5 | R0 = arctan (x) | 7 |
| 6 | R0 = Ratio of X & Y, R1 = Quadrant value (0.0, +/-0.25, +/-0.5) | 7 |
| 7 | R0 = x/y | 7 |
| 8 | R0 = $\sqrt{x^2+y^2}$ | 7 |

(1) Guaranteed by design, not tested in production.

## 4.18. I2C characteristics

**Table 4-41. I2C characteristics(1)(2)(3)**

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Fast mode plus | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{SCL(H)}$ | SCL clock high time | - | 4.0 | - | 0.6 | - | 0.2 | - | μs |
| $t_{SCL(L)}$ | SCL clock low time | - | 4.7 | - | 1.3 | - | 0.5 | - | μs |
| $t_{su(SDA)}$ | SDA setup time | - | 2 | - | 0.8 | - | 0.1 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{r(SDA/SCL)}$ | SDA and SCL rise time | - | - | 1000 | 20 | 300 | - | 120 | ns |
| $t_{f(SDA/SCL)}$ | SDA and SCL fall time | - | - | 300 | - | 300 | - | 120 | ns |
| $t_{h(STA)}$ | Start condition hold time | - | 4.0 | - | 0.6 | - | 0.26 | - | μs |

(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency, $f_{PCLK1}$ must be at least 2 MHz, To ensure the fast mode I2C frequency, $f_{PCLK1}$ must be at least 4 MHz. To ensure the fast mode plus I2C frequency, $f_{PCLK1}$ must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

**Figure 4-6. I2C bus timing diagram**

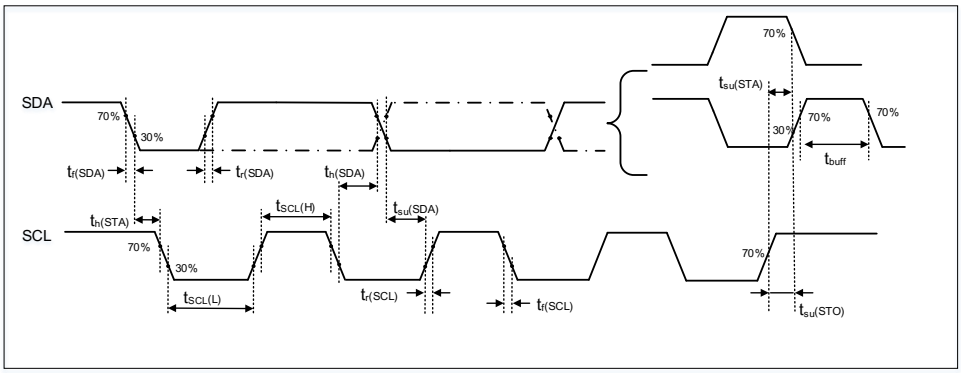



**Table 4-42. I2C analog filter delay characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{AF}$ | Analog filter delay time | - | 50 | 75 | 160 | ns |

(1) Guaranteed by design, not tested in production.

## 4.19. SPI characteristics

**Table 4-43. Standard SPI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | - | - | - | 22.5 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | Master mode, $f_{PCLKx}$ = 90 MHz, presc = 4 | - | 22.2 | - | ns |
| $t_{SCK(L)}$ | SCK clock low time | Master mode, $f_{PCLKx}$ = 90 MHz, presc = 4 | - | 22.2 | - | ns |
| **SPI master mode** | | | | | | |
| $t_{V(MO)}$ | Data output valid time | - | - | - | 10 | ns |
| $t_{SU(MI)}$ | Data input setup time | - | 1 | - | - | ns |
| $t_{H(MI)}$ | Data input hold time | - | 0 | - | - | ns |
| **SPI slave mode** | | | | | | |
| $t_{SU(NSS)}$ | NSS enable setup time | - | 0 | - | - | ns |
| $t_{H(NSS)}$ | NSS enable hold time | - | 1 | - | - | ns |
| $t_{A(SO)}$ | Data output access time | - | - | 10 | - | ns |
| $t_{DIS(SO)}$ | Data output disable time | - | - | 11 | - | ns |
| $t_{V(SO)}$ | Data output valid time | - | - | 11 | - | ns |
| $t_{SU(SI)}$ | Data input setup time | - | 0 | - | - | ns |
| $t_{H(SI)}$ | Data input hold time | - | 1 | - | - | ns |

(1) Based on characterization, not tested in production.

**Figure 4-7. SPI timing diagram – master mode**

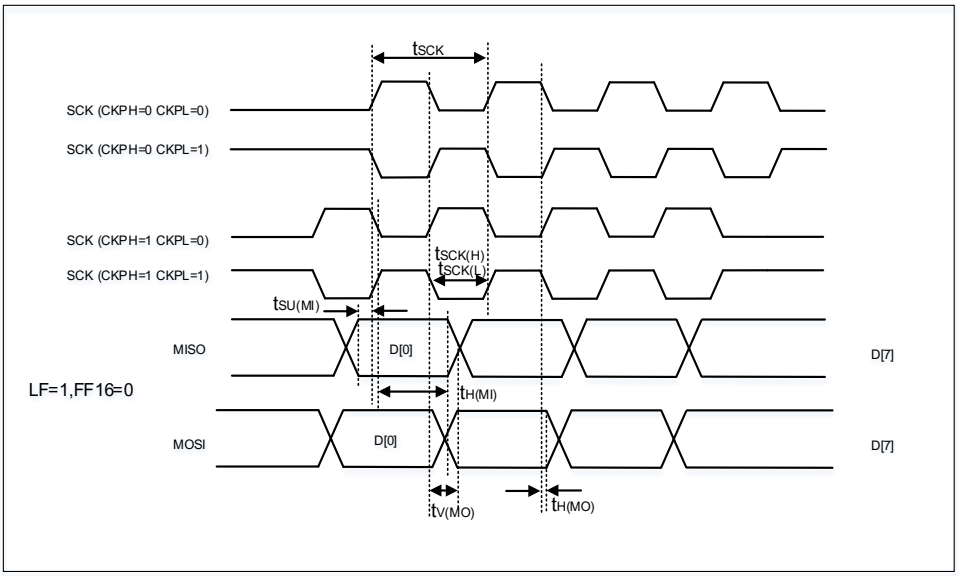
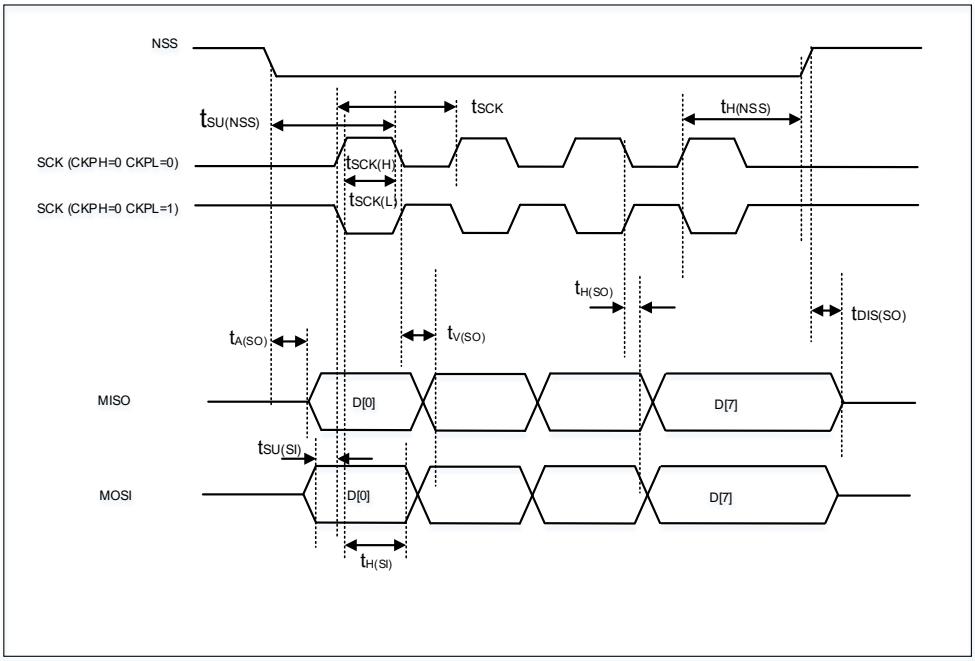


**Figure 4-8. SPI timing diagram – slave mode**



## 4.20. I2S characteristics

**Table 4-44. I2S characteristics(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | Clock frequency | Master mode (data: 32 bits, Audio frequency = 96 kHz) | - | 6.21 | - | MHz |
| | | Slave mode | - | - | 12.5 | |
| $t_H$ | Clock high time | - | - | 81 | - | ns |
| $t_L$ | Clock low time | | - | 81 | - | ns |
| $t_{V(WS)}$ | WS valid time | Master mode | - | 3 | - | ns |
| $t_{H(WS)}$ | WS hold time | Master mode | - | 3 | - | ns |
| $t_{SU(WS)}$ | WS setup time | Slave mode | 0 | - | - | ns |
| $t_{H(WS)}$ | WS hold time | Slave mode | 2 | - | - | ns |
| $Ducy_{(SCK)}$ | I2S slave input clock duty cycle | Slave mode | - | 50 | - | % |
| $t_{SU(SD_MR)}$ | Data input setup time | Master mode | 1 | - | - | ns |
| $t_{SU(SD_SR)}$ | Data input setup time | Slave mode | 0 | - | - | ns |
| $t_{H(SD_MR)}$ | Data input hold time | Master receiver | 0 | - | - | ns |
| $t_{H(SD_SR)}$ | | Slave receiver | 1 | - | - | ns |
| $t_{V(SD_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | - | 10 | ns |
| $t_{H(SD_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 3 | - | - | ns |
| $t_{V(SD_MT)}$ | Data output valid time | Master transmitter (after enable edge) | - | - | 10 | ns |
| $t_{H(SD_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 0 | - | - | ns |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production

**Figure 4-9. I2S timing diagram – master mode**

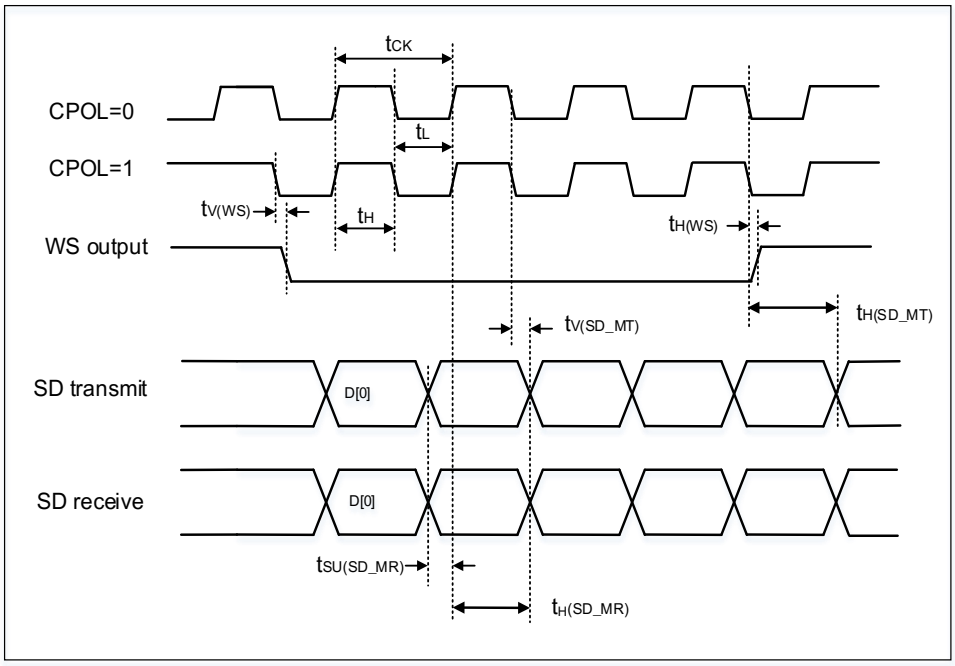
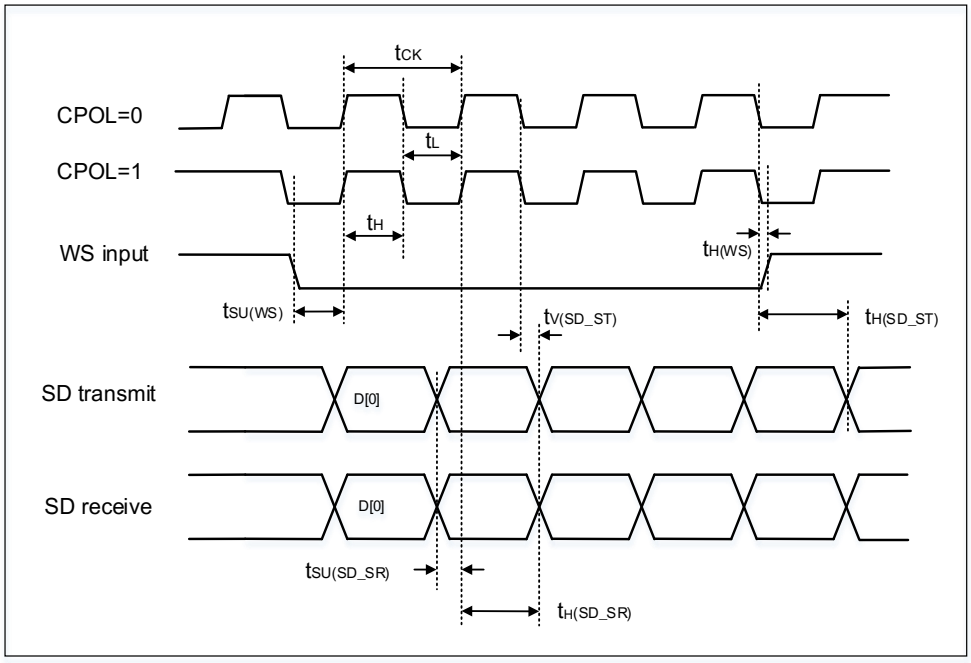



**Figure 4-10. I2S timing diagram – slave mode**



## 4.21. USART characteristics

**Table 4-45. USART characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | $f_{PCLKx}$ = 180 MHz | - | - | 90 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | $f_{PCLKx}$ = 180 MHz | 5 | - | - | ns |
| $t_{SCK(L)}$ | SCK clock low time | $f_{PCLKx}$ = 180 MHz | 5 | - | - | ns |

(1) Guaranteed by design, not tested in production.

## 4.22. USBHS characteristics

**Table 4-46. USBHS DC electrical characteristics**

| Symbol | | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| VDD (2) | | USB operating voltage | - | 3 | - | 3.63 | V |
| **LS/FS FUNCTIONALITY** | | | | | | | |
| Input levels(1) | $V_{DIFS}$ | Differential input sensitivity(FS/LS) | - | 0.2 | - | - | V |
| | $V_{CMFS}$ | Differential common mode range(FS/LS) | Includes $V_{DI}$ range | 0.8 | - | 2.5 | |
| | $V_{ILSE}$ | Single ended receiver low level input voltage (FS/LS) | - | - | - | 0.8 | |
| | $V_{IHSE}$ | Single ended receiver high level input voltage (FS/LS) | - | 2.0 | - | - | |
| Output levels (2) | $V_{OLFS}$ | Static output level low(FS/LS) | $R_L$ of 1.0 kΩ to 3.63 V | - | - | 0.3 | V |
| | $V_{OHFS}$ | Static output level high(FS/LS) | $R_L$ of 15 kΩ to $V_{SS}$ | 2.8 | 3.3 | 3.63 | |
| $R_{PD}$(2) | | PA11, PA12(USBHS_DM/DP) | $V_{IN}$ = $V_{DD}$ | 17 | 21 | 25 | kΩ |
| | | PA9(USBHS_VBUS) | | 0.72 | 0.9 | 1.1 | |
| $R_{PU}$(2) | | PA11, PA12(USBHS_DM/DP) | $V_{IN}$ = $V_{SS}$ | 1.2 | 1.5 | 1.8 | |
| | | PA9(USBHS_VBUS) | | 0.24 | 0.3 | 0.33 | |
| $Z_{HSDRV}$(1) | | Driver Output Impedance | Steady state drive | 40.5 | 45 | 49.5 | Ω |
| **HS FUNCTIONALITY** | | | | | | | |
| Input levels(1) | $V_{DIHS}$ | Differential input sensitivity(HS) | - | 0.1 | - | - | V |
| | $V_{CMHS}$ | Differential common mode range(HS) | - | -50 | - | 500 | mV |
| | $V_{HSSQ}$ | HS Squelch Detection Threshold | - | 100 | - | 150 | mV |
| | $V_{HSDSC}$ | HS Disconnect Threshold | - | 525 | - | 625 | mV |
| Output levels(1) | $V_{OLHS}$ | High speed low level output voltage | 45Ω load | -10 | - | 10 | mV |
| | $V_{OHHS}$ | High speed high level output voltage | 45Ω load | 360 | 400 | 440 | mV |

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.

**Table 4-47. USBHS dynamic characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{FR}$ | Rise time(FS/LS) | $C_L$ = 50 pF | 4 | 5 | 20 | ns |
| $T_{HSR}$ | Differential Rise Time(HS) | - | 500 | 600 | - | ps |
| $T_{FF}$ | Fall time(FS/LS) | $C_L$ = 50 pF | 4 | 5 | 20 | ns |
| $T_{HSF}$ | Differential Fall Time(HS) | - | 500 | 600 | - | ps |
| $t_{RFM}$ | Rise/ fall time matching(FS/LS) | $t_R$ / $t_F$ | 90 | - | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage(FS/LS) | - | 1.3 | - | 2.0 | V |

(1) Guaranteed by design, not tested in production.

**Table 4-48. USBHS Charger Detection characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DAT_SRC}$ | Data Source Voltage | - | 0.5 | - | 0.7 | V |
| $I_{DP_SRC}$ | Data Connect Current | - | 7 | - | 13 | uA |
| $V_{DAT_REF}$ | Data Detect Voltage | - | 0.25 | - | 0.4 | V |

(1) Guaranteed by design, not tested in production.

**Table 4-49. USBHS clock timing parameters(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | USBHS operating voltage | 3.0 | - | 3.63 | V |
| $f_{HCLK}$ | $f_{HCLK}$ value to guarantee proper operation of USBHS interface | 30 | - | - | MHz |
| $F_{START_8BIT}$ | Frequency (first transition) 8-bit +/- 10% | 54 | 60 | 66 | MHz |
| $F_{STEADY}$ | Frequency (steady state) +/-500 ppm | 59.97 | 60 | 60.63 | MHz |
| $D_{START_8BIT}$ | Duty cycle (first transition) 8-bit +/- 10% | 40 | 50 | 60 | % |
| $D_{STEADY}$ | Duty cycle (steady state) +/-500 ppm | 49.975 | 50 | 50.025 | % |

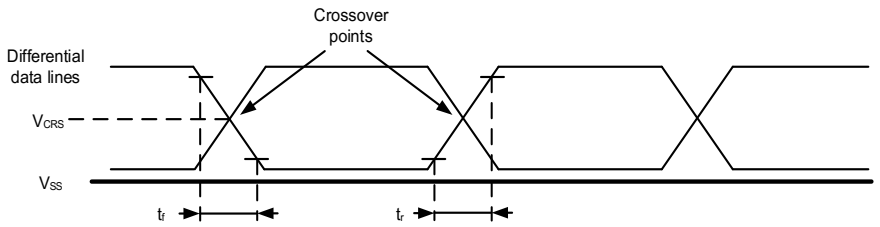
(1) Guaranteed by design, not tested in production.

**Table 4-50. USB-ULPI Dynamic characteristics(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SC}$ | Control in (ULPI_DIR, ULPI_NXT) setup time | - | - | 2 | ns |
| $t_{HC}$ | Control in (ULPI_DIR, ULPI_NXT) hold time | 0.5 | - | - | ns |
| $t_{SD}$ | Data in setup time | - | - | 2 | ns |
| $t_{HD}$ | Data in hold time | 0 | - | - | ns |

(1) Guaranteed by design, not tested in production.

**Figure 4-11. USBFS timings: definition of data signal rise and fall time**



## 4.23. EXMC characteristics

**Table 4-51. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)(3)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | EXMC_NE low time | 27 | 29 | ns |
| $t_{V(NOE_NE)}$ | EXMC_Nex low to EXMC_NOE low | 0 | - | ns |
| $t_{w(NOE)}$ | EXMC_NOE low time | 27 | 29 | ns |
| $t_{h(NE_NOE)}$ | EXMC_NOE high to EXMC_NE high hold time | 0 | - | ns |
| $t_{v(A_NE)}$ | EXMC_Nex low to EXMC_A valid | 0 | - | ns |
| $t_{v(BL_NE)}$ | EXMC_Nex low to EXMC_BL valid | 0 | - | ns |
| $t_{su(DATA_NE)}$ | Data to EXMC_Nex high setup time | 21.4 | - | ns |
| $t_{su(DATA_NOE)}$ | Data to EXMC_NOEx high setup time | 21.4 | - | ns |
| $t_{h(DATA_NOE)}$ | Data hold time after EXMC_NOE high | 0 | - | ns |
| $t_{h(DATA_NE)}$ | Data hold time after EXMC_Nex high | 0 | - | ns |
| $t_{v(NADV_NE)}$ | EXMC_Nex low to EXMC_NADV low | 0 | - | ns |
| $t_{w(NADV)}$ | EXMC_NADV low time | 4.6 | 6.6 | ns |

(1) $C_L$ = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: $f_{HCLK}$ = 180 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

**Table 4-52. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)(3)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | EXMC_NE low time | 15.8 | 17.8 | ns |
| $t_{V(NWE_NE)}$ | EXMC_Nex low to EXMC_NWE low | 4.6 | - | ns |
| $t_{w(NWE)}$ | EXMC_NWE low time | 4.6 | 6.6 | ns |
| $t_{h(NE_NWE)}$ | EXMC_NWE high to EXMC_NE high hold time | 4.6 | 6.6 | ns |
| $t_{v(A_NE)}$ | EXMC_Nex low to EXMC_A valid | 0 | - | ns |
| $t_{V(NADV_NE)}$ | EXMC_Nex low to EXMC_NADV low | 0 | - | ns |
| $t_{w(NADV)}$ | EXMC_NADV low time | 4.6 | 6.6 | ns |
| $t_{h(AD_NADV)}$ | EXMC_AD(address) valid hold time after EXMC_NADV high | 10.2 | - | ns |
| $t_{h(A_NWE)}$ | Address hold time after EXMC_NWE high | 4.6 | - | ns |
| $t_{h(BL_NWE)}$ | EXMC_BL hold time after EXMC_NWE high | 4.6 | - | ns |
| $t_{v(BL_NE)}$ | EXMC_Nex low to EXMC_BL valid | 15.8 | 17.8 | ns |
| $t_{v(DATA_NADV)}$ | EXMC_NADV high to DATA valid | 4.6 | - | ns |
| $t_{h(DATA_NWE)}$ | Data hold time after EXMC_NWE high | 4.6 | 6.6 | ns |

(1) $C_L$ = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: $f_{HCLK}$ = 180 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

**Table 4-53. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | EXMC_NE low time | 38.2 | 40.2 | ns |
| $t_{V(NOE_NE)}$ | EXMC_Nex low to EXMC_NOE low | 15.8 | - | ns |
| $t_{w(NOE)}$ | EXMC_NOE low time | 21.4 | 23.4 | ns |
| $t_{h(NE_NOE)}$ | EXMC_NOE high to EXMC_NE high hold time | 0 | - | ns |
| $t_{v(A_NE)}$ | EXMC_Nex low to EXMC_A valid | 0 | - | ns |
| $t_{v(A_NOE)}$ | Address hold time after EXMC_NOE high | 0 | - | ns |
| $t_{v(BL_NE)}$ | EXMC_Nex low to EXMC_BL valid | 0 | - | ns |
| $t_{h(BL_NOE)}$ | EXMC_BL hold time after EXMC_NOE high | 0 | - | ns |
| $t_{su(DATA_NE)}$ | Data to EXMC_Nex high setup time | 22.4 | - | ns |
| $t_{su(DATA_NOE)}$ | Data to EXMC_NOEx high setup time | 22.4 | - | ns |
| $t_{h(DATA_NOE)}$ | Data hold time after EXMC_NOE high | 0 | - | ns |
| $t_{h(DATA_NE)}$ | Data hold time after EXMC_Nex high | 0 | - | ns |
| $t_{v(NADV_NE)}$ | EXMC_Nex low to EXMC_NADV low | 0 | - | ns |
| $t_{w(NADV)}$ | EXMC_NADV low time | 4.6 | 6.6 | ns |
| $T_{h(AD_NADV)}$ | EXMC_AD(ddress) valid hold time after EXMC_NADV high | 4.6 | 6.6 | ns |

(1) $C_L$ = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: $f_{HCLK}$ = 180 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

**Table 4-54. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | EXMC_NE low time | 27 | 29 | ns |
| $t_{V(NWE_NE)}$ | EXMC_Nex low to EXMC_NWE low | 7.3 | - | ns |
| $t_{w(NWE)}$ | EXMC_NWE low time | 15.8 | 17.8 | ns |
| $t_{h(NE_NWE)}$ | EXMC_NWE high to EXMC_NE high hold time | 4.6 | - | ns |
| $t_{v(A_NE)}$ | EXMC_Nex low to EXMC_A valid | 0 | - | ns |
| $t_{V(NADV_NE)}$ | EXMC_Nex low to EXMC_NADV low | 0 | - | ns |
| $t_{w(NADV)}$ | EXMC_NADV low time | 4.6 | 6.6 | ns |
| $t_{h(AD_NADV)}$ | EXMC_AD(address) valid hold time after EXMC_NADV high | 4.6 | - | ns |
| $t_{h(A_NWE)}$ | Address hold time after EXMC_NWE high | 4.6 | - | ns |
| $t_{h(BL_NWE)}$ | EXMC_BL hold time after EXMC_NWE high | 4.6 | - | ns |
| $t_{v(BL_NE)}$ | EXMC_Nex low to EXMC_BL valid | 0 | - | ns |
| $t_{v(DATA_NADV)}$ | EXMC_NADV high to DATA valid | 4.6 | - | ns |
| $t_{h(DATA_NWE)}$ | Data hold time after EXMC_NWE high | 4.6 | - | ns |

(1) $C_L$ = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: $f_{HCLK}$ = 180 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

**Table 4-55. Synchronous multiplexed PSRAM/NOR read timings(1)(2)(3)(4)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | EXMC_CLK period | 22.4 | - | ns |
| $t_{d(CLKL-NexL)}$ | EXMC_CLK low to EXMC_Nex low | 0 | - | ns |
| $t_{d(CLKH-NexH)}$ | EXMC_CLK high to EXMC_Nex high | 10.2 | - | ns |
| $t_{d(CLKL-NADVL)}$ | EXMC_CLK low to EXMC_NADV low | 0 | - | ns |
| $t_{d(CLKL-NADVH)}$ | EXMC_CLK low to EXMC_NADV high | 0 | - | ns |
| $t_{d(CLKL-AV)}$ | EXMC_CLK low to EXMC_Ax valid | 0 | - | ns |
| $t_{d(CLKH-AIV)}$ | EXMC_CLK high to EXMC_Ax invalid | 10.2 | - | ns |
| $t_{d(CLKL-NOEL)}$ | EXMC_CLK low to EXMC_NOE low | 0 | - | ns |
| $t_{d(CLKH-NOEH)}$ | EXMC_CLK high to EXMC_NOE high | 10.2 | - | ns |
| $t_{d(CLKL-ADV)}$ | EXMC_CLK low to EXMC_AD valid | 0 | - | ns |
| $t_{d(CLKL-ADIV)}$ | EXMC_CLK low to EXMC_AD invalid | 0 | - | ns |

(1) $C_L$ = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: $f_{HCLK}$ = 180 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

**Table 4-56. Synchronous multiplexed PSRAM write timings(1)(2)(3)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | EXMC_CLK period | 22.4 | - | ns |
| $t_{d(CLKL-NexL)}$ | EXMC_CLK low to EXMC_Nex low | 0 | - | ns |
| $t_{d(CLKH-NexH)}$ | EXMC_CLK high to EXMC_Nex high | 10.2 | - | ns |
| $t_{d(CLKL-NADVL)}$ | EXMC_CLK low to EXMC_NADV low | 0 | - | ns |
| $t_{d(CLKL-NADVH)}$ | EXMC_CLK low to EXMC_NADV high | 0 | - | ns |
| $t_{d(CLKL-AV)}$ | EXMC_CLK low to EXMC_Ax valid | 0 | - | ns |
| $t_{d(CLKH-AIV)}$ | EXMC_CLK high to EXMC_Ax invalid | 10.2 | - | ns |
| $t_{d(CLKL-NWEL)}$ | EXMC_CLK low to EXMC_NWE low | 0 | - | ns |
| $t_{d(CLKH-NWEH)}$ | EXMC_CLK high to EXMC_NWE high | 10.2 | - | ns |
| $t_{d(CLKL-ADIV)}$ | EXMC_CLK low to EXMC_AD invalid | 0 | - | ns |
| $t_{d(CLKL-DATA)}$ | EXMC_A/D valid data after EXMC_CLK low | 0 | - | ns |
| $t_{h(CLKL-NBLH)}$ | EXMC_CLK low to EXMC_NBL high | 0 | - | ns |

(1) $C_L$ = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: $f_{HCLK}$ = 180 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

**Table 4-57. Synchronous non-multiplexed PSRAM/NOR read timings(1)(2)(3)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | EXMC_CLK period | 22.4 | - | ns |
| $t_{d(CLKL-NexL)}$ | EXMC_CLK low to EXMC_Nex low | 0 | - | ns |
| $t_{d(CLKH-NexH)}$ | EXMC_CLK high to EXMC_Nex high | 10.2 | - | ns |
| $t_{d(CLKL-NADVL)}$ | EXMC_CLK low to EXMC_NADV low | 0 | - | ns |
| $t_{d(CLKL-NADVH)}$ | EXMC_CLK low to EXMC_NADV high | 0 | - | ns |
| $t_{d(CLKL-AV)}$ | EXMC_CLK low to EXMC_Ax valid | 0 | - | ns |
| $t_{d(CLKH-AIV)}$ | EXMC_CLK high to EXMC_Ax invalid | 10.2 | - | ns |
| $t_{d(CLKL-NOEL)}$ | EXMC_CLK low to EXMC_NOE low | 0 | - | ns |
| $t_{d(CLKH-NOEH)}$ | EXMC_CLK high to EXMC_NOE high | 10.2 | - | ns |

(1) $C_L$ = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: HCLK=180 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

**Table 4-58. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | EXMC_CLK period | 22.4 | - | ns |
| $t_{d(CLKL-NexL)}$ | EXMC_CLK low to EXMC_Nex low | 0 | - | ns |
| $t_{d(CLKH-NexH)}$ | EXMC_CLK high to EXMC_Nex high | 10.2 | - | ns |
| $t_{d(CLKL-NADVL)}$ | EXMC_CLK low to EXMC_NADV low | 0 | - | ns |
| $t_{d(CLKL-NADVH)}$ | EXMC_CLK low to EXMC_NADV high | 0 | - | ns |
| $t_{d(CLKL-AV)}$ | EXMC_CLK low to EXMC_Ax valid | 0 | - | ns |
| $t_{d(CLKH-AIV)}$ | EXMC_CLK high to EXMC_Ax invalid | 10.2 | - | ns |
| $t_{d(CLKL-NWEL)}$ | EXMC_CLK low to EXMC_NWE low | 0 | - | ns |
| $t_{d(CLKH-NWEH)}$ | EXMC_CLK high to EXMC_NWE high | 10.2 | - | ns |
| $t_{d(CLKL-DATA)}$ | EXMC_A/D valid data after EXMC_CLK low | 0 | - | ns |
| $t_{h(CLKL-NBLH)}$ | EXMC_CLK low to EXMC_NBL high | 0 | - | ns |

(1) $C_L$ = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: HCLK = 180 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

## 4.24. Serial/Quad Parallel Interface (SQPI) characteristics

**Table 4-59.SQPI characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CLK}$(2) | CLK period | 11.0(4) | - | - | ns |
| $t_{CD}$(2) | CLK high level duty for even clock divided | 45 | 50 | 55 | % |
| | CLK high level duty for odd clock divided | 45 | - | 71 | |
| $t_{KHKL}$(3) | CLK rise or fall time | - | - | 3 | ns |
| $t_{CPH}$(2) | CE# high between subsequent burst operations | 22.2 | - | - | ns |
| $t_{CEM}$(2) | CE# low pulse width | 88.8 | - | - | ns |
| $t_{CSP}$(2) | CE# setup time to CLK rising edge | 5.5 | - | 177.7 | ns |
| $t_{CHD}$(2) | CE# hold time from CLK rising edge | 5.5 | - | 177.7 | ns |
| $t_{SP}$(2) | Setup time to active CLK edge | 5.5 | - | 177.7 | ns |
| $t_{HD}$(2) | Hold time from active CLK edge | 5.5 | - | 177.7 | ns |
| $t_{HZ}$(2) | CE# rise to data output high-Z | - | 0 | - | ns |
| $t_{ACLK}$(2) | CLK fall to data output valid delay | - | 0 | - | ns |
| $t_{KOH}$(2) | Data hold time from CLK falling edge | - | 0 | - | ns |

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Output driven mode is 50 MHz. Measured from 10% to 90% of VDD.
(4) This is designed minimal period. The operating minimal clock period is 22.2 ns(45 MHz = 180 MHz/4).

## 4.25. Super High-resolution Timer (SHRTIMER) characteristics

**Table 4-60. SHRTIMER characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_A$ | Timer ambient temperature range | $f_{SHRTIMER}$ = 180 MHz | -40 | - | 85 | ℃ |
| $f_{SHRTIMER}$ | SHRTIMER input clock for DLL | Under $T_A$ conditions | - | 180 | - | MHz |
| $t_{SHRTIMER}$ | | | - | 5.56 | - | ns |
| $t_{res(SHRTIMER)}$ | Timer resolution time | $f_{HPMER}$ = 180 MHz | - | 86.8 | - | ps |
| $RES_{SHRTIMER}$ | Timer resolution | - | - | - | 16 | bit |
| $t_{DTG}$ | Dead time generator clock period | - | 1/64 | - | 16 | $t_{SHRTIMER}$ |
| | | $f_{SHRTIMER}$ = 180 MHz | 0.0868 | - | 88.89 | ns |
| $\|t_{DTR}\|$ / $\|t_{DTF}\|$ | Dead time range (absolute value) | - | - | - | 2^16-1 | $t_{DTG}$ |
| | | $f_{SHRTIMER}$ = 180 MHz | - | - | 5825.41 | µs |
| $f_{CHPFRQ}$ | Chopper stage clock frequency | - | 1/256 | - | 1/16 | $f_{SHRTIMER}$ |
| | | $f_{SHRTIMER}$ = 180 MHz | 0.703 | - | 11.25 | MHz |
| $t_{1STPW}$ | Chopper first pulse length | - | 16 | - | 256 | $t_{SHRTIMER}$ |
| | | $f_{SHRTIMER}$ = 180 MHz | 0.089 | - | 1.42 | µs |

(1) Guaranteed by design, not tested in production.

**Table 4-61. SHRTIMER output response to fault protection(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $t_{LAT(DF)}$ | Digital fault response latency | Propagation delay from SHRTIMER_FLTx digital input to SHRTIMER_StxCHy output pin | - | - | 25 | ns |
| $t_{W(FLT)}$ | Minimum fault pulse width | - | 11 | - | - | |
| $t_{LAT(AF)}$ | Analog fault response latency | Propagation delay from comparator CMPx_Ipx input to SHRTIMER_StxCHy output pin | - | - | 35 | |

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.

**Table 4-62. SHRTIMER output response to external 1 to 10(Synchronous mode(1))**

| Symbol | Parameter | Conditions | Min | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $T_{PROP(SHRTIMER)}$ | External event response latency in SHRTIMER | SHRTIMER internal propagation delay(3) | 5 | - | 6 | $t_{SHRTIMER}$(2) |
| $t_{LAT(DEEV)}$ | Digital external event response latency | Propagation delay from SHRTIMER_EXEVx digital input to SHRTIMER_StxCHy output pin(30pF load) (3) | - | - | 48 | ns |
| $t_{W(FLT)}$ | Minimum external event pulse width | - | 11 | - | - | |
| $t_{LAT(AEEV)}$ | Analog external event response latency | Propagation delay from comparator CMPx_Ipx input pin to SHRTIMER_StxCHy output pin(30pF load) (3) | - | - | 60 | |
| $T_{JIT(EEV)}$ | External event response jitter | Jitter of the delay from SHRTIMER_EXEVx digital input or CMPx_Ipx input pin to SHRTIMER_StxCHy output pin(30pF load) | - | - | 1 | $t_{SHRTIMER}$(2) |
| $T_{JIT(PW)}$ | Jitter on output pulse width in response to an external event | - | - | - | 0 | $t_{SHRTIMER}$(2) |

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.
(3) $t_{SHRTIMER} = 1 / f_{SHRTIMER}$ with $f_{SHRTIMER} = 180$ MHz depending on the clock controller configuration.
(4) This parameter does not take into account latency introduced by GPIO or comparator.

**Table 4-63. SHRTIMER synchronization input / output(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $t_{W(SYNCIN)}$ | Minimum pulse width on SYNCIN inputs, including SHRTIMER_SCIN | - | 2 | - | - | $t_{SHRTIMER}$ |
| $t_{LAT(DF)}$ | Response time to external synchronization request | - | - | - | 1 | $t_{SHRTIMER}$ |
| $t_{W(AF)}$ | Pulse width on SHRTIMER_SCOUT output | - | - | 16 | - | $t_{SHRTIMER}$ |
| | | $f_{SHRTIMER}$ = 180 MHz | - | 88.89 | - | ns |

(1) Guaranteed by design, not tested in production.

## 4.26. TIMER characteristics

**Table 4-64. TIMER characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res}$ | Timer resolution time | - | 1 | - | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK}$ = 180 MHz | 5.6 | - | ns |
| $f_{EXT}$ | Timer external clock frequency | - | 0 | $f_{TIMERxCLK}/2$ | MHz |
| | | $f_{TIMERxCLK}$ = 180 MHz | 0 | 90 | MHz |
| RES | Timer resolution | TIMERx (except TIMER1) | - | 16 | bit |
| | | TIMER1 | - | 32 | |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | - | 1 | 65536 | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK}$ = 180 MHz | 0.0056 | 364.1 | μs |
| | 32-bit counter clock period when internal clock is selected ( only TIMER1 ) | - | 1 | $2^{32}$ | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK}$ = 180 MHz | 0.0056 | 23.86 | S |
| $t_{MAX_COUNT}$ | Maximum possible count ( except TIMER1 ) | - | - | $2^{16} \times 2^{16}$ | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK}$ = 180 MHz | - | 23.86 | s |
| | Maximum possible count ( only TIMER1 ) | - | - | $2^{16} \times 2^{32}$ | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK}$ = 180 MHz | - | $2^{16} \times 23.86$ | s |

(1) Guaranteed by design, not tested in production.

## 4.27. WDGT characteristics

**Table 4-65. FWDGT min/max timeout period at 40 kHz (IRC40K)(1)**

| Prescaler divider | PSC[2:0] bits | Min timeout RLD[11:0] = 0x000 | Max timeout RLD[11:0] = 0xFFF | Unit |
|---|---|---|---|---|
| 1/4 | 000 | 0.025 | 409.525 | ms |
| 1/8 | 001 | 0.025 | 819.025 | |
| 1/16 | 010 | 0.025 | 1638.025 | |
| 1/32 | 011 | 0.025 | 3276.025 | |
| 1/64 | 100 | 0.025 | 6552.025 | |
| 1/128 | 101 | 0.025 | 13104.025 | |
| 1/256 | 110 or 111 | 0.025 | 26208.025 | |

(1) Guaranteed by design, not tested in production.

**Table 4-66. WWDGT min-max timeout value at 90 MHz ($f_{PCLK1}$)(1)**

| Prescaler divider | PSC[1:0] | Min timeout value CNT[6:0] = 0x40 | Unit | Max timeout value CNT[6:0] = 0x7F | Unit |
|---|---|---|---|---|---|
| 1/1 | 00 | 45.51 | µs | 2.91 | ms |
| 1/2 | 01 | 91.02 | | 5.83 | |
| 1/4 | 10 | 182.04 | | 11.65 | |
| 1/8 | 11 | 364.08 | | 23.30 | |

(1) Guaranteed by design, not tested in production.

## 4.28. Parameter condition

Unless otherwise specified, all values given for $V_{DD}$ = $V_{DDA}$ = 3.3 V, $T_A$ = 25 °C.

# 5. Package information

## 5.1. LQFP144 package outline dimensions

**Figure 5-1. LQFP144 package outline**

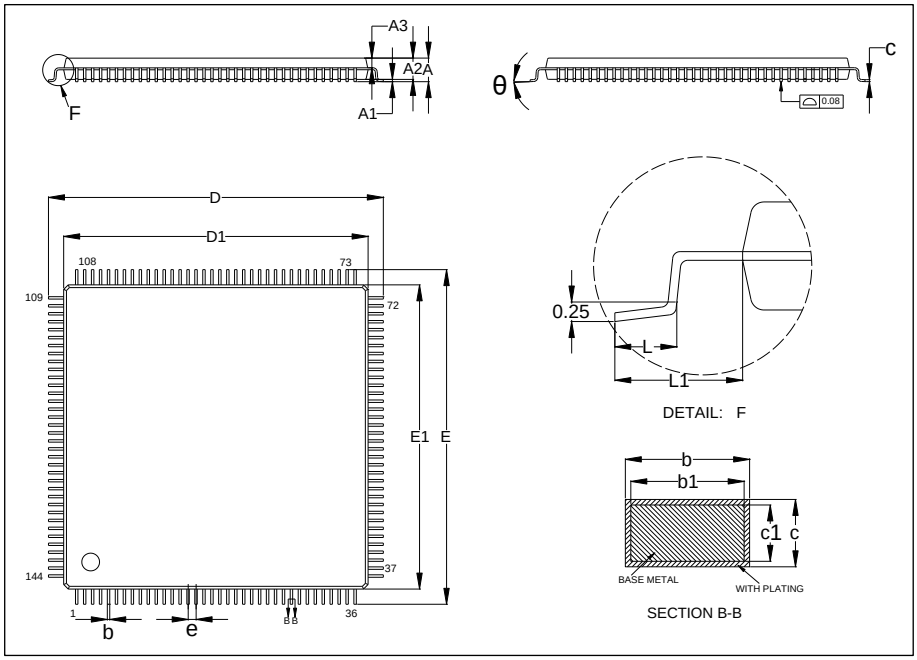
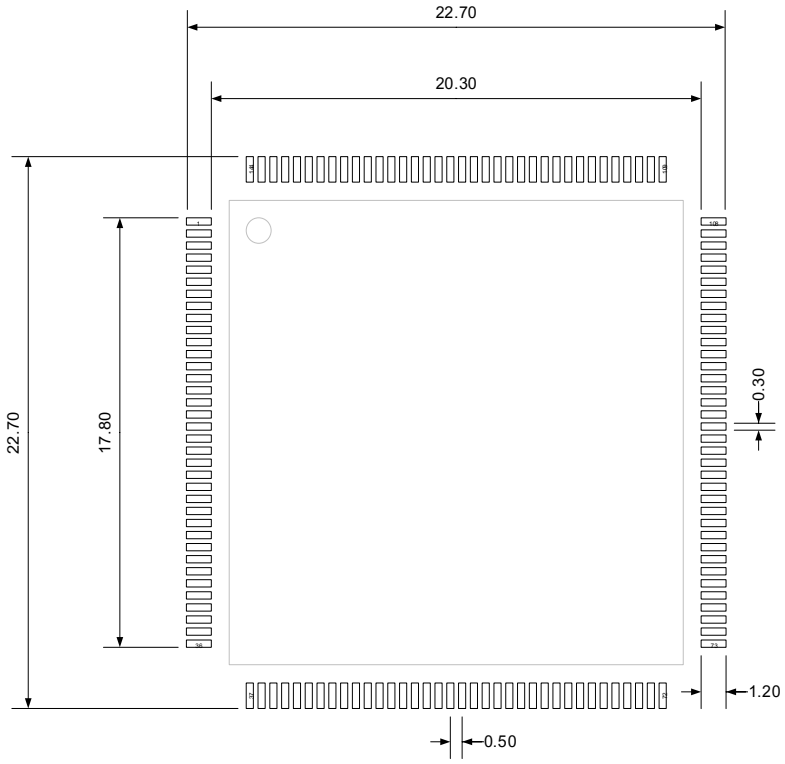



**Table 5-1. LQFP144 package dimensions**

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 21.80 | 22.00 | 22.20 |
| D1 | 19.90 | 20.00 | 20.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| e | - | 0.50 | - |
| L | 0.45 | - | 0.75 |
| L1 | - | 1.00 | - |
| θ | 0° | - | 7° |

(Original dimensions are in millimeters)

**Figure 5-2. LQFP144 recommended footprint**




(Original dimensions are in millimeters)

## 5.2. LQFP100 package outline dimensions

**Figure 5-3. LQFP100 package outline**

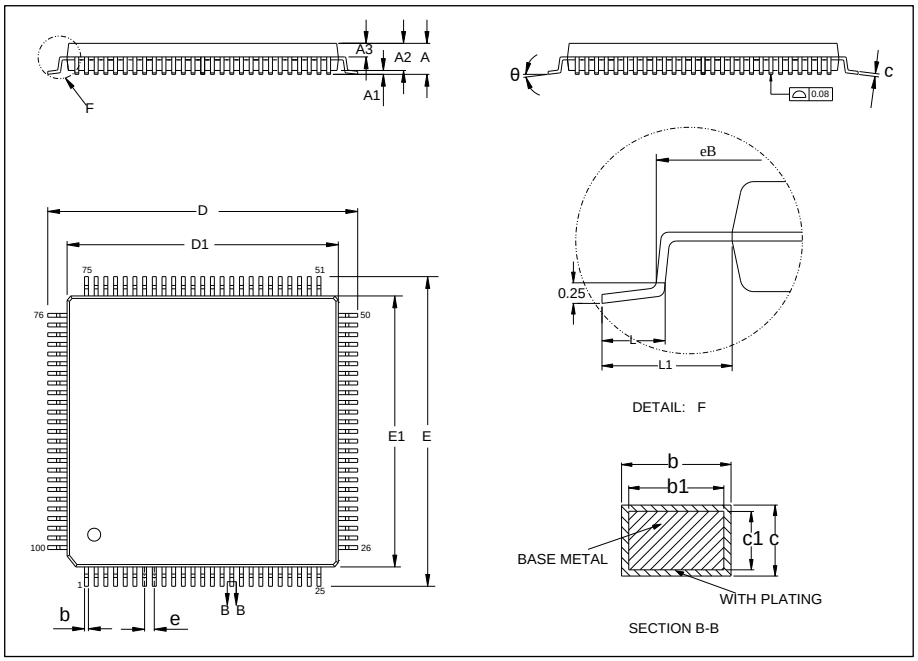
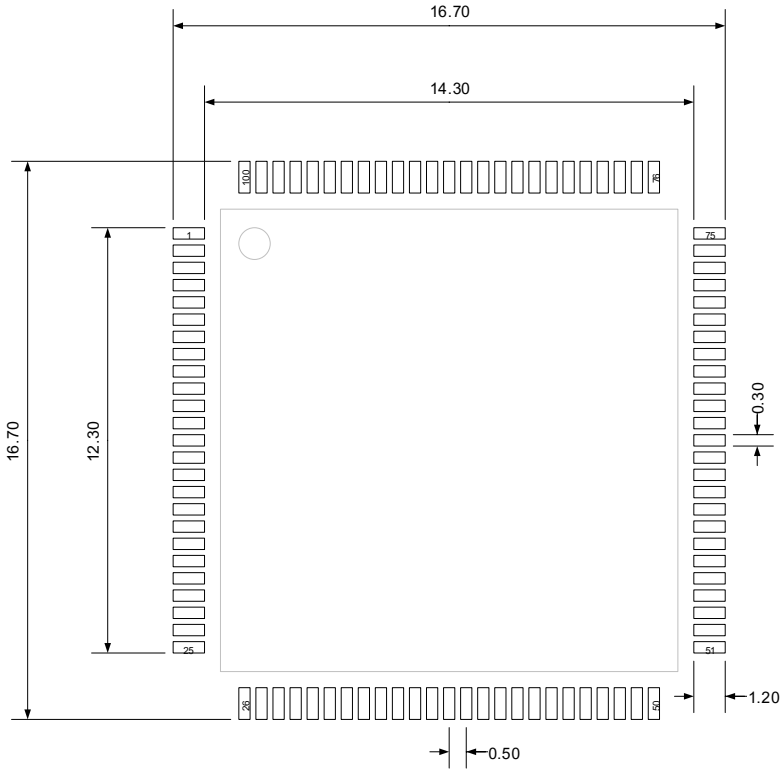



**Table 5-2. LQFP100 package dimensions**

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.10 |
| e | - | 0.50 | - |
| eB | 15.05 | - | 15.35 |
| L | 0.45 | - | 0.75 |
| L1 | - | 1.00 | - |
| θ | 0° | - | 7° |

(Original dimensions are in millimeters)

**Figure 5-4. LQFP100 recommended footprint**




(Original dimensions are in millimeters)

## 5.3. LQFP64 package outline dimensions

**Figure 5-5. LQFP64 package outline**

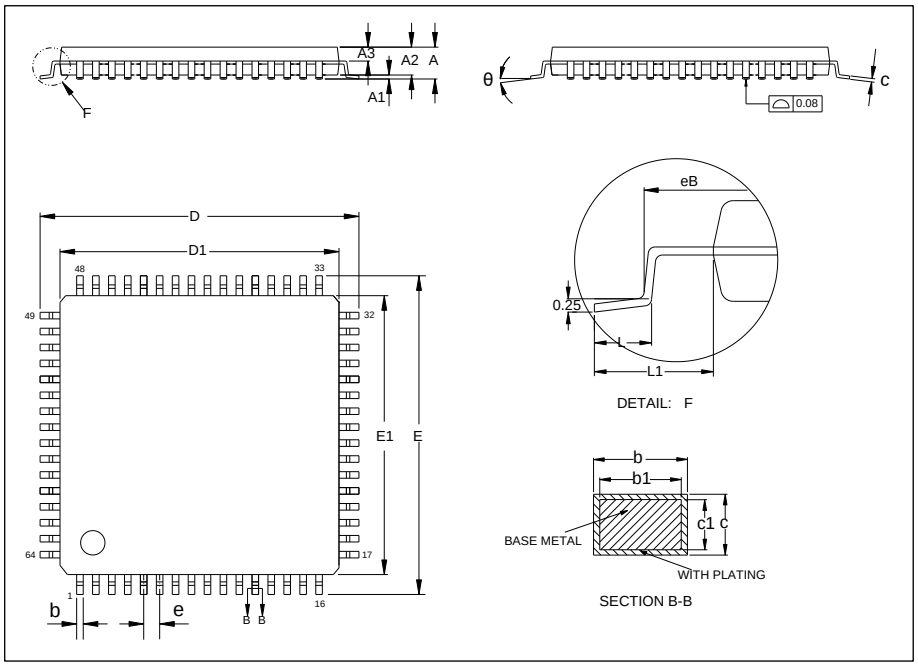
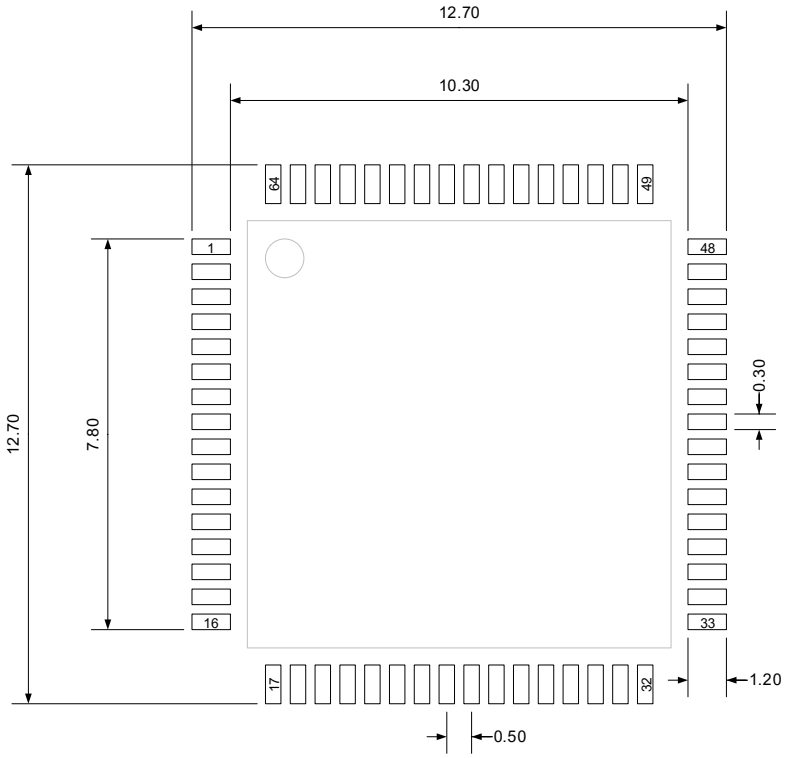



**Table 5-3. LQFP64 package dimensions**

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 11.80 | 12.00 | 12.20 |
| D1 | 9.90 | 10.00 | 10.10 |
| E | 11.80 | 12.00 | 12.20 |
| E1 | 9.90 | 10.00 | 10.10 |
| e | - | 0.50 | - |
| eB | 11.25 | - | 11.45 |
| L | 0.45 | - | 0.75 |
| L1 | - | 1.00 | - |
| θ | 0° | - | 7° |

(Original dimensions are in millimeters)

**Figure 5-6. LQFP64 recommended footprint**




(Original dimensions are in millimeters)

## 5.4. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

$\theta_{JA}$: Thermal resistance, junction-to-ambient.

$\theta_{JB}$: Thermal resistance, junction-to-board.

$\theta_{JC}$: Thermal resistance, junction-to-case.

$\Psi_{JB}$: Thermal characterization parameter, junction-to-board.

$\Psi_{JT}$: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, $T_J$ = Junction temperature.

$T_A$ = Ambient temperature

$T_B$ = Board temperature

$T_C$ = Case temperature which is monitoring on package surface

$P_D$ = Total power dissipation

$\theta_{JA}$ represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower $\theta_{JA}$ can be considerate as better overall thermal performance. $\theta_{JA}$ is generally used to estimate junction temperature.

$\theta_{JB}$ is used to measure the heat flow resistance between the chip surface and the PCB board.

$\theta_{JC}$ represents the thermal resistance between the chip surface and the package top case. $\theta_{JC}$ is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

**Table 5-4. Package thermal characteristics(1)**

| Symbol | Condition | Package | Value | Unit |
|---|---|---|---|---|
| $\theta_{JA}$ | Natural convection, 2S2P PCB | LQFP144 | 48.76 | °C/W |
| | | LQFP100 | 49.18 | |
| | | LQFP64 | 54.57 | |
| $\theta_{JB}$ | Cold plate, 2S2P PCB | LQFP144 | 35.00 | °C/W |
| | | LQFP100 | 22.70 | |
| | | LQFP64 | 35.08 | |
| $\theta_{JC}$ | Cold plate, 2S2P PCB | LQFP144 | 12.03 | °C/W |

| Symbol | Condition | Package | Value | Unit |
|---|---|---|---|---|
| | | LQFP100 | 12.52 | |
| | | LQFP64 | 18.11 | |
| $\Psi_{JB}$ | Natural convection, 2S2P PCB | LQFP144 | 35.32 | °C/W |
| | | LQFP100 | 32.85 | |
| | | LQFP64 | 35.41 | |
| $\Psi_{JT}$ | Natural convection, 2S2P PCB | LQFP144 | 1.86 | °C/W |
| | | LQFP100 | 0.53 | |
| | | LQFP64 | 1.10 | |

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

# 6. Ordering information

**Table 6-1. Part ordering code for GD32E507xx devices**

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---|---|---|---|---|
| GD32E507ZET6 | 512 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32E507ZCT6 | 256 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32E507VET6 | 512 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32E507VCT6 | 256 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32E507RET6 | 512 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32E507RCT6 | 256 | LQFP64 | Green | Industrial -40°C to +85°C |

# 7. Revision history

**Table 7-1. Revision history**

| Revision No. | Description | Date |
|---|---|---|
| 1.0 | Initial Release | Feb.28, 2020 |
| 1.1 | 1. Module information modification, refers to ***Functional description***. | Aug.28, 2020 |
| 1.2 | 1. Add deep-sleep 1 and deep-sleep 2 mode power consumption data, refers to ***Power consumption***, and modify the LDO mode conditions.<br>1. Electrical characteristics table update, refers to ***Electrical characteristics***. | Dec.7, 2020 |
| 1.3 | 1. Add CAN module related information.<br>2. Modify I2C and SPI timing diagrams, refers to ***I2C characteristics*** and ***SPI characteristics***.<br>3. CAN module description modification, refers to ***Controller area network (CAN)***. | Mar.24, 2021 |
| 1.4 | 1. Delete the OSCIN from PD0 remap information in chapter 2.6, and delete OSCOUT from PD1 remap information in chapter 2.6, , and delete PD0 / PD1 from OSCIN / OSCOUT remap information in chapter 2.6.3, delete ETM related functions in chapter 2.6, refers to ***Pin definitions***.<br>2. Modify pinouts, refers to ***Pinouts and pin assignment***.<br>3. Update SPI and I2S timing diagrams, refers to ***SPI characteristics*** and ***I2S characteristics***.<br>4. Update package information and ordering information, refers to ***Package information*** and ***Ordering information***. | Dec.14, 2021 |
| 1.5 | 1. Add $P_D$ parameter in ***Table 4-1. Absolute maximum ratings(1)(4)*** .<br>2. Add EMI parameter, refers to ***Table 4-9. EMI characteristics(1)***.<br>3. Modify LQFP64 package information, refer to ***LQFP64 package outline dimensions***.<br>4. Update NRST external pin circuit, refer to ***Figure 4-4. Recommended external NRST pin circuit(1)*** .<br>5. Change parameters in DC operating conditions, refer to ***Table 4-2. DC operating conditions***.<br>6. EXMC related pin update, refer to ***Pin definitions***. | Jun.30, 2022 |
| 1.6 | 1. Pin name modification in ***Pin definitions*** and ***Pinouts and pin assignment***.<br>2. Add TRACESWO function to PB3 in ***Pin definitions***. | Dec.6, 2022 |

| | | |
|---|---|---|
| | 3. Modify PA11 and PA12 to non-5V tolerant pin.<br>4. Add comments to ***Table 4-1. Absolute maximum ratings***.<br>5. Add comments to ***Power consumption***.<br>6. Modify ***I2C characteristics*** diagram ***Figure 4-6. I2C bus timing diagram***. | |
| 1.7 | 1. Updated $V_{DD}$ , $V_{SSA}$ , $V_{DDA}$ , $V_{BAK}$ range from “1.62 to 3.6 V” to “1.71 to 3.63 V” in chapter 3.3<br>2. Fixed SPI max frequency from 30 MHz to 22.5MHz in chapter 3.13 | Feb.28, 2023 |
| 1.8 | 1. Update the diagrams in chapter 2 and chapter 5.<br>2. Added the ability to drive the I/O current of the backup domain.<br>3. Added the OSCIN and OSCOUT remap information. | Jan.05, 2024 |
| 1.9 | 1. Coplanarity information added for each packages in chapter 5.<br>2. Maximum current for multiple IO information added in chapter 4.1.<br>3. Fixed a input voltage description issue in chapter 4.12. | Jul.10, 2024 |
| 2.0 | 1. Chapter 1.14, added a note for VREFP and VDDA signal at power up.<br>2. Chapter 2.6, updated DAC_OUT0 / DAC_OUT1 to DAC0_OUT0 / DAC0_OUT1 in Pin definitions table.<br>3. Chapter 3.14, Respectively added descriptions of the maximum speed for different USART channels. | Dec.27, 2024 |
| 2.1 | 1. Update DAC to DAC0 in ***Figure2-1 block diagram.***<br>2. Changed TIMER characteristics $t_{COUNTER}$’s unit to ‘μs’ in ***Table 4-62 TIMER characteristics***.<br>3. Added $V_{CORE}$ item into ***Table 4 2. DC operating conditions***., the typical value is 1.1V.<br>4. Modified the parameter descriptions of $V_{ESD}$ and $V_{FTB}$ in ***Table 4 8 EMS characteristics***<br>5. Added $V_{DD}$ / $V_{DDA}$ / $V_{REFP}$ / $V_{REFN}$ parameters into ***Table 4-27 Temperature sensor characteristics.*** | Jan.31, 2026 |
| 2.2 | 1. Correct the values of $PE_{CYC}$ and $t_{RET}$ in the ***Table 4-25 Flash memory characteristics***. | Aug.02, 2026 |

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