GigaDevice Semiconductor Inc.

GD30LD3301x
3A High-accuracy, Low Noise LDO

Datasheet

Table of Contents

List of Figures

List of Tables

1 Features

- Input Voltage Range
  - With BIAS: 1.1 V to 6.5 V
  - Without BIAS: 1.4 V to 6.5 V
- Output Voltage Range
  - 0.8 V to 5.2 V, Set by a Resistor Divider
  - 0.8 V to 3.95 V, Pin-Setting, No External Resistor
- Accurate Output Voltage Accuracy: 1%, Over Line, Load and Temperature
- Ultra Low Dropout Voltage: Maximum 180 mV at 3 A with BIAS
- Ultra High PSRR: 39 dB at 500 KHz
- Excellent Noise Immunity
  - 5.9 uVRMS at 0.8 V Output
  - 9.8 uVRMS at 5 V Output
- Enable Function
- Programmable Soft-Start
- Power-Good Indicator Function

2 Applications

- Wireless Infrastructure: 5G AAU, 4G RRU….
- Telecom/Networking Cards
- Industrial Application

3 General description

The GD30LD3301x is a high-current, low-noise, high accuracy, low-dropout linear regulator (LDO) capable of sourcing 3A with extreme low dropout (max, 180 mV).

The device output voltage is pin-setting from 0.8V to 3.95V and adjustable from 0.8V to 5.2V using the external resistor divider. The device supports input supply voltage as low to 1.1V with BIAS and as low to 1.4V without BIAS.

The low noise, high PSRR and high output current capability makes the GD30LD3301xx ideal to power noise-sensitive devices such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. With very high accuracy, remote sensing, and soft-start capabilities to reduce inrush current, the GD30LD3301x is ideal for powering digital loads such as FPGAs, DSPs, and ASICs.

The external enable control and power good indicator function makes the control sequence easier. The output noise immunity is enhanced by adding external bypass capacitor on

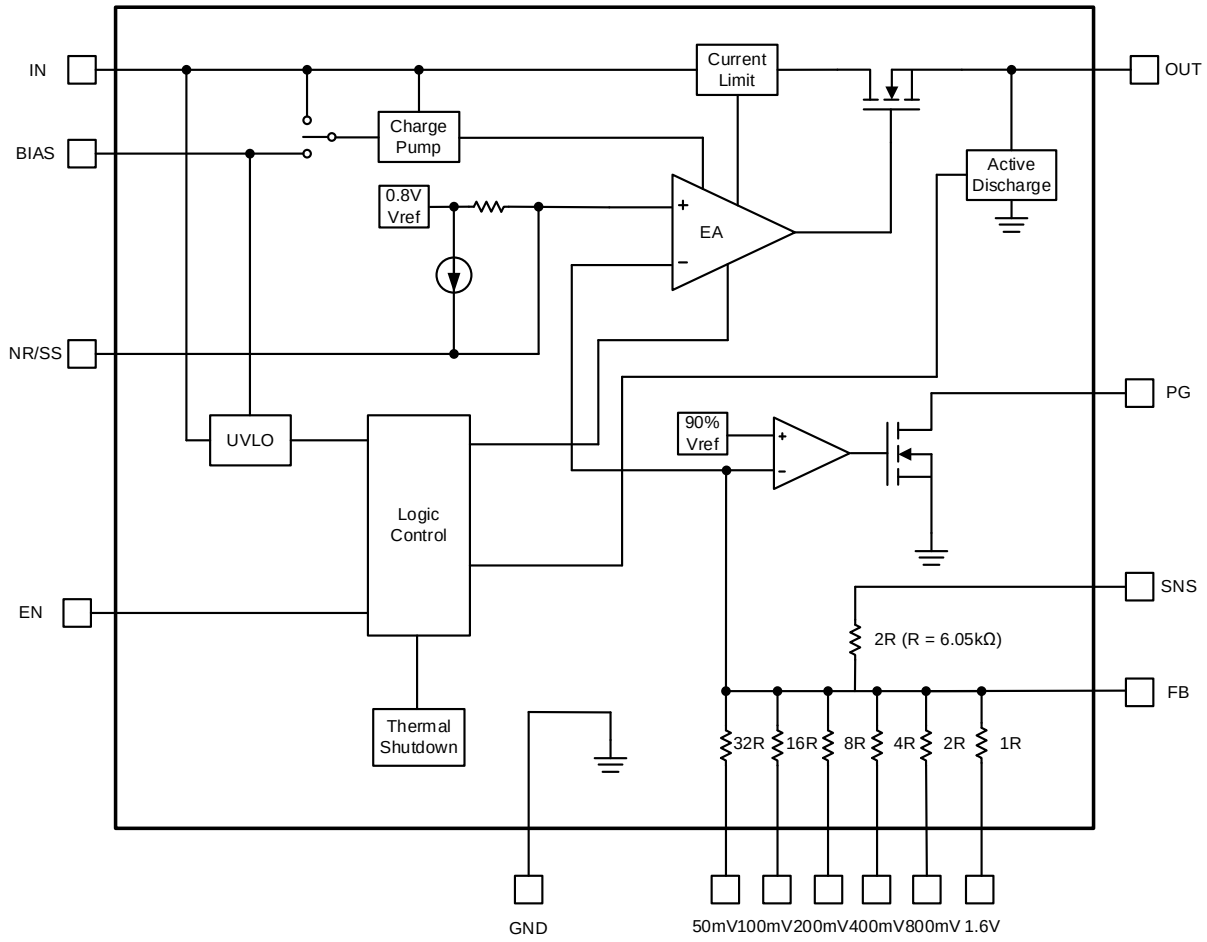
NR/SS pin. The device is fully specified over the temperature range of T_J = −40°C to 125°C and is offered in a QFN20 3.5x3.5mm package.

.

4 Device overview

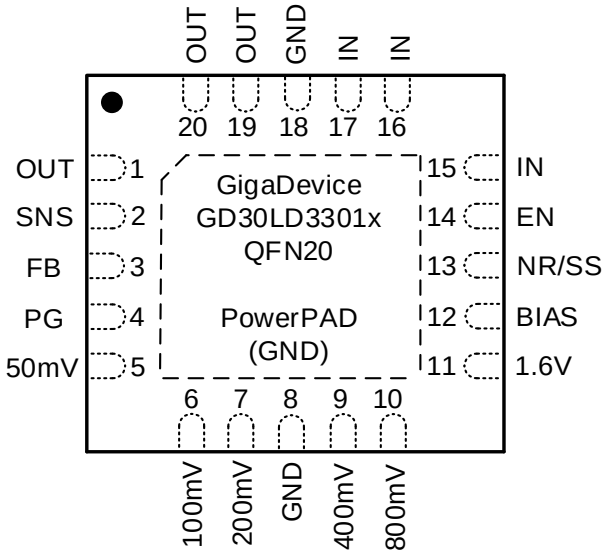
4.1 Block diagram

Figure 4-1 Block diagram for GD30LD3301x



4.2 Pinout and pin assignment

Figure 4-2 GD30LD3301x QFN20 pinouts



4.3 Pin definitions

Table 4-1. GD30LD3301x QFN20 pin definitions

Pin Name	Pins	Pin Type	Functions description
OUT	1, 19, 20	O	LDO output pins. The larger ceramic capacitor (47uF or 2 x 22uF or greater) is stable. Place the output capacitor as close to the device as possible. Minimize the impedance between V_{OUT} pin to load.
SNS	2	I	Output voltage sense input pin. Connect this pin only if using the configuration without external resistors. Keep SNS pin floating if the V_{OUT} voltage is set by external resistor.
FB	3	I	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.8V typically.
PG	4	O	Power good indicator output. An open-drain output and active high when the output voltage reaches 89% of the target. The pin is pulled to ground when the output voltage is lower than its specified threshold, EN shutdown, OCP and OTP.

Pin Name	Pins	Pin Type	Functions description
50mV,100mV 200mV,400mV 800mV,1.6V	5,6,7,9,10,11	O	Output voltage setting pins. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) if the V_{OUT} voltage is set by external resistor.
GND	8,18,21 Thermal pad	G	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
BIAS	12	I	BIAS supply voltage. This pin enables the use of low-input voltage, low-output (LILO) voltage conditions (that is, V_{IN} = 1.2V, V_{OUT} = 1V) to reduce power dissipation across the die. The use of a BIAS voltage improves dc and ac performance for V_{IN} ≤ 2.2 V. A 1μF capacitor or larger must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground.
NR/SS	13	I	Noise-reduction and soft-start pin. Decouple this pin to GND with an external capacitor $C_{NR/SS}$ can not only reduce output noise to very low levels but also slow down the rising of V_{OUT}, providing a soft-start behavior. For low noise applications, a 10nF to 100nF $C_{NR/SS}$ is suggested.
EN	14	I	Enable control input. Connecting this pin to logic high enables the regulator, and driving this pin low puts it into shutdown mode. The device can have V_{IN} and V_{EN} sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} is preferred.
IN	15,16,17	I	Supply input. A general 10uF or larger ceramic capacitor should be placed as close as possible to this pin for better noise rejection.

Notes:

1. Type: I = input, O = output, I/O = input or output, P = power, G = Ground.

5 Functional description

5.1 Output Voltage Setting

The output voltage of the GD30LD3301x can be set by external resistors or by using the output voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV and 1.6V) to achieve different output targets.

By using external resistors, the output voltage is determined by the values of R1 and R2 as shown in Table 7-1. The values of R1 and R2 can be calculated for any voltage value using the following formula:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

The GD30LD3301x can also short pins 5, 6, 7, 9, 10, and 11 to ground and program the regulated output voltage level without external resistors after the SNS pin is connected to the V_{OUT}. Pins 5, 6, 7, 9, 10, and 11 are connected with internal resistor pairs. Each pin is either connected to ground (active) or left open (floating). Voltage programming is set as the sum of the internal reference voltage (V_{FB} = 0.8V) plus the accumulated sum of the respective voltages assigned to each active pin as illustrated in Table 7-2.

$$V_{OUT} = V_{FB} + V_{PIN-SET}$$

5.2 Recommended device selection

5.2.1 C_{IN} and C_{OUT} Selection

The GD30LD3301x is designed to support low-series resistance (ESR) ceramic capacitors. It is recommended to use ceramic capacitors with X7R, X5R, and C0G-rated ceramic capacitors to get good capacitive stability across different temperatures.

However, the capacitance of ceramic capacitors varies with operating voltage and temperature, and the design engineer must be aware of these characteristics. Ceramic capacitors are usually recommended to be derated by 50%. A 47μF or greater output ceramic capacitor is suggested to ensure stability. Input capacitance is selected to minimize transient input drop during load current steps. For general applications, an input capacitor of at least 10μF is highly recommended for minimal input impedance. If the trace inductance between the GD30LD3301x input pin and power supply is high, a fast load transient can cause V_{IN} voltage level ringing above the absolute maximum voltage rating which damages the device. Adding more input capacitors is available to restrict the ringing and keep it below the device absolute maximum ratings.

Generally, a 47μF 0805-sized ceramic capacitor in parallel with two 10μF 0805-sized ceramic capacitor ensures the minimum effective capacitance at high input voltage and high

output voltage requirement. Place these capacitors as close to the pins as possible for optimum performance and to ensure stability.

5.2.2 Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled.

5.3 Low-Noise, High-RSRR Output

The GD30LD3301x includes a low-noise reference and error amplifier ensuring minimal noise during operation. The NR/SS capacitor ($C_{NR/SS}$) and feed-forward capacitor (C_{FF}) are the easiest way to reduce device noise. $C_{NR/SS}$ filters the noise from the reference and CFF filters the noise from the error amplifier. The noise contribution from the charge pump is minimal. The overall noise of the system at low output voltages can be reduced by using a bias rail because this rail provides more headroom for internal circuitry.

The high power-supply rejection ratio (PSRR) of the GD30LD3301x ensures minimal coupling of input supply noise to the output. The PSRR performance is primarily results from a high-bandwidth, high-gain error amplifier and an innovative circuit to boost the PSRR between 200kHz and 1MHz.

5.4 Power-Good Function

The PG circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. The PG circuit asserts whenever FB, V_{IN}, or EN are below their thresholds. The PG operation versus the output voltage is shown in Figure 5-1, ch is described by Table 5-1.

Figure 5-1 Typical PG Operation

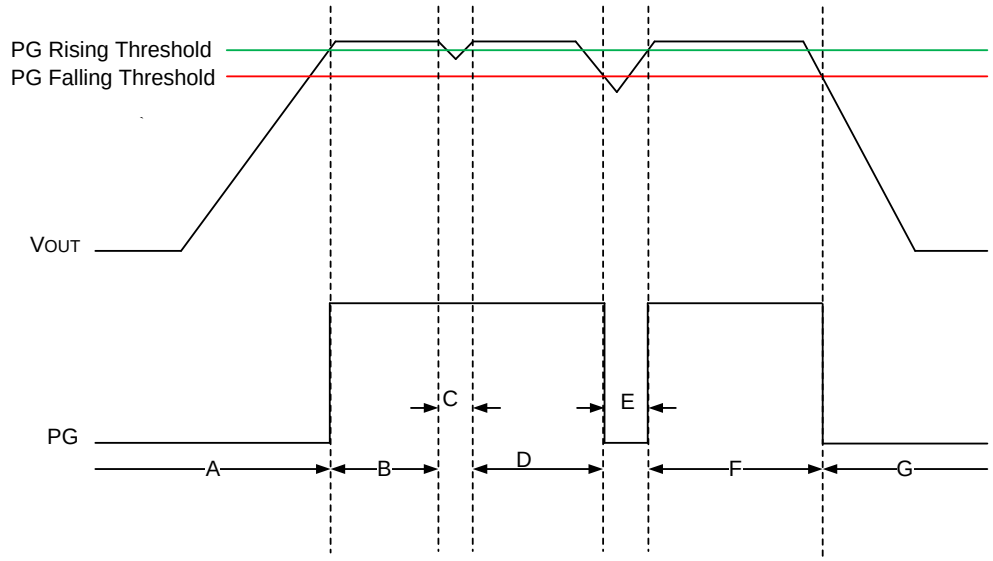


Table 5-1 Typical PG Operation Description

Region	EVENT	PG STATUS	FB VOLTAGE
A	Turn on	0	$V_{FB} < V_{IT(PG)} + V_{HYS(PG)}$
B	Regulation	Hi-Z	$V_{FB} \geq V_{IT(PG)}$
C	Output voltage dip	Hi-Z	
D	Regulation	Hi-Z	
E	Output voltage dip	0	$V_{FB} < V_{IT(PG)}$
F	Regulation	Hi-Z	$V_{FB} \geq V_{IT(PG)}$
G	Turnoff	0	$V_{FB} < V_{IT(PG)}$

The PG pin is open-drain, and connecting a pullup resistor to an external supply enables others devices to receive Power Good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices.

To ensure proper operation of the PG circuit, the pullup resistor value must be from 10kΩ and 100kΩ. The lower limit of 10kΩ results from the maximum pulldown strength of the PG transistor, and the upper limit of 100kΩ results from the maximum leakage current at the PG node. If the pullup resistor is outside of this range, then the PG signal may not read a valid digital logic level.

5.5 Soft-Start Function

The GD30LD3301x is designed for a programmable, monotonic soft-start time during the output rising, which can be achieved via an external capacitor ($C_{NR/SS}$) on NR/SS pin. Using an external $C_{NR/SS}$ is recommended for general application, it is not only for the in-rush current minimization but also helps reduce the noise component from the internal reference. During the monotonic start-up procedure, the error amplifier of the GD30LD3301x tracks the voltage ramp of the external soft-start capacitor ($C_{NR/SS}$) until the voltage approaches the internal reference 0.8V.

The soft-start ramp time can be calculated with equation, which depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference 0.8V (V_{FB}).

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS}$$

For noise-reduction, $C_{NR/SS}$ in conjunction with an internal noise-reduction resistor forms a low-pass filter (LPF) and filters out the noise from the internal bandgap reference before being amplified via the error amplifier, thus reducing the total device noise floor.

5.6 Undervoltage Lockout (UVLO)

The UVLO circuits ensure that the device stays disabled before its input or bias supplies reach the minimum operational voltage range, and ensures that the device properly shuts down when either the input or bias supply collapses. Figure 5-2 and Table 5-2 explain one of the UVLO circuits being triggered to various input voltage events, assuming $V_{EN} \geqslant V_{IH(EN)}$.

Figure 5-2 Typical UVLO Operation

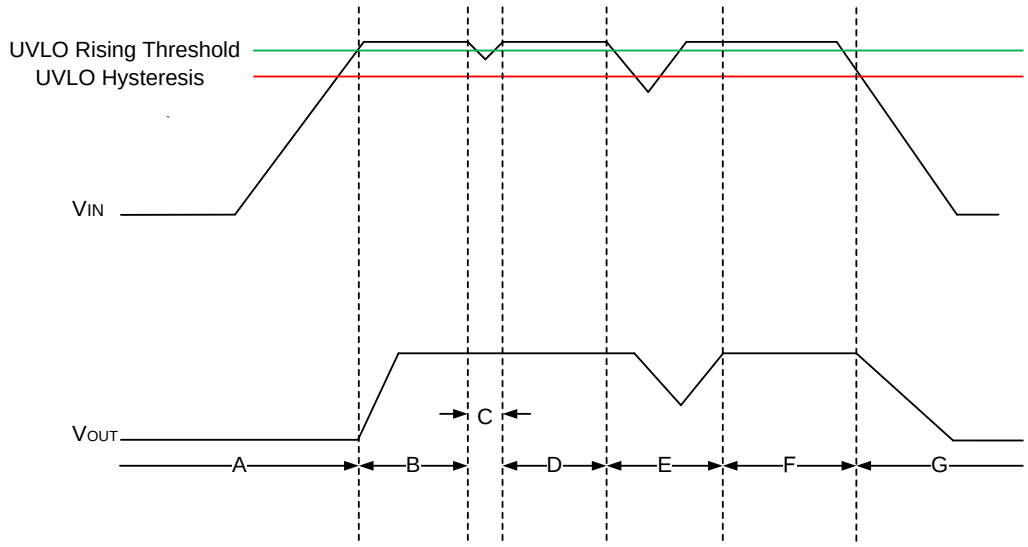


Table 5-2 Typical UVLO Operation Description

Region	EVENT	VOUT STATUS	COMMENT
A	Turn on, $V_{IN} \geq V_{UVLO\_1,2(IN)}$ and $V_{BIAS} \geq V_{UVLO(BIAS)}$	Off	Startup
B	Regulation	On	Regulates to target V_{OUT}
C	Brown out, $V_{IN} \geq V_{UVLO\_1,2(IN)} - V_{HYS\_1,2(IN)}$ or $V_{UVLO(BIAS)} – V_{HYS(BIAS)}$	On	The output can fall out of regulation but the device is still enabled
D	Regulation	On	Regulates to target V_{OUT}
E	Brownout $V_{IN} < V_{UVLO\_1,2(IN)} - V_{HYS\_1,2(IN)}$ or $V_{BIAS} \geq V_{UVLO(BIAS)} – V_{HYS(BIAS)}$	Off	The device is disabled and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO fault is removed when either the IN or BIAS UVLO rising threshold is reached by the input or bias voltage and a normal start-up then follows.
F	Regulation	On	Regulates to target V_{OUT}
G	Turnoff, $V_{IN} < V_{UVLO\_1,2(IN)} – V_{HYS\_1,2(IN)}$ or $V_{BIAS} < V_{UVLO(BIAS)} – V_{HYS(BIAS)}$	Off	The output falls because of the load and active discharge circuit.

Similar to many other LDOs with this feature, the UVLO circuits take a few microseconds to fully assert. During this time, a downward line transient below approximately 0.8V causes the UVLO to assert for a short time; however, the UVLO circuits do not have enough stored energy to fully discharge the internal circuits inside of the device. When the UVLO circuits are not given enough time to fully discharge the internal nodes, the outputs are not fully disabled.

The effect of the downward line transient can be mitigated by using a larger input capacitor to increase the fall time of the input supply when operating near the minimum V_{IN}.

5.7 Power Dissipation (P_D)

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

$V_{IN} \times I_{GND}$ represents the static power consumption of the LDO, the value is relatively small and can be ignored. An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB, device package, and the temperature of the ambient air (T_A).

$$T_J = T_A + \theta_{JA} \times P_D$$

$$I_{OUT} = \left(T_J - T_A\right) / \left[\theta_{JA} \times \left(V_{IN} - V_{OUT}\right)\right]$$

6 Electrical characteristics

6.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 6-1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Voltage	IN, BIAS, PG, EN, OUT	-0.3	7.0	V
	NR/SS, FB	-0.3	3.6	V
Current	OUT	Internally limited	Internally limited	A
	PG(sink current into device)	—	5	mA
Thermal characteristics				
T_J	Operating junction temperature	-55	150	°C
T_{stg}	Storage temperature	-65	150	°C

6.2 Recommended Operating Conditions

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage range	1.1	—	6.5	V
V_{BIAS}	Bias supply voltage range	3.0	—	6.5	V
V_{OUT}	Output voltage range	0.8	—	5.2	V
V_{EN}	Enable Voltage range	0	—	V_{IN}	V
I_{OUT}	Output current	0	—	3	A
C_{IN}	Input capacitor	10	47	—	uF
C_{OUT}	Output capacitor	47	47 // 10 // 10	—	uF
R_{PG}	Power-good pullup resistance	10	—	100	kΩ

Symbol	Parameter	Min	Typ	Max	Unit
$C_{NR/SS}$	NR/SS capacitor	—	10	—	nF
C_{FF}	Feed-forward capacitor	—	10	—	nF
R_1	Adjustable resistance in FB network	—	12.1	—	kΩ
R_2	Adjustable resistance in FB network	—	—	160	kΩ
T_J	Operating junction temperature	-40	—	125	℃

6.3 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample.

Table 6-3 Electrostatic Discharge characteristics

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; JS-001-2017	±2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; JS-002-2018	±500	V

6.4 Electrical Specifications

Over operating temperature range (T_J = −40°C to 125°C), Typical values are at T_J = 25°C. V_{IN} = 1.4 V or V_{IN} = $V_{OUT\ (TARGET)}$ + 0.4 V, V_{BIAS}=OPEN, $V_{OUT\ (TARGET)}$ = 0.8 V, V_{OUT} connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{IN} = 10 μF, C_{OUT} = 47 μF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to OUT with 100 kΩ, unless otherwise noted.

Table 6-4 Electrical characteristics

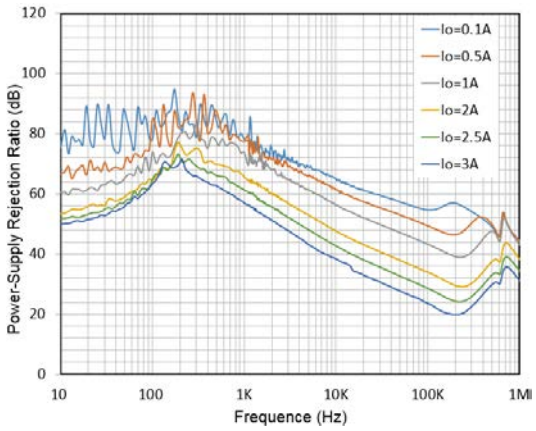
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Range	—	1.1	—	6.5	V
V_{BIAS}	BIAS Range	V_{IN} = 1.1 V	3.0	—	6.5	V
V_{FB}	Feedback Voltage	—	—	0.8	—	V
$V_{NR/SS}$	NR/SS pin Voltage	—	—	0.8	—	V
$V_{UVLO1(IN)}$	UVLO1 with BIAS	V_{IN} rising with V_{BIAS} = 3.0 V	—	0.93	1.085	V
$V_{HYS1(IN)}$	UVLO1 hysteresis With	V_{BIAS} = 3.0 V	—	240	—	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	BIAS					
$V_{UVLO2(IN)}$	UVLO2 without BIAS	V_{IN} rising	—	1.33	1.39	V
$V_{HYS2(IN)}$	UVLO2 hysteresis without BIAS	—	—	230	—	mV
$V_{UVLO(BIAS)}$	UVLO(BIAS)	V_{BIAS} rising, V_{IN} = 1.1 V	—	2.72	2.9	V
$V_{HYS(BIAS)}$	UVLO(BIAS) hysteresis With BIAS	V_{IN} = 1.1 V	—	250	—	mV
V_{OUT}	Output Voltage Range	Using Voltage setting pins (50 mV, 100 mV, 200 mV, 400 mV, 800 mV and 1.6 V)	0.8 -1%	—	3.95 +1%	V
		Using external resistors	0.8 -1%	—	5.2 +1%	V
	Output Accuracy	V_{IN} = V_{OUT} + 0.3 V, 0.8 V ≤ V_{OUT}≤ 5.2 V	-1	—	1	%
$\triangle V_{OUT}/\triangle V_{IN}$	Line Regulation	I_{OUT} = 5 mA, 1.4 V ≤ V_{IN}≤ 6.5 V	—	0.1	—	mV/V
$\triangle V_{OUT}/\triangle I_{OUT}$	Load Regulation	5 mA ≤ I_{OUT}≤ 3 A	—	0.3	—	mV/A
V_{DROP}	Dropout Voltage	V_{IN} = 1.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%	—	135	250	mV
		V_{IN} = 5.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%	—	155	250	mV
		V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%	—	110	180	mV
I_{LIM}	Output Current Limit	V_{OUT} = 90% * $V_{OUT(TARGET)}$ V_{IN} = $V_{OUT(TARGET)}$ + 400 mV	3.6	4.2	4.8	A
I_{SC}	Short-Circuit Current Limit	R_{LOAD} = 20 mΩ	—	1	—	A
I_{GND}	Ground Pin Current	Vin = 6.5 V, I_{OUT} = 5 mA	—	3.0	4.2	mA
		Vin = 1.4 V, I_{OUT} = 3 A	—	4.2	5.5	mA
		Shutdown, PG = OPEN, V_{IN} = 6.5 V, V_{EN} = 0.5 V	—		25	uA
I_{BIAS}	BIAS Pin Current	V_{IN} = 1.1 V, V_{BIAS}= 6.5 V, V_{OUT} = 0.8 V, I_{OUT} = 3 A	—	3.0	4.2	mA
I_{EN}	EN Pin Current	V_{IN} = 6.5 V, V_{EN} = 0 V and 6.5 V	-0.1	—	0.1	uA
V_{EN_H}	EN Pin High-Level	—	1.1	—	6.5	V
V_{EN_L}	EN Pin	—	0	—	0.5	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
	Low-Level						
$V_{IT(PG)}$	PG Pin Threshold	For falling V_{OUT}		83% *V_{OUT}	88% *V_{OUT}	93% *V_{OUT}	V
V_{HYS_PG}	PG Pin Hysteresis	For rising V_{OUT}		—	3% *V_{OUT}	—	V
V_{PG_L}	PG Pin Low-Level output Voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = -1 mA		—	—	0.1	V
I_{PG_LK}	PG Pin Low-leakage Current	V_{OUT} > $V_{IT(PG)}$, V_{PG} = 6.5 V		—	—	1	uA
$I_{NR/SS}$	NR/SS Pin Charging Current	V_{IN} = GND,V_{IN} = 6.5 V		4	7.2	9	uA
I_{FB}	FB Pin leakage Current	V_{IN} = 6.5 V		-100	—	100	nA
PSRR	Power Supply Ripple Rejection	V_{IN}-V_{OUT} = 0.4 V I_{OUT} = 3 A $C_{NR/SS}$ = 100 nF C_{FF} = 10 nF C_{OUT}= 47uF//10uF//10uF	f =10 KHz, V_{OUT}=0.8 V V_{BIAS} = 5 V	—	42	—	dB
			f = 500KHz, V_{OUT} = 0.8 V V_{BIAS} = 5V	—	39	—	dB
			f =10 KHz, V_{OUT} = 5 V	—	40	—	dB
			f = 500 KHz, V_{OUT} = 5 V	—	25	—	dB
V_N	Output Noise Voltage	BW = 10 Hz to 100 KHz, Vin = 1.1 V V_{OUT} = 0.8 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF C_{OUT} = 47 uF//10 uF//10 uF		—	5.9	—	uV_{RMS}
		BW = 10 Hz to 100 KHz, V_{OUT}= 5.0 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF C_{OUT} = 47 uF//10 uF//10 uF		—	9.8	—	uV_{RMS}
T_{SD}	Thermal Shutdown Threshold	Shut down, temperature increasing		—	160	—	°C
		Reset, temperature increasing		—	140	—	°C

6.5 Typical Characteristics

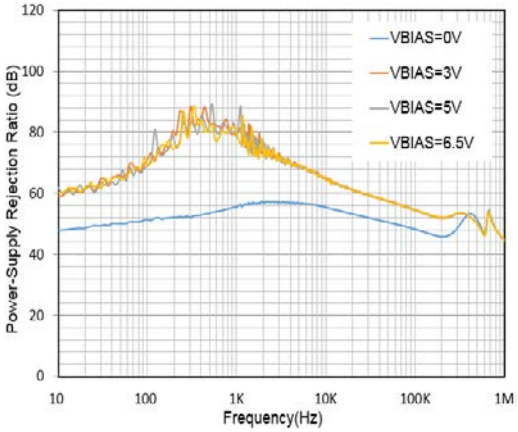
T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = OPEN, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 uF // 10 µF// 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



V_{IN} = 1.1 V, V_{BIAS} = 5 V, C_{FF} = 10 nF

C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF

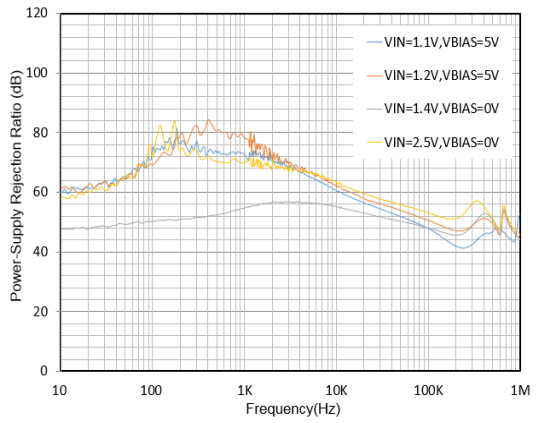
PSRR vs Frequency and I_{OUT}



V_{IN} = 1.4 V, I_{OUT} = 1A, C_{FF} = 10 nF

C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF

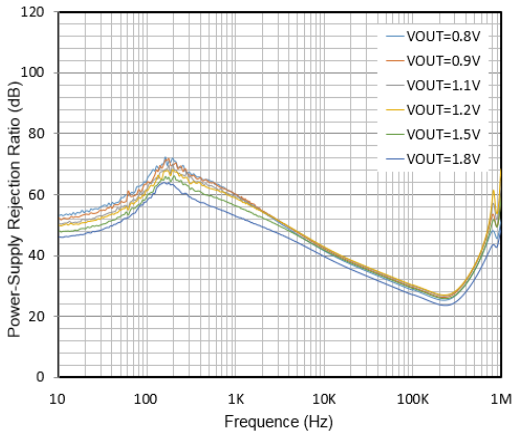
PSRR vs Frequency and V_{BIAS}



I_{OUT} = 1 A, C_{FF} = 10 nF

C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF

PSRR vs Frequency and V_{IN}

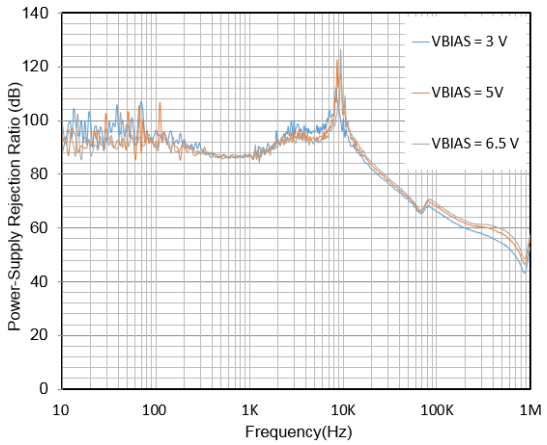


V_{IN} = V_{OUT} + 0.3 V

I_{OUT} = 3 A, C_{FF} = 10 nF, V_{BIAS} = 5 V,

C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF

PSRR vs Frequency and V_{OUT} with BIAS

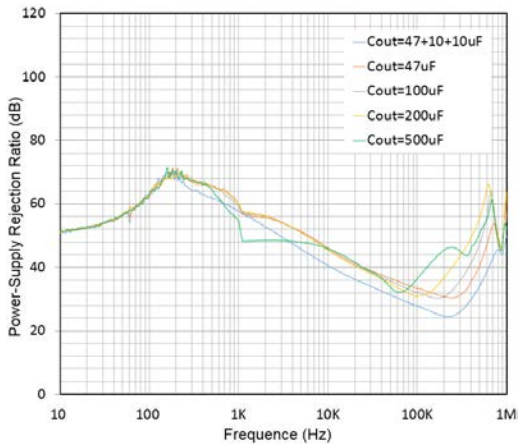


V_{IN} = V_{OUT} + 0.3 V, I_{OUT} = 3 A, V_{OUT} = 1 V,

C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF

C_{FF} = 10 nF

V_{BIAS} PSRR vs Frequency



V_{IN} =1.4 V, V_{BIAS} = 5 V, V_{OUT} = 1 V, I_{OUT} = 3 A

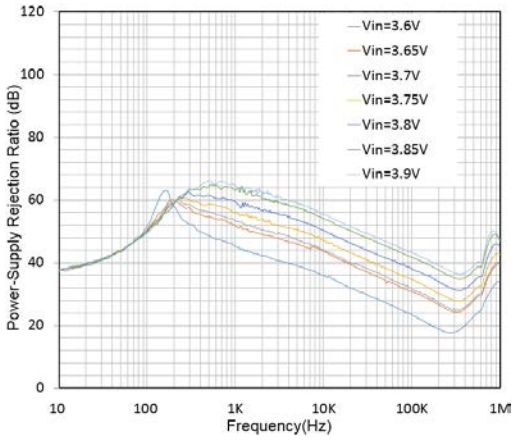
C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF

C_{FF} = 10 nF

PSRR vs Frequency and C_{OUT}

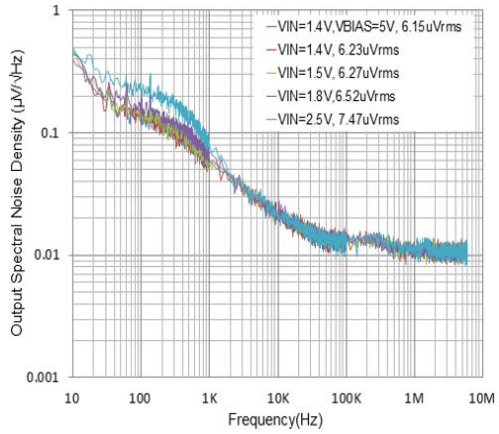
Typical Characteristics

T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = OPEN, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 uF // 10 µF// 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



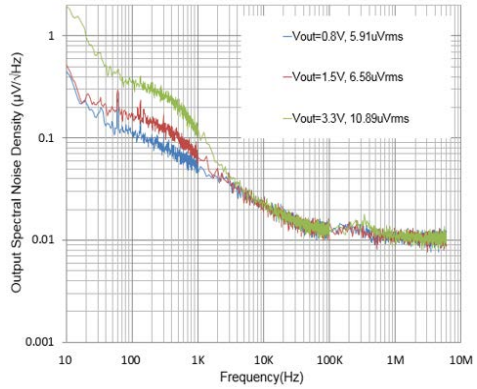
C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, I_{OUT} = 3 A

PSRR vs Frequency and V_{IN} (V_{OUT} = 3.3 V)



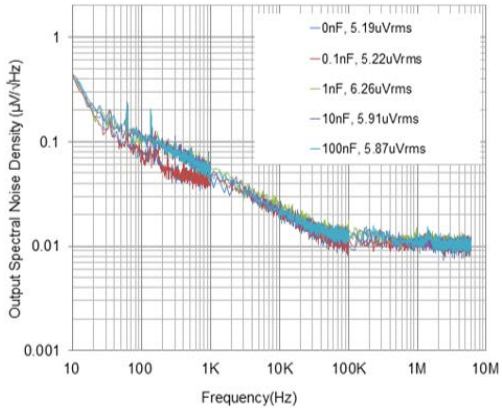
C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, I_{OUT} = 3 A

Output Noise vs Frequency and Input Voltage



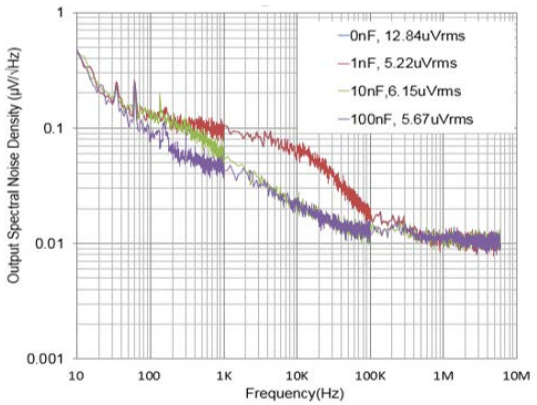
V_{IN} = V_{OUT} + 0.3 V and V_{BIAS} = 5 V for V_{OUT} ≤ 2.2 V, I_{OUT} = 3 A, C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Output Noise vs Frequency and Output Voltage



V_{IN} = 1.1 V, V_{BIAS} = 5 V, V_{OUT} = 0.8 V, I_{OUT} = 3 A, C_{OUT} = 47 µF // 10 µF // 10 µF, $C_{NR/SS}$ = 10 nF

Output Noise vs Frequency and C_{FF}



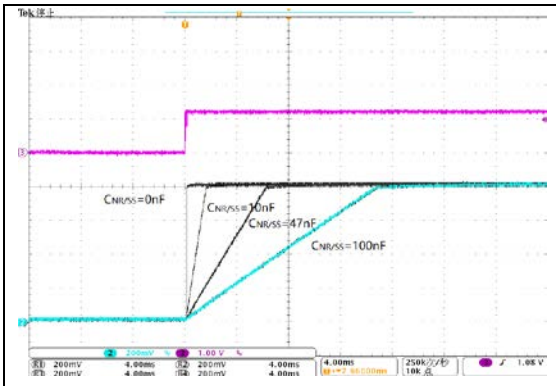
V_{IN} = 1.1 V, V_{BIAS} = 5 V, V_{OUT} = 0.8 V, I_{OUT} = 3 A,

C_{OUT} = 47 µF // 10 µF // 10 µF, C_{FF} = 10 nF

Output Noise vs Frequency and $C_{NR/SS}$

Typical Characteristics

T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = OPEN, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 uF // 10 µF// 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).

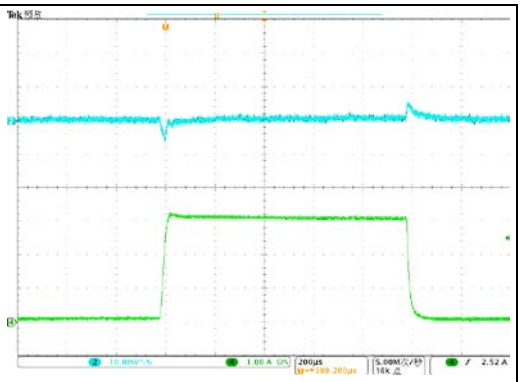


CH3 = EN, CH2 = V_{OUT}

V_{IN} = 1.4 V, V_{OUT} = 0.8 V, I_{OUT} = 3 A,

C_{OUT} = 47 µF // 10 µF // 10 µF, C_{FF} = 10 nF

Startup waveform vs $C_{NR/SS}$

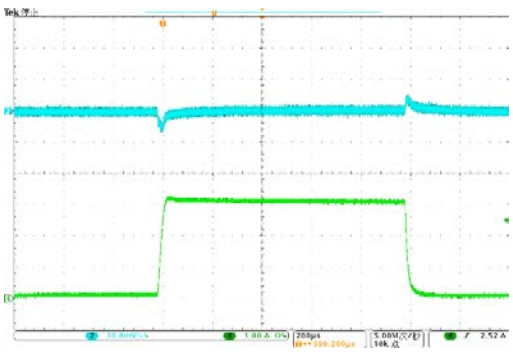


CH2 = V_{OUT}, CH4 = I_{OUT}

V_{IN} = 1.1 V, V_{BIAS} = 5 V

V_{OUT} = 0.8 V, I_{OUT} = 100 mA-3A, slew rate = 1 A/µs

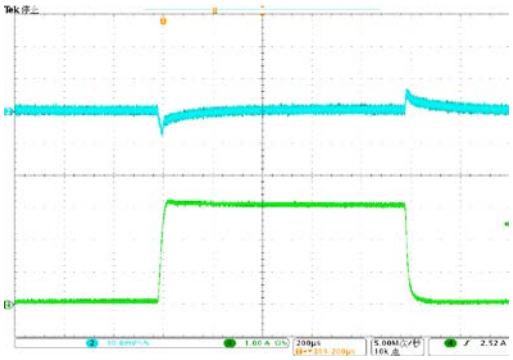
Load Transient With BIAS



CH2 = V_{OUT}, CH4 = I_{OUT}, V_{IN} = 1.4 V, V_{BIAS} = OPEN

V_{OUT} = 0.8V, I_{OUT} = 100 mA-3A, slew rate = 1 A/µs,

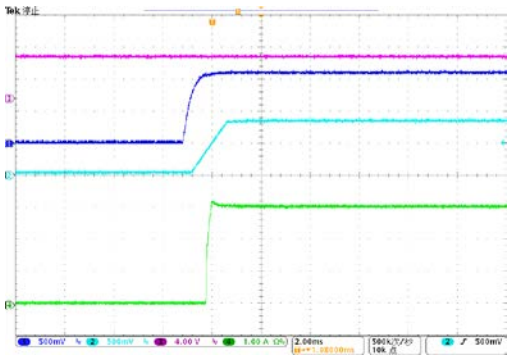
Load Transient Without BIAS, V_{OUT} = 0.8V



CH2 = V_{OUT}, CH4 = I_{OUT}, V_{IN} = 3.6 V, V_{BIAS} = OPEN,

V_{OUT} = 3.3V, I_{OUT} = 100 mA - 3A, slew rate = 1 A/µs

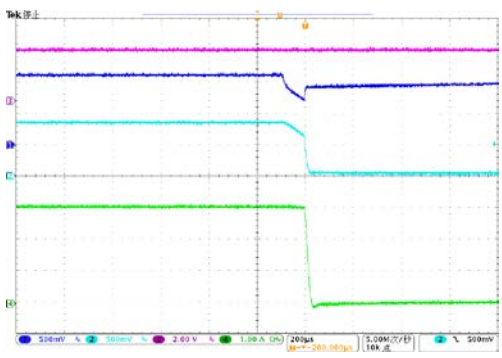
Load Transient Without BIAS, V_{OUT} = 0.8V



CH1 = V_{IN}, CH2 = V_{OUT}, CH3 = V_{BIAS}, CH4 = I_{OUT}

V_{IN} = V_{EN} =1.1 V, V_{BIAS} = 3 V, V_{OUT} = 0.8 V, I_{OUT} = 3 A

Power On by V_{IN} = V_{EN} = 1.1 V



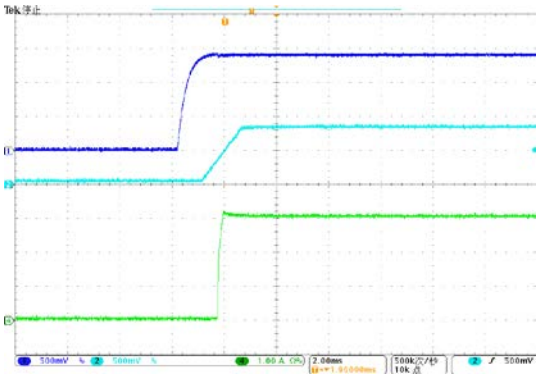
CH1 = V_{IN}, CH2 = V_{OUT}, CH3 = V_{BIAS}, CH4 = I_{OUT}

V_{IN} = V_{EN} =1.1 V, V_{BIAS} = 3 V, V_{OUT} = 0.8 V, I_{OUT} = 3 A

Power off by V_{IN} = V_{EN} = 1.1 V

Typical Characteristics

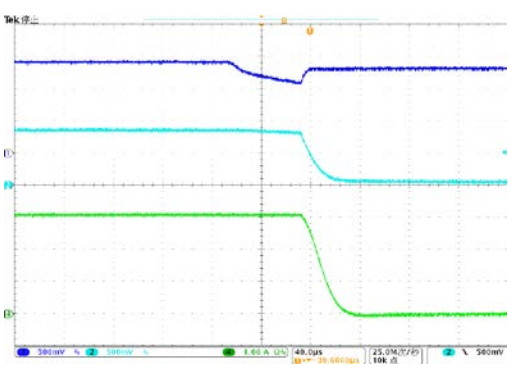
T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = OPEN, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 uF // 10 µF// 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

V_{IN} = V_{EN} =1.4 V, V_{OUT}=0.8 V, I_{OUT} = 3 A

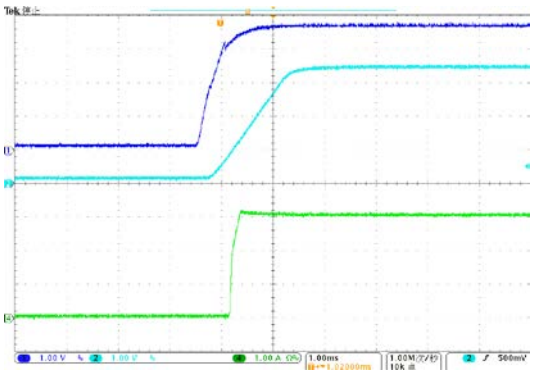
Power On by V_{IN} = V_{EN} = 1.4V



CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

V_{IN} = V_{EN} = 1.4 V, V_{OUT}=0.8 V, I_{OUT} = 3 A

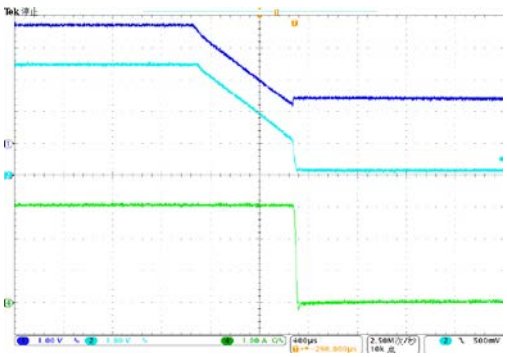
Power off by V_{IN} = V_{EN} = 1.4V



CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

V_{IN} = V_{EN} =3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A

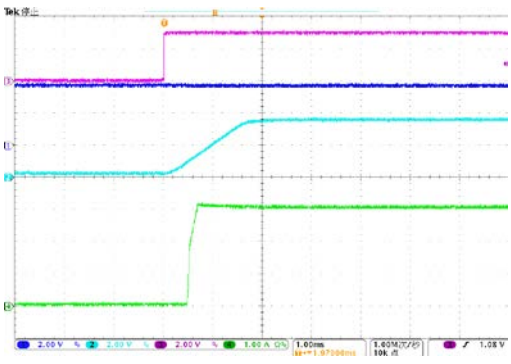
Power On by V_{IN} = V_{EN} = 3.3 V



CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

V_{IN} = V_{EN} =3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A

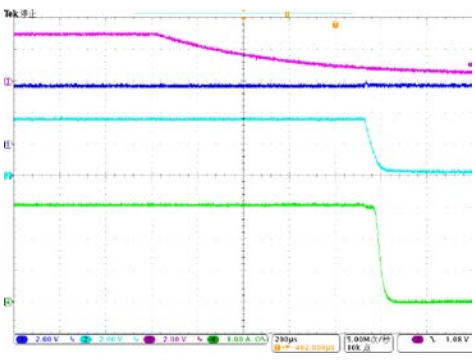
Power off by V_{IN} = V_{EN} = 3.3 V



CH1 = V_{IN}, CH2 = V_{OUT}, CH3 = V_{EN}, CH4 = I_{OUT}

V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A

Power On by V_{EN}



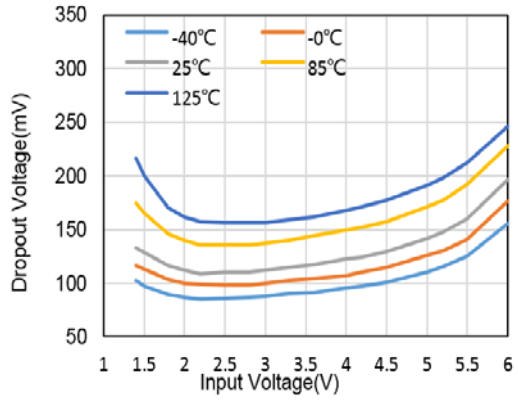
CH1 = V_{IN}, CH2 = V_{OUT}, CH3 = V_{EN}, CH4 = I_{OUT}

V_{IN} = 3.3 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A

Power Off by V_{EN}

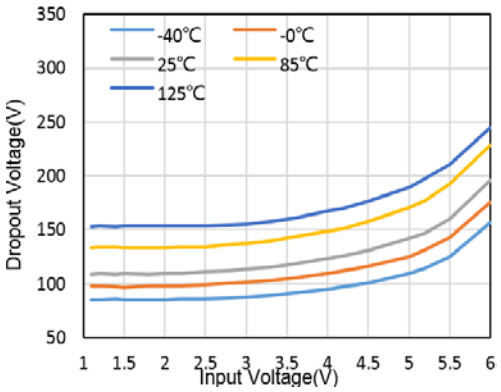
Typical Characteristics

T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = OPEN, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 uF // 10 µF// 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



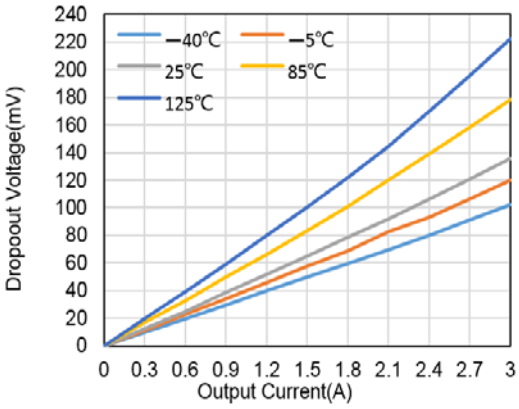
I_{OUT} = 3 A

Dropout Voltage vs Input Voltage without BIAS



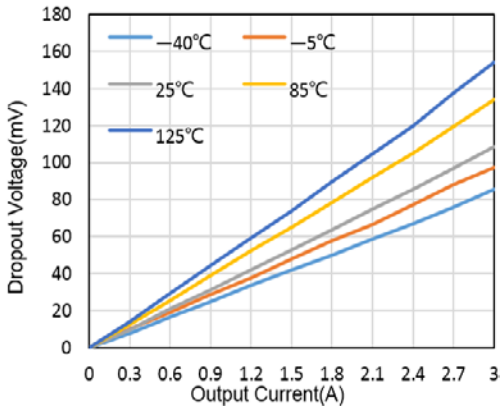
I_{OUT} = 3 A V_{BIAS} = 6.5 V

Dropout Voltage vs Input Voltage with BIAS



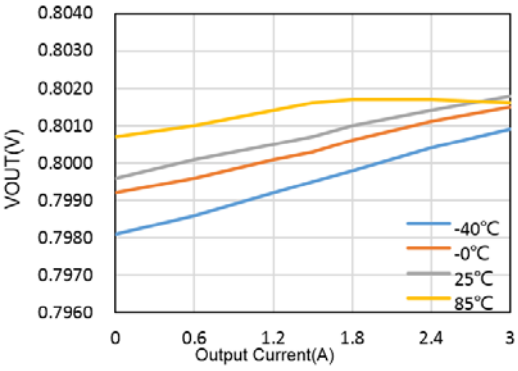
V_{IN} = 1.4 V

Dropout Voltage vs Output Current without BIAS



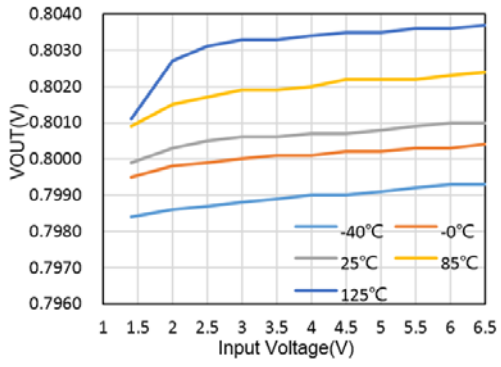
V_{IN} = 1.1 V, BIAS = 3.0 V

Dropout Voltage vs Input Voltage with BIAS



V_{IN} = 1.4 V

Output Voltage vs Output Current

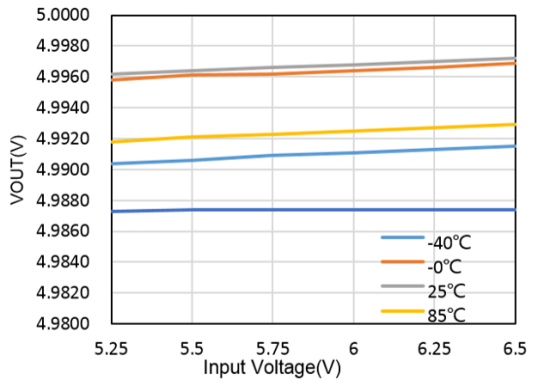


V_{OUT} = 0.8 V, I_{OUT} = 5 mA

Output Voltage vs Input Voltage

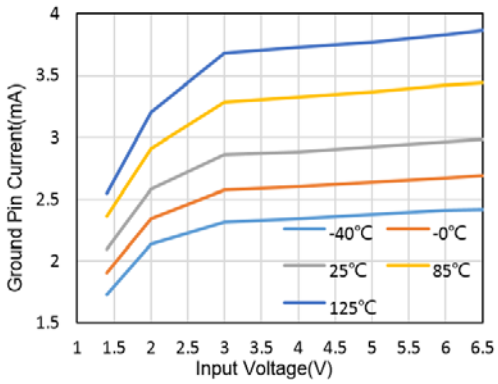
Typical Characteristics

T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = OPEN, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 uF // 10 µF// 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



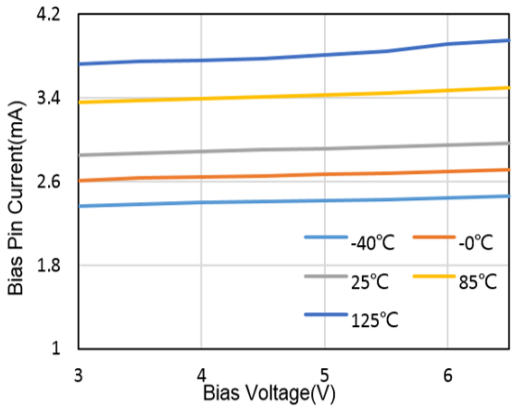
V_{OUT} = 5 V, I_{OUT} = 5 mA

Output Voltage vs Input Voltage



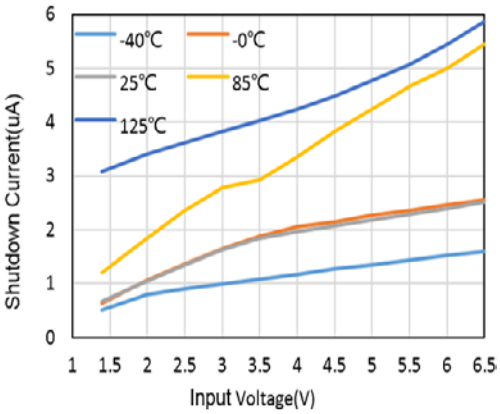
V_{BIAS} = 0 V, I_{OUT} = 5 mA

Ground Pin Current vs Input Voltage



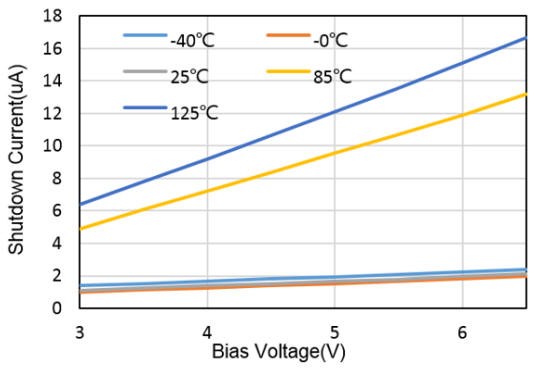
V_{IN} = 1.1 V, I_{OUT} = 5 mA

BIAS Pin Current vs BIAS Voltage



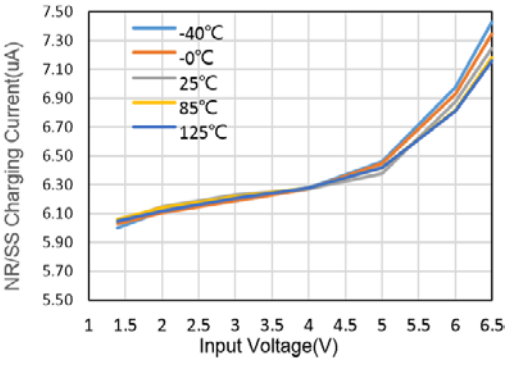
V_{BIAS} = 0 V

Shutdown Current vs Input Voltage



V_{IN} = 1.1 V

Shutdown Current vs BIAS Voltage

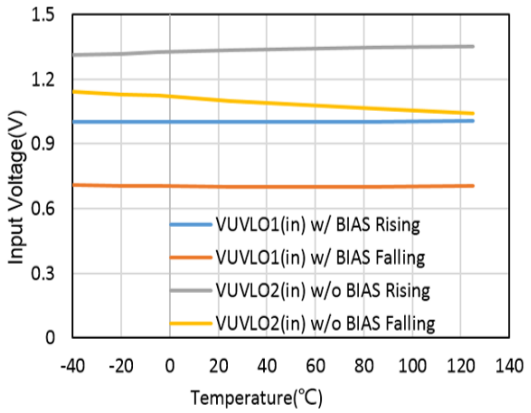


V_{BIAS} = 0 V

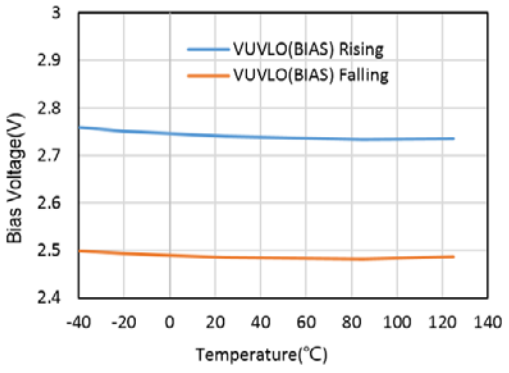
$I_{NR/SS}$ Current vs Input Voltage

Typical Characteristics

T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = OPEN, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 uF // 10 µF// 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).

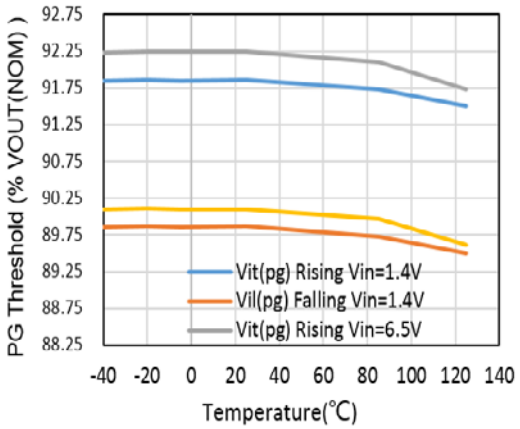


V_{IN} UVLO vs Temperature

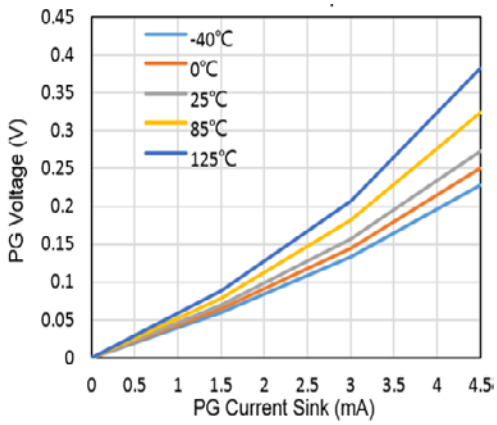


V_{IN} = 1.1 V

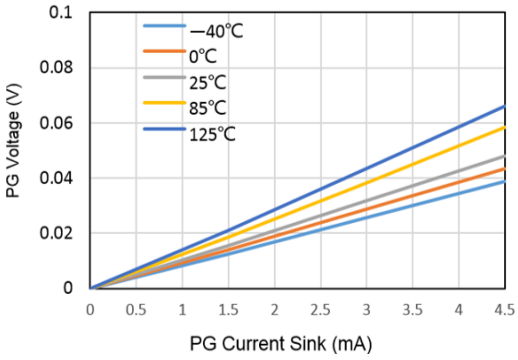
V_{BIAS} UVLO vs Temperature



PG Threshold vs Temperature



PG Voltage vs PG Current Sink



V_{IN} = 6.5 V

PG Voltage vs PG Current Sink

7 Typical application circuit

Figure 7-1 Typical GD30LD3301x application circuit with adjustable resistance

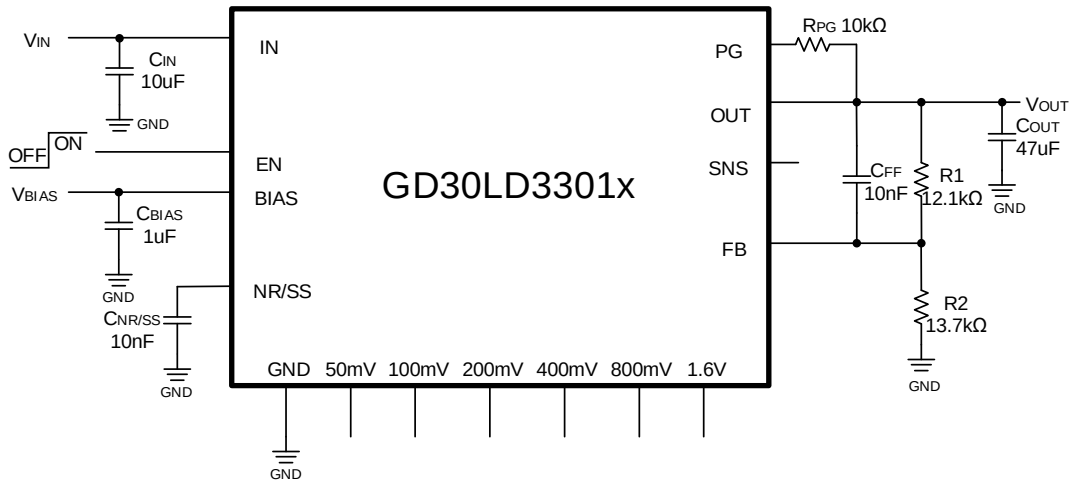
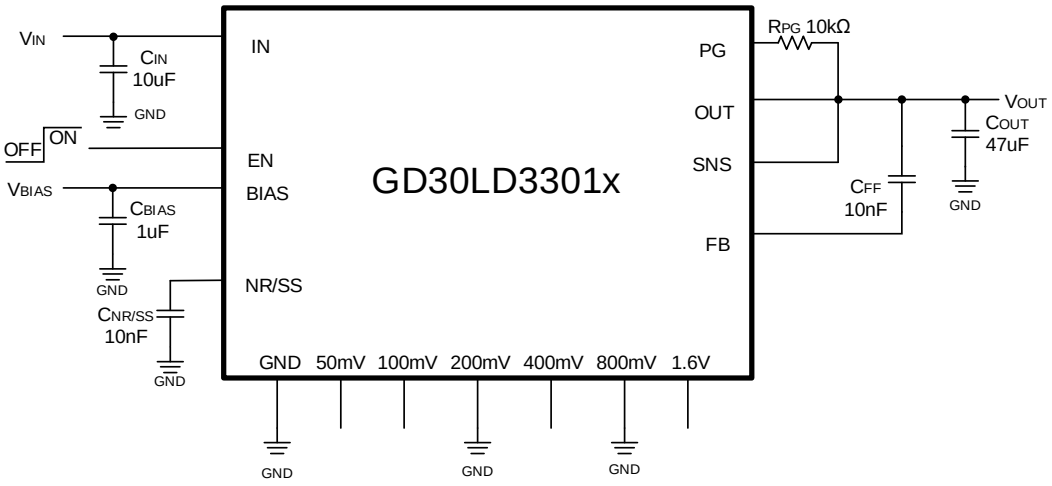


Table 7-1 Adjusted V_{OUT} by external feedback resistor

V_{OUT}(V)	External Feedback Resistor	
	R1 (kΩ)	R2(kΩ)
0.8	0	NC
0.9	12.1	97.6
1.00	12.1	48.7
1.10	12.1	32.4
1.20	12.1	24.3
1.50	12.1	13.7
1.80	12.1	9.76
1.90	12.1	8.87
2.50	12.1	5.76
2.85	12.1	4.75
3.00	12.1	4.42
3.30	12.1	3.83
3.60	12.1	3.48
4.5	12.1	2.61
5.00	12.1	2.32
5.2	12.1	2.2

Figure 7-2 Typical GD30LD3301x application circuit with pin-setting



1.8V Fixed V_{OUT} (V_{OUT} = V_{FB} + 200mV + 800mV = 1.8V)

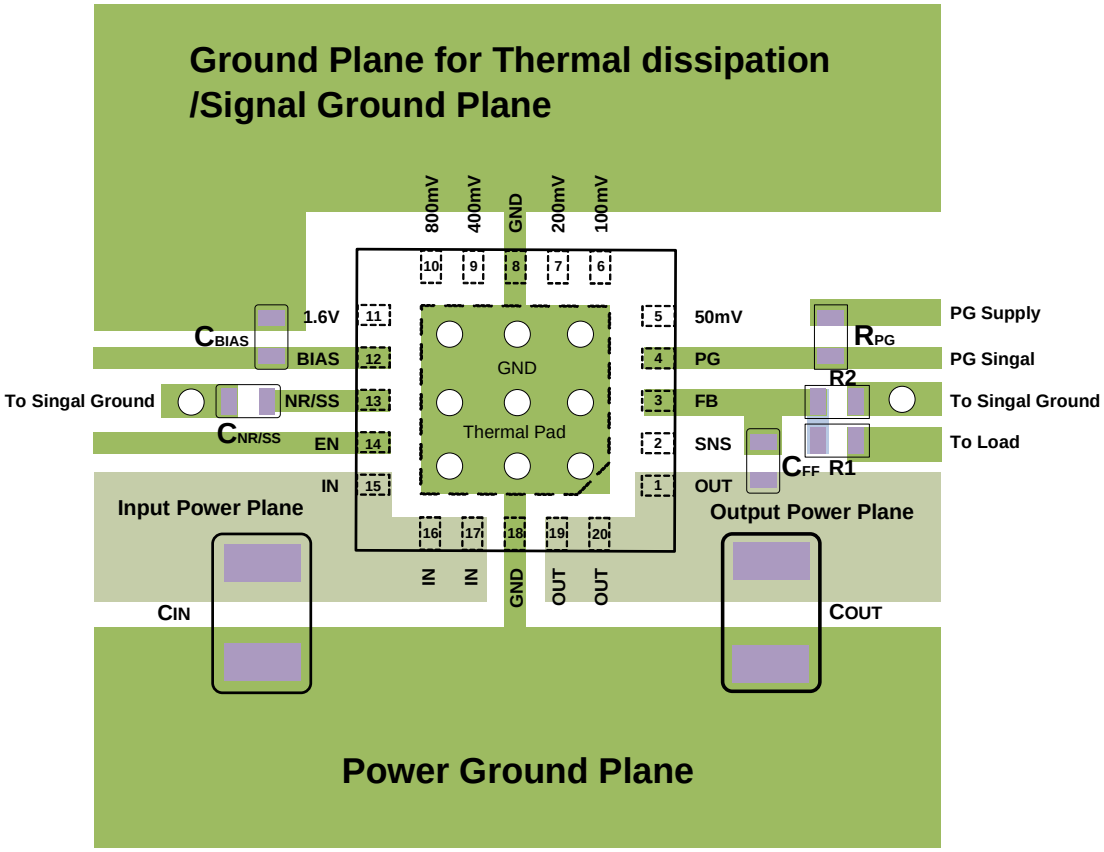
Table 7-2 Adjusted V_{OUT} by pin-setting

V_{FB} = 0.8 V, SNS connect to V_{OUT}						
V_{OUT}(V)	**50mV**	**100mV**	**200mV**	**400mV**	**800mV**	**1.6V**
0.80	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
0.85	GND	OPEN	OPEN	OPEN	OPEN	OPEN
0.90	OPEN	GND	OPEN	OPEN	OPEN	OPEN
0.95	GND	GND	OPEN	OPEN	OPEN	OPEN
1.00	OPEN	OPEN	GND	OPEN	OPEN	OPEN
1.05	GND	OPEN	GND	OPEN	OPEN	OPEN
1.10	OPEN	GND	GND	OPEN	OPEN	OPEN
1.15	GND	GND	GND	OPEN	OPEN	OPEN
1.20	OPEN	OPEN	OPEN	GND	OPEN	OPEN
1.25	GND	OPEN	OPEN	GND	OPEN	OPEN
1.30	OPEN	GND	OPEN	GND	OPEN	OPEN
1.35	GND	GND	OPEN	GND	OPEN	OPEN
1.40	OPEN	OPEN	GND	GND	OPEN	OPEN
1.45	GND	OPEN	GND	GND	OPEN	OPEN
1.50	OPEN	GND	GND	GND	OPEN	OPEN
1.55	GND	GND	GND	GND	OPEN	OPEN
1.60	OPEN	OPEN	OPEN	OPEN	GND	OPEN
1.65	GND	OPEN	OPEN	OPEN	GND	OPEN
1.70	OPEN	GND	OPEN	OPEN	GND	OPEN
1.75	GND	GND	OPEN	OPEN	GND	OPEN
1.80	OPEN	OPEN	GND	OPEN	GND	OPEN
1.85	GND	OPEN	GND	OPEN	GND	OPEN
1.90	OPEN	GND	GND	OPEN	GND	OPEN
1.95	GND	GND	GND	OPEN	GND	OPEN
2.00	OPEN	OPEN	OPEN	GND	GND	OPEN

V_{FB} = 0.8 V, SNS connect to V_{OUT}						
V_{OUT}(V)	**50mV**	**100mV**	**200mV**	**400mV**	**800mV**	**1.6V**
2.05	GND	OPEN	OPEN	GND	GND	OPEN
2.10	OPEN	GND	OPEN	GND	GND	OPEN
2.15	GND	GND	OPEN	GND	GND	OPEN
2.20	OPEN	OPEN	GND	GND	GND	OPEN
2.25	GND	OPEN	GND	GND	GND	OPEN
2.30	OPEN	GND	GND	GND	GND	OPEN
2.35	GND	GND	GND	GND	GND	OPEN
2.40	OPEN	OPEN	OPEN	OPEN	OPEN	GND
2.45	GND	OPEN	OPEN	OPEN	OPEN	GND
2.50	OPEN	GND	OPEN	OPEN	OPEN	GND
2.55	GND	GND	OPEN	OPEN	OPEN	GND
2.60	OPEN	OPEN	GND	OPEN	OPEN	GND
2.65	GND	OPEN	GND	OPEN	OPEN	GND
2.70	OPEN	GND	GND	OPEN	OPEN	GND
2.75	GND	GND	GND	OPEN	OPEN	GND
2.80	OPEN	OPEN	OPEN	GND	OPEN	GND
2.85	GND	OPEN	OPEN	GND	OPEN	GND
2.90	OPEN	GND	OPEN	GND	OPEN	GND
2.95	GND	GND	OPEN	GND	OPEN	GND
3.00	OPEN	OPEN	GND	GND	OPEN	GND
3.05	GND	OPEN	GND	GND	OPEN	GND
3.10	OPEN	GND	GND	GND	OPEN	GND
3.15	GND	GND	GND	GND	OPEN	GND
3.20	OPEN	OPEN	OPEN	OPEN	GND	GND
3.25	GND	OPEN	OPEN	OPEN	GND	GND
3.30	OPEN	GND	OPEN	OPEN	GND	GND
3.35	GND	GND	OPEN	OPEN	GND	GND
3.40	OPEN	OPEN	GND	OPEN	GND	GND
3.45	GND	OPEN	GND	OPEN	GND	GND
3.50	OPEN	GND	GND	OPEN	GND	GND
3.55	GND	GND	GND	OPEN	GND	GND
3.60	OPEN	OPEN	OPEN	GND	GND	GND
3.65	GND	OPEN	OPEN	GND	GND	GND
3.70	OPEN	GND	OPEN	GND	GND	GND
3.75	GND	GND	OPEN	GND	GND	GND
3.80	OPEN	OPEN	GND	GND	GND	GND
3.85	GND	OPEN	GND	GND	GND	GND
3.90	OPEN	GND	GND	GND	GND	GND
3.95	GND	GND	GND	GND	GND	GND

8 Layout guideline

Figure 8-1 Typical GD30LD3301x layout guideline



Notes:

1. The capacitor C_{IN} and C_{OUT} should be placed on the top layer to reduce parasitic parameters.
2. All capacitors are as close as possible to the corresponding pins of the LDO.

.

9 Package information

9.1 QFN20 package outline dimensions

Figure 9-1 QFN20 package outline

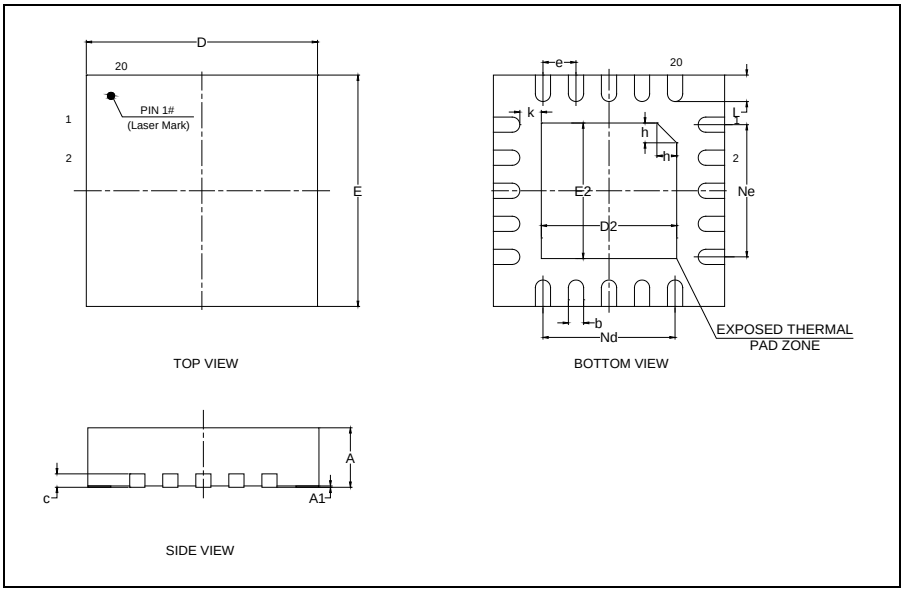
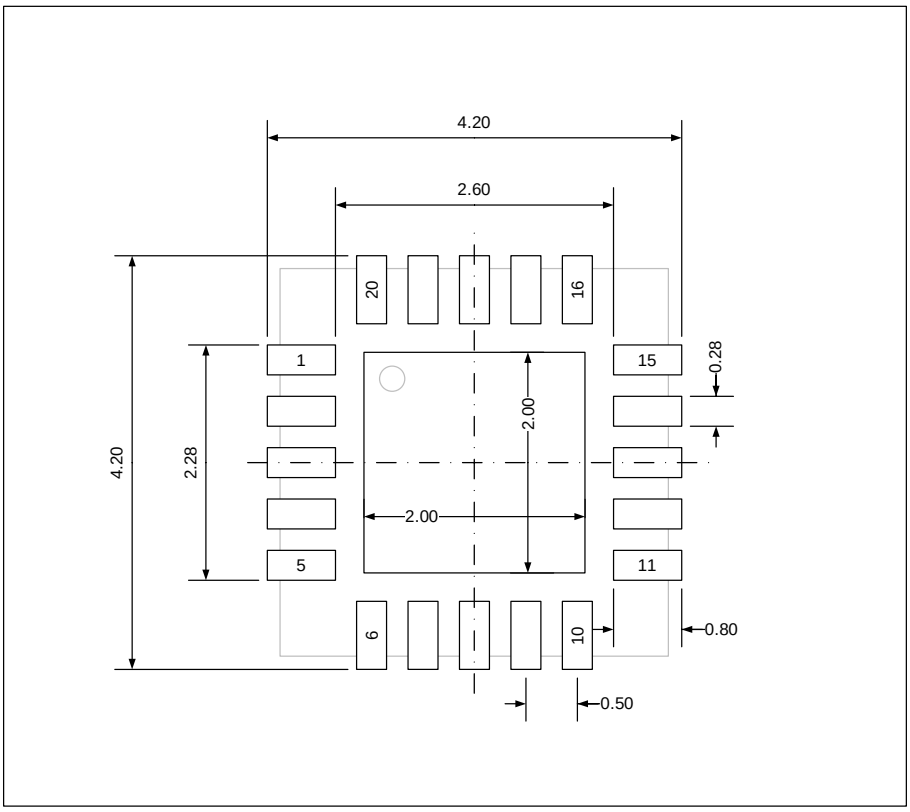


Table 9-1. QFN20 dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.23	0.30
c	—	0.203	—
D	3.40	3.50	3.60
D2	1.95	2.05	2.15
E	3.40	3.50	3.60
E2	1.95	2.05	2.15
e	—	0.50	—
h	0.25	0.30	0.35
K	0.275	0.325	0.375
L	0.35	0.40	0.45
Nd	—	2.00	—
Ne	—	2.00	—

(Original dimensions are in millimeters)

Figure 9-2 QFN20 recommend footprint



(All dimensions are in millimeters)

9.2 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "Θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$\Theta_{JA} = (T_J - T_A)/P_D$

$\Theta_{JB} = (T_J - T_B)/P_D$

$\Theta_{JC} = (T_J - T_C)/P_D$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

Θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 9-2. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
Θ_{JA}	Natural convection, 2S2P PCB	QFN20	53.17	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	QFN20	18.96	°C/W
$\Theta_{JC(Top)}$	Cold plate, 2S2P PCB	QFN20	30.61	°C/W
$\Theta_{JC(Bottom)}$	Cold plate, 2S2P PCB	QFN20	7.88	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	QFN20	19.14	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	QFN20	2.56	°C/W

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

10 Ordering information

Table 10-1 Part ordering code for GD30LD3301x devices

Ordering Code	Package	Package Type	Temperature Junction Range
GD30LD3301FUTR	QFN20	Green	Industrial -40°C to +125°C

11 Revision history

Table 11-1 Revision history

Revision No.	Description	Date
1.0	Initial Release	Dec.22, 2021
1.1	Modify the definition of BIAS pin, it is recommended to use a 1uF capacitor, the modification location is in the Table 4-1. GD30LD3301x QFN20 pin definitions. It is recommended to add specific values of peripheral devices to typical circuits, and the modification location is in Chapter 7. Modify the part ordering code information to GD30LD3301FUTR, the modification location is in the Table 10-1 Part ordering code for GD30LD3301x devices.	Mar.15,2022
1.2	Increase the parameter information of $\Theta_{JC(Bottom)}$, the modification location is in the Table 9-2. Package thermal characteristics(1). Modify the package outline dimensions and change the chip thickness to (minimum 0.70 typical 0.75 maximun 0.80), the modification location is in the Table 9-1. QFN20 dimensions.	APR.2, 2022

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company under the intellectual property laws and treaties of the People’s Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as it’s suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as it’s suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products.

Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and Products and services described herein at any time, without notice.