GigaDevice Semiconductor Inc.

Arm® Cortex®-M3 32-bit MCU

应用笔记

AN012

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1. 前言

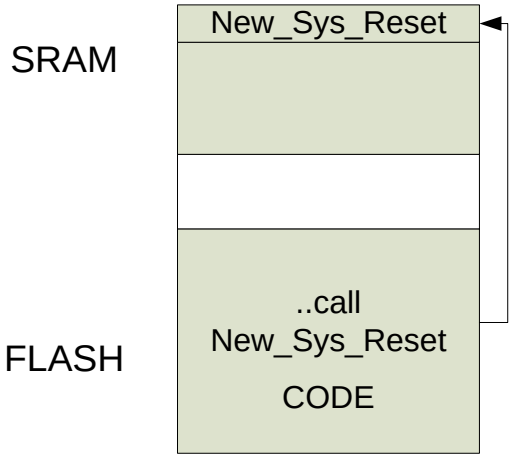
这篇应用笔记的编写目的是当MCU频繁复位时，避免芯片故障。通常，当有一个不好的或意外的条件发生时，在硬件或软件上会产生一个复位。当这个条件频繁发生时，复位也会频繁发生。为了获得更稳定的复位，本笔记基于GD32F10X和GD32F20X系列芯片，推荐如下的一些配置方法。

2. 配置方法

2.1 软件复位

软件复位主要是指在代码上触发了 MCU 的复位。软件复位函数的代码地址最好是放在 SRAM 的地址区域。

图 2-1. 地址区域



这个配置需要两个步骤：

首先，当复位函数声明时，为函数分配一个段名称。函数体内部由一个写 SCB->AIRCR 寄存器和一个 while 循环构成。例如复位函数在 nvic_conf.c 文件中，代码如下：

```
void Sys_Reset(void)  __attribute__((section ("New_Sys_Reset")));
void Sys_Reset(void)
{
    SCB->AIRCR  = (NVIC_AIRCR_VECTKEY | (SCB->AIRCR & (0x700)) |
(1<<NVIC_SYSRESETREQ));        /* Keep priority group unchanged */
    while(1);
}
```

其次，改变函数的执行地址。例如，可以改变分散加载文件，如果工程是在 Keil 中建立的。

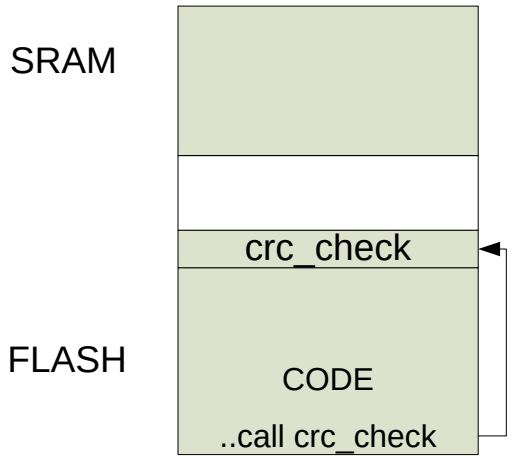
```
; *************************************************************
; *** Scatter-Loading Description File generated by uVision ***
; *************************************************************
LR_IROM1 0x08000000 0x00040000  {    ; load region size_region
  ER_IROM1 0x08000000 0x00040000  {  ; load address = execution address
   *.o (RESET, +First)
   *(InRoot$$Sections)
```

```
    *(+RO)
  }
  RW_IRAM1 0x20000000 0x0000A000  {  ; RW data
    .ANY (+RW +ZI)
  }
  ER_IRAM2 0x2000A000 UNINIT 0x00000400  {
     nvic_conf.o(New_Sys_Reset)
  }
}
```

2.2 硬件复位

MCU 上电时，FLASH 中的内容需要执行 CRC 校验。MCU 每次复位时，也会执行 CRC 计算，计算得到的结果与固件库下载时的 CRC 值进行比较。如果比较结果不一致，MCU 会进入 standby 模式并等待一个唤醒事件。当 MCU 被事件唤醒，会执行一个和上电复位一样的 FLASH 硬件修正过程。

图 2-2. FLASH 硬件修正过程



写代码时，建议遵循下列意见：

1. 程序的加载地址需要在 CRC 校验代码段和其他代码段之间。例如，CRC 校验代码段可以通过修改分散加载文件来配置在 FLASH 的尾部。CRC 校验函数在文件 crc_check.c 中，分散加载文件如下：

```
; *************************************************************
; *** Scatter-Loading Description File generated by uVision ***
; *************************************************************
LR_IROM1 0x08000000 0x0003F000  {      ; load region size_region
  ER_IROM1 0x08000000 0x0003F000  {  ; load address = execution address
    *.o (RESET, +First)
    *(InRoot$$Sections)
```

```
    *(+RO)
  }
  RW_IRAM1 0x20000000 0x00010000  {  ; RW data
   .ANY (+RW +ZI)
  }
}

LR_IROM2 0x0803F000 0x1000  {
    ER_IROM2 0x0803F000 0x1000  {
      crc_check.o (+RO)
  }
}
```

2. CRC 校验的输入条件不包括 CRC 校验代码段本身，意味着只包含其他代码段。

3. CRC 校验代码段在复位中断的一开始就被调用。

3. 版本历史

表 3-1. 版本历史

版本号.	描述	日期
1.0	首次发布	2021 年 04 月 30 日

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