GigaDevice Semiconductor Inc.

Arm® Cortex®- M3/M4/M23/M33 32-bit MCU

Application Note AN022



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1. Introduction

SDRAM is short for Synchronous Dynamic Random Access Memory. Synchronization means that memory work needs to synchronize clock, and internal command sending and data transmission are based on it; Dynamic means that the storage array needs constant refresh to ensure that the stored data is not lost. Because the data stored in SDRAM works through the capacitor, because the capacitor will discharge in the natural state, if the discharge is finished, it means that the data in SDRAM is lost, so SDRAM needs to refresh before the discharge of the capacitor is finished. Random means that the data is not stored in linear order, but read and write the data freely at the specified address.

Since SDRAM has some of the same characteristics as SRAM, if you need to run code on SDRAM, in addition to using MPU, you can also map SDRAM Device0 address (0xC000000) to 0x00000000 to run the code stored in SDRAM. This article introduces how to map SDRAM Device0 address (0xC000000) to 0x00000000 to run the code on GD32F450. Among them, APP_GPIO_Running_LED is the APP program programmed to SDRAM Device0 address (0xC000000). BOOT_EXMC_SDRAM is the BOOT program programmed to address 0x08000000.



2. FLM file

2.1. Custom SDRAM_256Mb.FLM file

This AN is based on GD32F450Z-EVAL evaluation board, equipped with a MT48LZ16M16 A2P-6AIT SDRAM with a capacity of 256Mb.

When making FLM files, the starting address is 0x00000000. The details are shown in *Figure 2-1. Address range of FLM file*.

Figure 2-1. Address range of FLM file

Description	Device Size	Device Type	Address Range
SDRAM_256Mb	256M	Unknown Device	00000000H - OFFFFFFH

2.2. Copy the FLM file to the Keil 5 installation path

Copy the SDRAM_256Mb.FLM file to the Keil 5 installation path, generally "C:\Keil_v5\ARM\Flash".



3. APP_GPIO_Running_LED project

3.1. Modify the project scatter-loading file

Since the APP_GPIO_Running_LED code is to run at address 0x00000000, it is necessary to modify the scatter-loading file of the project and load it to address 0x00000000. The details are shown in <u>Table 3-1. Scatter-loading file of APP_GPIO_Running_LED</u>.

Table 3-1. Scatter-loading file of APP_GPIO_Running_LED

```
LR_IROM1 0x0000000 0x00100000 {    ; load region size_region
    ER_IROM1 0x0000000 0x00100000 {    ; load address = execution address
    *.o (RESET, +First)
    *(InRoot$$Sections)
    .ANY (+RO)
    .ANY (+RO)
    .ANY (+XO)
    }
    RW_IRAM1 0x20000000 0x00030000 {    ; RW data
    .ANY (+RW +ZI)
    }
}
```

3.2. Modify the entry address of the interrupt vector table

Since the code itself runs at address 0x00000000, it is necessary to modify the entry address of the interrupt vector table of the APP project. You need to call nvic_vector_table_set at the appropriate location and set the entry address of the interrupt vector table to 0x0000000 and the offset to 0, as shown in <u>Table 3-2. Setting the entry address of interrupt vector table</u>.



Table 3-2. Setting the entry address of interrupt vector table



3.3. Add the SDRAM_256Mb.FLM file to the Keil project

Open the Keil project, in the Keil Flash download interface, add the SDRAM_256Mb.FLM file, and change the RAM for Algorithm Size to 0x2000, as shown in *Figure 3-1. Configration of Flash Algorithm in Keil project*. Then download the program to SDRAM.

Figure 3-1. Configration of Flash Algorithm in F	Keil project
--	--------------

-Downlos	ad Function Erase Full C Erase Sector Do not Erase	▼ Program ▼ Verify ■ Reset and Run	RAM for Alg	000000 ze: 0x2000
Progra	nming Algorithm			
Desci	ription	Device Size	Device Type	Address Range
SDRAM	_256МЪ	256M	Unknown Device	00000000H - OFFFFFFFH
•		"	!	•



4. BOOT_EXMC_SDRAM project

In the BOOT_EXMC_SDRAM project, you need to change the BOOT_MODE of the SYSCFG_CFG0 register to 0b`100. The specific implementation is shown in <u>Table 4-1. Set</u> boot mode to EXMC SDRAM.

Table 4-1. Set boot mode to EXMC SDRAM

.....

.

```
rcu_periph_clock_enable(RCU_SYSCFG);
syscfg_bootmode_config(<mark>SYSCFG_BOOTMODE_EXMC_SDRAM</mark>);
```

If EXMC clock is enabled and EXMC SDRAM has been configured in BOOT_EXMC_SDRAM, you can observe the value of SDRAM through debugging to see if it is the APP_GPIO_Running_LED code. The details are shown in *Figure 4-1. The value of 0xC0000000 in debug mode* and *Figure 4-2. The bin file compiled by the APP_GPIO_Running_LED project*.

Figure 4-1. The value of 0xC0000000 in debug mod
--

Memory 1					д
Address: 0xC000	0000				
0xC0000000:	20000408	000001C1	00000211	0000020D	
0xC0000010:	0000020F	00000209	00000289	00000000	
0xC0000020:	00000000	00000000	00000000	00000215	
0xC000030:	0000020B	00000000	00000213	00000217	
0xC0000040:	000001DB	000001DB	000001DB	000001DB	
0xC0000050:	000001DB	000001DB	000001DB	000001DB	
0xC0000060:	000001DB	000001DB	000001DB	000001DB	
0xC0000070:	000001DB	000001DB	000001DB	000001DB	
0xC0000080:	000001DB	000001DB	000001DB	000001DB	
0xC0000090:	000001DB	000001DB	000001DB	000001DB	
0xC00000A0:	000001DB	000001DB	000001DB	000001DB	
0xC00000B0:	000001DB	000001DB	000001DB	000001DB	
0xC00000C0:	000001DB	000001DB	000001DB	000001DB	
0xC00000D0:	000001DB	000001DB	000001DB	000001DB	
0xC00000E0:	000001DB	000001DB	000001DB	000001DB	
0xC00000F0:	000001DB	000001DB	000001DB	000001DB	
0xC0000100:	000001DB	000001DB	000001DB	000001DB	
0xC0000110:	000001DB	000001DB	000001DB	000001DB	
0xC0000120:	000001DB	000001DB	000001DB	000001DB	
0xC0000130:	000001DB	000001DB	000001DB	000001DB	
0xC0000140:	000001DB	000001DB	000001DB	000001DB	
0xC0000150:	000001DB	000001DB	000001DB	000001DB	
0xC0000160:	000001DB	000001DB	000001DB	000001DB	
0xC0000170:	000001DB	000001DB	000001DB	00000000	
0xC0000180:	000001DB	000001DB	000001DB	000001DB	
0xC0000190:	000001DB	000001DB	000001DB	00000000	
0xC00001A0:	000001DB	000001DB	000001DB	D00CF8DF	
0xC00001B0:	F818F000	47004800	0000037D	20000408	
0xC00001C0:	47804806	47004806	E7FEE7FE	E7FEE7FE	
0xC00001D0:	E7FEE7FE	E7FEE7FE	E7FEE7FE	0000021D	
0xC00001E0:	000001AD	4D074C06	68E0E006	0301F040	
0xC00001F0:	0007E894	34104798	D3F642AC	FFDAF7FF	
0xC0000200:	0000056C	0000058C	4770E7FE	E7FEE7FE	
0xC0000210:	47704770	F0004770	0000B85F	B4184816	
0xC0000220:	F4416801	60010170	68104A14	0001F040	
0xC0000230:	4C126010	68203408	0080F040	23006020	



A <u>d</u> dress:	0x0	<u>x1 x2</u>	x <u>4</u>		
Address	0	4	8	C	ASCII
0000	20000408	000001C1	00000211	0000020D	
0010	0000020F	00000209	00000289	00000000	
0020	00000000	00000000	00000000	00000215	
0030	0000020B	00000000	00000213	00000217	
0040	000001DB	000001DB	000001DB	000001DB	
0050	000001DB	000001DB	000001DB	000001DB	
0060	000001DB	000001DB	000001DB	000001DB	
0070	000001DB	000001DB	000001DB	000001DB	
0080	000001DB	000001DB	000001DB	000001DB	
0090	000001DB	000001DB	000001DB	000001DB	
00A0	000001DB	000001DB	000001DB	000001DB	
00B0	000001DB	000001DB	000001DB	000001DB	
0000	000001DB	000001DB	000001DB	000001DB	
00D0	000001DB	000001DB	000001DB	000001DB	
00E0	000001DB	000001DB	000001DB	000001DB	
00F0	000001DB	000001DB	000001DB	000001DB	
0100	000001DB	000001DB	000001DB	000001DB	
0110	000001DB	000001DB	000001DB	000001DB	
0120	000001DB	000001DB	000001DB	000001DB	
0130	000001DB	000001DB	000001DB	000001DB	
0140	000001DB	000001DB	000001DB	000001DB	
0150	000001DB	000001DB	000001DB	000001DB	
0160	000001DB	000001DB	000001DB	000001DB	

After configuring the BOOT_MODE of the SYSCFG_CFG0 register to 0b`100, you need to jump the program to the address where the APP_GPIO_Running_LED project is located to run the code. The specific configuration is shown in <u>Table 4-2. Jump to the address where</u> <u>the APP project is located to run the code</u>.



Table 4-2. Jump to the address where the APP project is located to run the code

```
typedef void (*pFunction)(void);
#define ApplicationAddress 0xC000000

pFunction Jump_To_Application;
uint32_t JumpAddress = 0;
.....
if (((*(__IO uint32_t*)ApplicationAddress) & 0x2FFE0000 ) == 0x20000000) {
    JumpAddress = *(__IO uint32_t*) (ApplicationAddress + 4);
    Jump_To_Application = (pFunction) JumpAddress;
    __set_MSP(*(__IO uint32_t*) ApplicationAddress);
    Jump_To_Application();
  }
......
```

After resetting the chip, it can be observed that the APP code is already running normally.



5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov.30 2021



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