# **GigaDevice Semiconductor Inc.**

# Arm<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit MCU

Application Note AN029



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## 1. Introduction

GD32F3xx and GD32F403 with Cortex-M4 kernel are launched by GD in recent years. These two series products can run 103 program directly. But the 103 program doesn't have the DSP instruction set. Is there a way to let the users to use the DSP instruction set and FPU when the program is based on 103? The answer is yes. The detailed method is show as below.

## 2. Operation steps

The following steps use Keil4 as an example, and the configuration method of Keil5 is exactly the same.

### 2.1 Turn on FPU

The 303 and 403 series have the FPU function. Some particular configuration need to be set as below.

1. Enable FPU before executing code

#### Figure 2-1. Enable FPU



2. Select 303 or 403 model and use FPU



#### Figure 2-2. Select 303 or 403 and enable FPU

💟 Options for Target '403_Math' 🛛 🕹					
Device Target Output Listing User   C/C++   Asm   Linker   Debug   Utilities					
GigaDevice GD32F403VE Xtal (MHz): 25.0					
Operating system:     None     Use Cross-Module Optimization       Surtem Viewer File ( Sfe):     Image: Use MicroLIB     Big Endian					
System-Viewer File (.str): SFD\GD\GD32F4xx\GD32F403.SFR Floating Point Hardware: Use FPU					
Read/Only Memory Areas default off-chip Start Size Startup	Read/Write Memory Areas default off-chip Start Size Nolnit				
□ ROM1: □ C	□ RAM1: □ □				
□ ROM2: □ ○	□ RAM2: □ □				
□ ROM3: □ O	□ RAM3: □ □				
on-chip	on-chip				
OK Cancel Defaults Help					

3. Fill in the corresponding compilation macro definition.

#### Figure 2-3. Add the corresponding compilation macro

🕎 Options for Target 'GD32F10X_HD'	×
Device Target Output Listing User C/C++ Asm Linker Debug Utilities	
Preprocessor Symbols Define: USE_STDPERIPH_DRIVER GD32F10X_CLFPU_PRESENTTARGET_FPU_VFP	
Undefine:	

Note: GD32F10X\_CL must be configured for F403, and F303 and F103 must be the same.

### 2.2 Check whether the FPU is turned on successfully

In the JLINK debugging control interface, enter the command:

mem32 0xE000ED88 1

See the following figure for detailed operation. After entering the command, 00f00000 indicates that the FPU has been turned on. If it is 00000000, it indicates that the FPU has not been turned on.

Figure 2-4. Check whether the FPU is turned on



```
T) cJTAG

TIF>swd

Specify target interface speed [kHz]. <Default>: 4000 kHz

Speed>

Device "GD32F303RE" selected.

Connecting to target via SWD

Found SW-DP with ID 0x2BA01477

Scanning AP map to find all available APs

AP[1]: Stopped AP scan as end of AP map has been reached

AP[0]: AHB-AP (IDR: 0x24770011)

Iterating through AP map to find AHB-AP to use

AP[0]: Core found

AP[0]: Core found

AP[0]: AHB-AP ROM base: 0xE00FF000

CPUID register: 0x410FC241. Implementer code: 0x41 (ARM)

Found Cortex-M4 r0p1, Little endian.

FPUnit: 6 code (BP) slots and 2 literal slots

CoreSight components:

ROMTb1[0][0]: E000E000, CID: B105E00D, PID: 000BB00C SCS-M7

ROMTb1[0][1]: E0001000, CID: B105E00D, PID: 003BB002 DWT

ROMTb1[0][2]: E0002000, CID: B105E00D, PID: 003BB002 DWT

ROMTb1[0][2]: E0002000, CID: B105E00D, PID: 003BB001 ITM

ROMTb1[0][3]: E0004000, CID: B105900D, PID: 003BB01 ITM

ROMTb1[0][4]: E0040000, CID: B105900D, PID: 003BB01 ITM

ROMTb1[0][5]: E0041000, CID: B105900D, PID: 003BB01 ITM

ROMTb1[0][5]: E0041000, CID: B105900D, PID: 003BB01 ITM

ROMTb1[0][5]: E0041000, CID: B105900D, PID: 000BB9A1 TPIU

ROMTb1[0][5]: E0041000, CID: 00000000, PID: 0000B9A1 TPIU

ROMTb1[0][5]: E0041000, CID: 00000000, PID: 00000000 ???

Cortex-M4 identified.

J-Link>mem32 0xE000ED88 1

3000ED88 = 00F00000
```

## 2.3 Performance test comparison

Compile the code, then the performance of M4 can be tested on 103 code.

```
int main (void)
{
   float i;
   float m = 2.5f;
   float n = 4;
   /* configure systick */
   systick config();
   /* initilize the LEDs, USART and key */
   gd eval led init (LED2);
   gd eval led init (LED3);
   gd eval led init (LED4);
   gd_eval_com_init(EVAL_COM0);
   gd_eval_key_init(KEY_WAKEUP, KEY MODE GPIO);
   while(1) {
      if (RESET == gd eval key state get (KEY WAKEUP)) {
          gd eval led on (LED3);
          i = m * n;
          gd eval led off(LED3);
```



```
printf("\r\ni = %f", i);
while(RESET == gd_eval_key_state_get(KEY_WAKEUP));
}
```

Grab the pin waveform of LED3 with the logic analyzer and check the calculation time of floating-point operation. The following is the test comparison between opening FPU and not opening FPU:

Figure 2-5. Comparison of performance test



If FPU is not enabled, a floating-point multiplication takes 640ns, and only 160ns after FPU is enabled.

### 2.4 Turn on DSP

1. Copy math.lib from the MDK path and add to the project. The specific document is arm\_cortexM4l\_math.lib. (If the FPU is used, arm\_cortexM4lf\_math.lib will be selected.)

新加卷 (D:) ▶ Keil ▶ ARM ▶ CMSIS ▶ I	ib 🕨 ARM		▼ 4 搜索	/
工具(T) 帮助(H)				
共享 ▼ 新建文件夹				
名称	修改日期	类型	大小	
🚔 arm_cortexM0l_math.lib	2012/10/24 11:07	Altium Library	10,364 KB	
🛃 arm_cortexM3I_math.lib	2012/10/24 11:07	Altium Library	10,656 KB	
🚔 arm_cortexM4l_math.lib	2012/10/24 11:07	Altium Library	10,822 KB	
🚔 arm_cortexM4lf_math.lib	2012/10/24 11:07	Altium Library	10,905 KB	

Figure 2-6. math.lib file

2. Copy the corresponding .H file to the project. The core\_cm4.h file is needed if DSP is used.



#### Figure 2-7. The required .H file

Firmware CMSIS			▼ 4 <sub>7</sub> ₩2≤ 14
LES When			
Area			
18 <sup>1</sup>	\$1535\$	zda.	<i>Q</i> .
🖺 arm math.h	2016/11/5 1:33	H文件	247 KB
📄 core_cm0.h	2016/11/5 1:33	H 文件	36 KB
core_cm0plus.h	2016/11/5 1:33	H 文件	43 KB
core_cm3.c	2010/6/7 10:25	C 文件	17 KB
core cm3.h	2016/11/5 1:33	H文件	102 KB
📋 core_cm4.h	2016/11/5 1:33	H 文件	112 KB
📋 core_cm4_simd.h	2017/4/27 16:18	H 文件	23 KB
📋 core_cmFunc.h	2016/11/5 1:33	H 文件	18 KB
core_cminstr.n	2010/11/3 1:55	n X1+	20 ND
📋 core_cmSimd.h	2016/11/5 1:33	H 文件	23 KB
📄 gd32f10x.h	2015/3/23 9:59	H 文件	699 KB
system_gd32f10x.c	2015/1/19 9:08	C 文件	38 KB
📄 system_gd32f10x.h	2015/1/19 9:08	H 文件	2 KB

3. Change the core\_cm3.h to core\_cm4.h in gd32f10x.h file.

Figure 2-8. Core\_cm3.h changed to core\_cm4.h



4. Modify the selection of the MCU model. 303 select the corresponding 303 model, 403 select the corresponding 403 model and the corresponding Math compilation macro.



### Figure 2-9. Modify the chip model

Options for Target '303_Math'	X
Device Target Output Listing User C/C++ Asm Linker Debug Utilities Database: GigaDevice GD32F30x Devices V Vendor: GigaDevice Device: GD32F303RG Toolset: ARM	
GigaDevice GD32F303CC GD32F303CC GD32F303CC GD32F303CC GD32F303CC GD32F303CC GD32F303RC GD32F303RC GD32F303RC GD32F303RC GD32F303RC GD32F303RC GD32F303RC GD32F303RK GD32F303RK GD32F303VC GD32F302C GD32F302C GD32F302C GD32F302C	
OK Cancel Defaults	Help

Figure 2-10. Add the corresponding Math compilation macro

Options for Target '303_Math'		x		
Device Target Output Listing User C/C++ Asm Linker Debug Vtilities				
Preprocessor Symbols				
Define: USE_STDPERIPH_DRIVER,GD32F10X_HD,MATH_313,ARM_MATH_CM4				
Undefine:				
Language / Code Generation		Warringe		
	Strict ANSI C	Warnings.		
Optimization: Level 0 (-00)	Enum Container always int			
Optimize for Time	Plain Char is Signed	Thumb Mode		
Split Load and Store Multiple	Read-Only Position Independent	No Auto Includes		
☑ One ELF Section per Function	Read-Write Position Independent			
Include Paths Misc				
Controls				
Compiler -ccpu Cortex-M4 -D_MICROLIB -g -O0apcs=interworksplit_sections -l\ -l\\Firmware \Peripherals\inc -l\\Firmware\CMSIS				
	Concol Defendato			
	Cancer Defaults	летр		





## 3. Revision history

### Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.30, 2021



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