GigaDevice Semiconductor Inc.

GD32F1
ARM® Cortex®-M3 32-bit MCU

Application Note
AN004

Table of Contents

Table of Contents 1

1 Introduction 2

2 GD32F10xx4/6/8/B version D limitations 2

2.1 USART RTS pin multiplexing 2

2.2 GPIO 5V output in open drain mode 2

3 GD32F10xxC/D/E/F/G/I/K version B limitations 3

3.1 System boot clock 3

3.2 Specified power down threshold voltage 3

4 GD32F1x0 version A limitations 4

4.1 System boot clock 4

4.2 Specified power down threshold voltage 4

5 GD32F1x0 version B limitations 5

5.1 SPI clock interference in master mode 5

5.2 Timer PWM output status when stops under debug mode 5

6 Revision history 6

1 Introduction

The objective of this application note is to explain the silicon limitations of GD32F1 series device known at the release date of this document. The purpose is not to provide detailed electrical specifications on the devices, but to highlight the known limitations and relevant workarounds.

2 GD32F10xx4/6/8/B version D limitations

2.1 USART RTS pin multiplexing

Description

While using USART without RTS modem operation, the relevant RTS pin has been occupied and can not be used as other alternate functions.

Workaround

This limitation has been revised and not existed in the following new version chips.

2.2 GPIO 5V output in open drain mode

Description

When GPIO is configured and outputting “1” in open drain mode, the voltage level should be determined by the external pull-up resistor voltage on PCB. However, the output can not reach 5V even the pull-up resistor voltage is 5V.

Workaround

This limitation has been revised and not existed in the following new version chips.

3 GD32F10xxC/D/E/F/G/I/K version B limitations

3.1 System boot clock

Description

The HSI clock is generated by an internal 8 MHz RC Oscillator and used directly as PLL system boot clock input during device power on period. While additional noise is introduced on HSI clock from circuit board, it will delay the PLL lock procedure and impact the PLL clock ready flag set. That may cause an unpredictable power on delay (which may be detected as boot failure) in some conditions.

Set HSI clock to be the system boot clock directly will help to eliminate the effects.

Workaround

This limitation has been revised and not existed in the following new version chips.

3.2 Specified power down threshold voltage

Description

During power on period, MCU remains in reset mode When V_{DDA} is below V_{POR}. During power down period, the integrated PDR Circuit keeps MCU under reset when V_{DDA} drops down V_{PDR}. Proper threshold of V_{PDR} allows proper operation down below 2V.

Workaround

This limitation has been revised and not existed in the following new version chips.

Specified power down Voltage (V_{PDR}) of new version chip has been changed from 2.38V to 1.86V (in typical condition).

4 GD32F1x0 version A limitations

4.1 System boot clock

Description

The HSI clock is generated by an internal 8 MHz RC Oscillator and used directly as PLL system boot clock input during device power on period. While additional noise is introduced on HSI clock from circuit board, it will delay the PLL lock procedure and impact the PLL clock ready flag set. That may cause an unpredictable power on delay (which may be detected as boot failure) in some conditions.

Set HSI clock to be the system boot clock directly will help to eliminate the effects.

Workaround

This limitation has been revised and not existed in the following new version chips.

4.2 Specified power down threshold voltage

Description

During power on period, MCU remains in reset mode When V_{DDA} is below V_{POR}. During power down period, the integrated PDR circuit keeps MCU under reset when V_{DDA} drops down V_{PDR}. Proper threshold of V_{PDR} allows proper operation down below 2V.

Workaround

Specified power down Voltage (V_{PDR}) can be changed from 2.38V to 1.86V (in typical condition) or other lower values by relevant register setting of GD32F1x0.

5 GD32F1x0 version B limitations

5.1 SPI clock interference in master mode

Description

The SPI clock (SPI_SCK) of master mode is detected the occurrence of noise generated by external interference, which causes the SPI abnormal application behavior under certain circumstances.

Workaround

This limitation has been revised and not existed in the following new version chips.

5.2 Timer PWM output status when stopped under debug mode

Description

When the MCU enters debug mode that the clock of the involved timer counter is set to be stopped inside a break point by register configuration, CHx and CHxN of PWM output also stops in the previous status, which may cause the unexpected status in application. The PWM outputs should also be disabled as if there were an emergency stop in response to a break event.

Workaround

This limitation has been revised and not existed in the following new version chips.

6 Revision history

Table 1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jan.6, 2014
2.0	Chapter 3 & Chapter 4 of new devices added	Aug.1, 2014
2.1	Chapter 5 updated	Feb.8, 2015