GigaDevice Semiconductor Inc.

GD30DR8413x
Triple Half Bridge Motor Driver

Datasheet

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1 Features

- 4.5-30V Supply Voltage
- Triple Half Bridge to Drive BLDC or Brushed DC Motor
- High Drive Currents up to 3A
- Independent Half Bridge Control up to 200 kHz
- Low On Resistance Built in MOSFET
- Built in LDO of 5V, support up to 20mA load
- Small package and footprint 4x4mm QFN24 with enhanced thermal ground
- Protection Features:
  - Over Temperature shutdown
  - Supply undervoltage lockout

2 Applications

- 3-Phase BLDC Motors
- Brushed Motor for Power Tools
- Industrial Automation

3 General description

The GD30DR8413x integrates three individually controllable half bridge drivers, to drive a 3-phase BLDC motor or other inductive loads. Each driver is composed of two NMOSFETs which support up to 3A source and sink current. The GD30DR8413x can operate with a single power supply ranging from 4.5V to 30V. A regulated Bootstrap circuit is integrated in the device to supply the high side gate drive currents. Dead time and automatic handshaking is applied to prevent the high side and low side NMOSFETs from shoot through when switching. Each half bridge has an optional terminal which allows external current sensing. The IC has a LDO for both internal circuit and external output up to 20mA. A general purpose comparator is also integrated in the device.

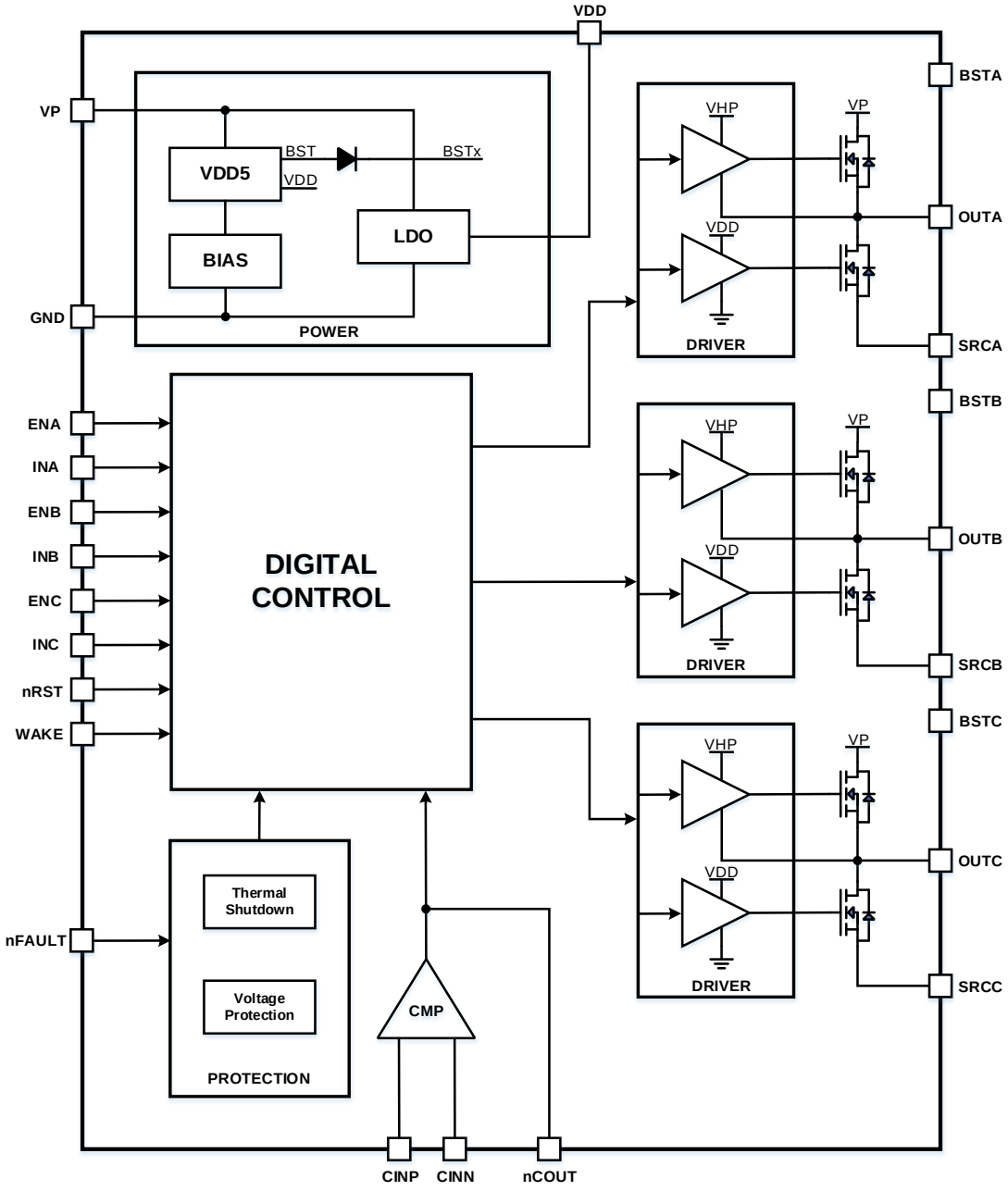
Multiple internal protection features are implemented to prevent the IC and system from malfunction damage. The protection includes supply undervoltage lockout,-over temperature. All the protection features are reported through nFAULT pin.

The versatile features of the IC allow for it to be used in a broad range of applications, such as BLDC motors, brushed DC motors, etc. The GD30DR8413x is available in thermal enhanced package QFN24.

4 Device overview

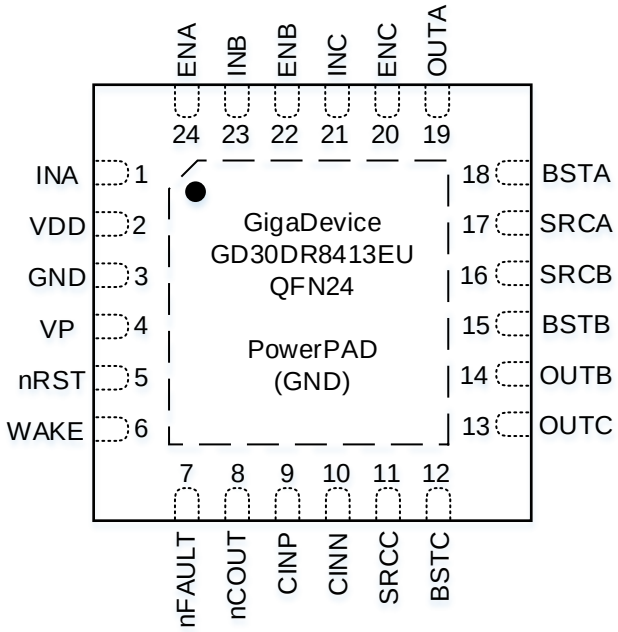
4.1 Block diagram

Figure 4-1 Block diagram for GD30DR8413x



4.2 Pinout and pin assignment

Figure 4-2 GD30DR8413x QFN24 Pinouts



4.3 Pin definitions

The table below shows the pin definition of GD30DR8413x.

Table 4-1. GD30DR8413x PIN Configuration

PIN		TYPE	DESCRIPTION
NAME	NO.		
INA	1	I	Input signal for half bridge A from MCU
VDD	2	P	5V internal digital supply regulator; bypass to GND with a 1μF ceramic capacitor
GND	3	G	Ground for device
VP	4	P	Power supply voltage for IC and motor; common for all three half bridges; bypass to GND with a 10μF ceramic capacitor
nRST	5	I	Reset signal from MCU, low effective
WAKE	6	I	Wakeup signal from MCU; high effective; stay low put IC into sleep mode
nFAULT	7	OD	Open drain fault indicator; when low indicates a fault has occurred; external pullup to MCU power supply needed (1kΩ to 10kΩ)
nCOUT	8	OD	Open drain comparator output
CINP	9	I	Comparator input
CINN	10	I	Comparator input
SRCC	11	O	Source of driver C low-side NMOS; connect to ground or to a current sense resistor
BSTC	12	P	Bootstrap to drive C high-side NMOS; connect a 0.1uF capacitor to OUTC
OUTC	13	O	Half bridge driver C output; connect to load
OUTB	14	O	Half bridge driver B output; connect to load
BSTB	15	P	Bootstrap to drive B high-side NMOS; connect a 0.1uF capacitor to OUTB
SRCB	16	O	Source of driver B low-side NMOS; connect to ground or to a current sense resistor
SRCA	17	O	Source of driver A low-side NMOS; connect to ground or to a current sense resistor
BSTA	18	P	Bootstrap to drive A high-side NMOS; connect a 0.1uF capacitor to OUTA
OUTA	19	O	Half bridge driver A output; connect to load
ENC	20	I	Enable for half bridge C; internal pull-down by 50KΩ resistor
INC	21	I	Input signal for half bridge C from MCU
ENB	22	I	Enable for half bridge B; internal pull-down by 50KΩ resistor

PIN		TYPE	DESCRIPTION
NAME	NO.		
INB	23	I	Input signal for half bridge B from MCU
ENA	24	I	Enable for half bridge A; internal pull-down by 50KΩ resistor
PGND	Thermal	G	Enhanced thermal pad and device ground; must connect to ground

Notes:

Type: I = input, O = output, P = power, OD = open drain, G = ground.

5 Functional description

5.1 Functional mode

The GD30DR8413x is a gate driver IC designed for 3-phase motor driver applications, operating in a wide range of 4.5V to 30V. This device integrates three independent controllable half bridge drivers and one general purpose comparator.

The GD30DR8413x enters standby mode when WAKE goes low for more than t_{SLEEP} (typically 1ms). The outputs will remain High-Z in standby mode. In sleep mode charge pump, gate driver and VDD will be all turned off. After WAKE goes high for at least 5us, the device will be in active mode twake (1ms) later.

In active mode, if the device triggers the protection feature in operation, it will enter different fault status depending on the protection features. All the faults can be cleared or reset by pulling the nRST pin to low. All the inputs will be ignored while nRST is low.

Table 5-1 Function blocks' status and device mode

Mode	Conditions	H-Bridge	VDD
Active	WAKE=1, NO FAULT	ON	ON
Sleep	WAKE=0	OFF	OFF
FAULT	Under Voltage Lockout	OFF	ON
	Over Temperature	OFF	ON

5.2 Half bridge driver

Three independent half bridge drivers are implemented in GD30DR8413x. All three H bridges output OUTx are controlled only by INx and ENx.

Table 5-2 Truth table for H-Bridge output

INx	ENx	OUTx
X	Hi-Z	Hi-Z
H	H	H
L	H	L

Notes:

Type: X = Don't care, Hi-Z = High Impedance, H = High level, L = Low level.

The sources of low side NMOSFET of the three H bridges are separated to allow the sensing of the current of each bridge independently. Or they can be connected together to ground if not needed. In any case, the voltages on these three nodes are ensured not to exceed +/-500mV.

5.3 Comparator

A general purpose comparator is integrated in GD30DR8413x. For example, it can be used to sense the total current of the 3-phase drive with a single sense resistor connected to all SRCx of the device.

5.4 Bootstrap circuit and internal supply

A bootstrap circuit is integrated to generate the appropriate gate to source voltage bias for the high side NMOSFET. The Bootstrap voltage VBSTx are all regulated at 5V above VP when VP is higher than 6V. A regulated 5V VDD derived from the VP supplies the gate to source voltage for the low side NMOSFET.

5.5 Protection features

5.5.1 Over temperature protection

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}, typical 170°C), all the NMOSFETs are disabled, the internal power supplies are shut down. Normal operation starts again when the temperature falls below the hysteresis and the over temperature condition clears.

5.5.2 Under voltage lockout

At any time if the voltage on the power supply VP UVLO threshold, all the internal NMOSFETs in the H bridge will be disabled. Normal operation will resume when VP rises above UVLO threshold. Also the Bootstrap voltage is also monitored.

6 Electrical characteristics

6.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device's reliability.

Table 6-1. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Gate driver and comparator				
V_{VP}	Power supply pin voltage (VP)	-0.3	36	V
—	Voltage differential between ground pins (GND, PGND)	-0.3	0.3	V
V_{BSTx}	Bootstrap voltage to drive high-side NMOS	-0.3	V_{VP} + 6	V
V_{VDD}	Digital pin voltage (ENx, INx, nRST, nFAULT, Wake, nCOUT)	-0.3	5.75	V
V_{OUTx}	Continuous output drive pin voltage (OUTx)	-1.5	V_{VHP} + 0.5	V
	Transient 200 ns output drive pin voltage (OUTx)	-3	V_{VHP} + 0.5	V
V_{SRCx}	Sense voltage at driver low-side NMOS (SRCx)	-0.6	0.6	V
V_{CINx}	Input voltage to comparator (CINP, CINN)	-0.6	0.6	V
I_{SRC}	OUTx pin source current	Internally limited		A
I_{SNK}	OUTx pin sink current	Internally limited		A
Thermal parameters				
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

6.2 Recommended operation conditions

Table 6-2 Recommended operation conditions

Symbol	Parameter	Min	Max	Unit
Gate drivers and comparator				
V_{VP}	Power supply voltage (VP)	4.5	30	V
V_I	Input voltage (ENx,Inx, nRST, Wake)	0	5.5	V
f_{INx}	Input INx signal (INx)	0	200	kHz
I_{SNK}	Maximum continuous sink current (OUTx)	—	3	A
I_{SRC}	Maximum continuous source current (OUTx)	—	3	A
I_{VDD}	External load current (VDD)	0	20	mA
V_{OD}	Open drain pullup voltage (nFAULT, nCOUT)	0	5.5	V
I_{OD}	Open drain output current (nFAULT, nCOUT)	0	5	mA
Thermal parameter				
T_J	Operating junction temperature	-40	125	°C

6.3 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample.

Table 6-3 Electrostatic Discharge

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JS-001-2017	TBD	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C JS-002-2018	TBD	V

6.4 Power supplies and current consumption

Table 6-4 Power supplies and currents

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VP}	VP operating supply current	V_{VP} = 24 V, EN = 3.3 V, OUTx = 0 V	—	3.0	—	mA
I_{VPQ}	VP sleep mode supply current	WAKE = 0 V, V_{VP} = 24 V, T_A = 25°C	—	30	—	µA
		WAKE = 0 V, V_{VP} = 24 V, T_A = 125°C	—	—	—	µA
t_{RST}	Reset pulse time	nRST= 0 V to reset faults	8	—	40	µs
t_{WAKE}	Turn on time	V_{VP} > V_{UVLO}, WAKE = 3.3 V to outputs ready	1	—	—	ms
t_{SLEEP}	Turn off time	WAKE = 0 V to device sleep mode	1	—	—	ms
V_{VDD}	VDD regulator voltage	I_{VDD} = 0 to 20 mA	—	5	—	V
V_{BST}	$V_{BST\ to\ VP}$	V_{VP} = 12 V	—	5	—	V

6.5 Logic inputs characteristics

Logic input pins include ENx, INx, nRST, WAKE.

Table 6-5 Logic input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input logic low voltage	—	0	—	0.8	V
V_{IH}	Input logic high voltage	—	1.5	—	5.5	V
V_{HYS}	Input logic hysteresis	—	100	—	—	mV
I_{IL}	Input logic low current	V_{VIN} = 0 V	-5	—	5	μA
I_{IH}	Input logic high current	V_{VIN} = 5 V	—	50	70	μA
R_{PD}	Pulldown resistance	ENx, INx, Wake To GND	100	—	—	kΩ
t_{PD}	Propagation delay	INx transition to OUTx transition	TBD	—	—	ns

6.6 Open drain outputs characteristics

Open drain output pins include nFAULT, nCOUT.

Table 6-6 Open drain output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output logic low voltage	I_O = 5 mA	—	—	0.1	V
I_{OZ}	Output high impedance leakage	V_O = 5 V	-2	—	2	μA

6.7 Gate driver characteristics

Gate driver pins include OUTx, SRCx.

Table 6-7 Gate driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{DTF}	Gate drive dead time (Fixed)	Guaranteed by design	—	300	—	ns
I_{SRC}	Peak source gate current	—	—	3	—	A
I_{SNK}	Peak sink gate current	—	—	3	—	A
R_{OFF}	Gate hold off resistor	OUTx to SRCx	—	100	—	kΩ
R_{ONH}	High side NMOSFET on resistance	—	—	140	—	mΩ
R_{ONL}	Low side NMOSFET on resistance	—	—	140	—	mΩ

6.8 Protection features

Protection features include over current protection, under voltage lockout and thermal shutdown.

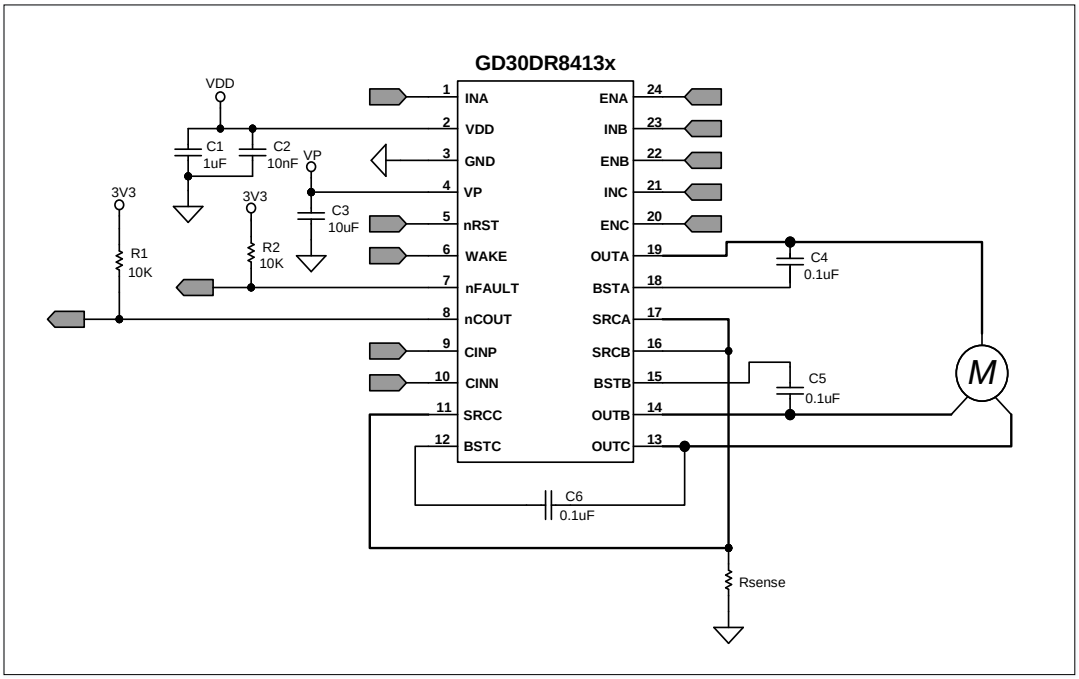
Table 6-8 Protection features' characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{UVLO}	VP undervoltage lockout	VP rising, UVLO	—	4.3	—	V
		VP falling, UVLO	—	4.1	—	
V_{UVLO_HYS}	VP undervoltage hysteresis	Rising to falling threshold	—	200	—	mV
t_{UVLO_DEG}	VP undervoltage deglitch time	VP falling, UVLO	—	10	—	μs
V_{BST_UV}	Bootstrap voltage undervoltage lockout	V_{BST} falling, CPUV	—	V_{VP} + 2.2	—	V
T_{OTSD}	Thermal shutdown temperature	Die temperature, T_J	150	170	185	°C
T_{HYS}	Thermal hysteresis	Die temperature, T_J	—	20	—	°C

7 Typical application circuit

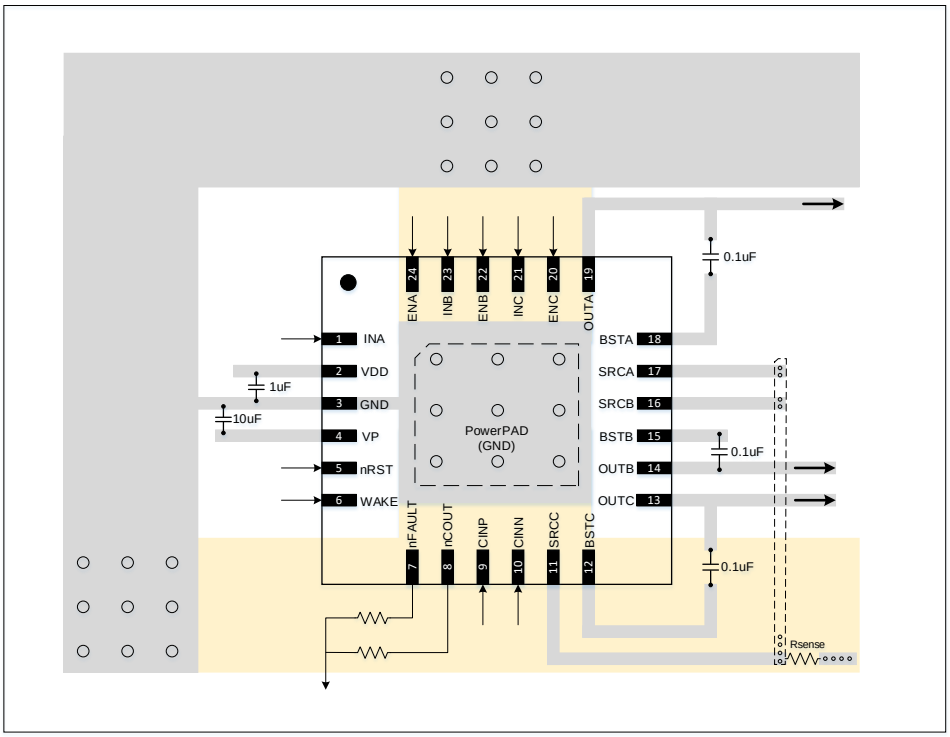
Figure 7-1 Typical application circuit

In this application, the GD30DR8413x is used to drive a 3-phase BLDC or Brushed DC motor.



8 Layout guideline

Figure 8-1 Typical layout guideline



Notes:

1) The VDD 1uF bypass capacitors should connect directly the VDD to ensure loop stability.
2) The VP 10uF bypass capacitor should be placed close to the supply pin with a direct path back to the GND pad.
3) The 0.1uF Bootstrap capacitors should connect to the BSTX/OUTX pins.
4) All capacitors should be as close to the chip pin as possible.
5) The high-current device outputs should use wide metal traces.
6) The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the I2 × rDS(on) heat that is generated in the device.

9 Package information

9.1 QFN package outline and dimensions

Figure 9-1 QFN24 package outline

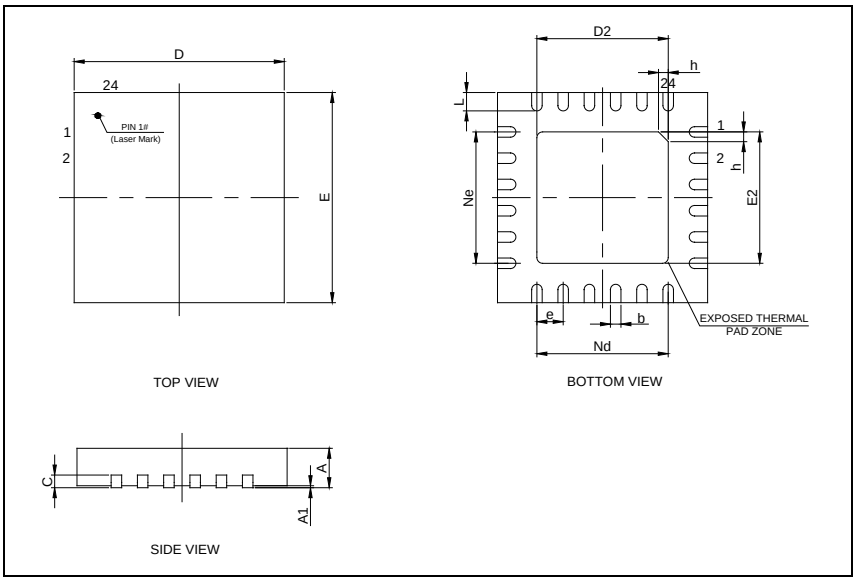
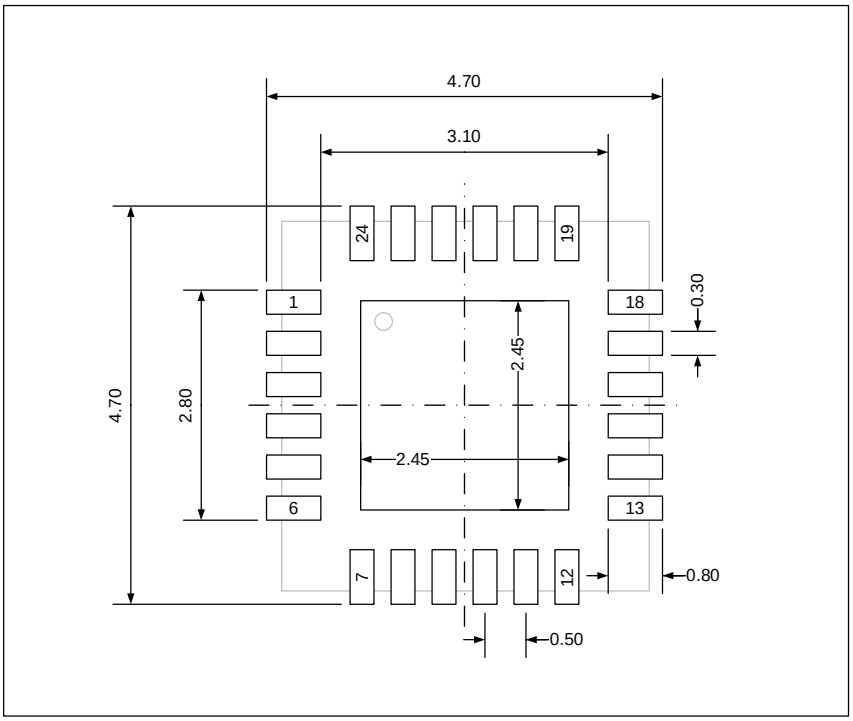


Table 9-1 QFN24 dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
e	—	0.50	—
h	0.30	0.35	0.40
L	0.35	0.40	0.45
Nd	—	2.50	—
Ne	—	2.50	—

(original dimensions are in millimeters)

Figure 9-2 QFN24 recommend footprint



(All dimensions are in millimeters)

9.2 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "Θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$\Theta_{JA} = (T_J - T_A)/P_D$

$\Theta_{JB} = (T_J – T_B)/P_D$

$\Theta_{JC} = (T_J – T_C)/P_D$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

Θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 9-2 Package Thermal Information(1)

Symbol	Condition	Package	Value	Unit
Θ_{JA}	Natural convection, 2S2P PCB	QFN24	47.51	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	QFN24	14.9	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	QFN24	20.99	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	QFN24	15.05	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	QFN24	0.86	°C/W

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

10 Ordering information

Table 10-1 Part order code for GD30DR8413x device

Part Order Code	Package	Package Type	Temperature Operating Range(T_J)
GD30DR8413EUTR	QFN24	Green	Industrial -40°C to +125°C

11 Revision history

Table 11-1 Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.30, 2022
1.0	Modify section 9.2 package thermal information condition description	May.20, 2022

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