GigaDevice Semiconductor Inc.

GD32F4xx Hardware Development Guide

Application Note
AN056

Revision 1.2

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1. Introduction

The article is specially provided for developers of 32-bit general-purpose MCU GD32F4xx series based on Arm® Cortex®-M4 architecture. It provides an overall introduction to the hardware development of GD32F4xx series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32F4xx series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32F4xx series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32F4xx series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32F4xx series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32F4xx series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32F4xx series.
6. Reference circuit and PCB Layout design, mainly introduces GD32F4xx series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32F4xx series.

This document also satisfies the minimum system hardware resources used in application development based on GD32F4xx series products.

Table 1-1. Applicable Products

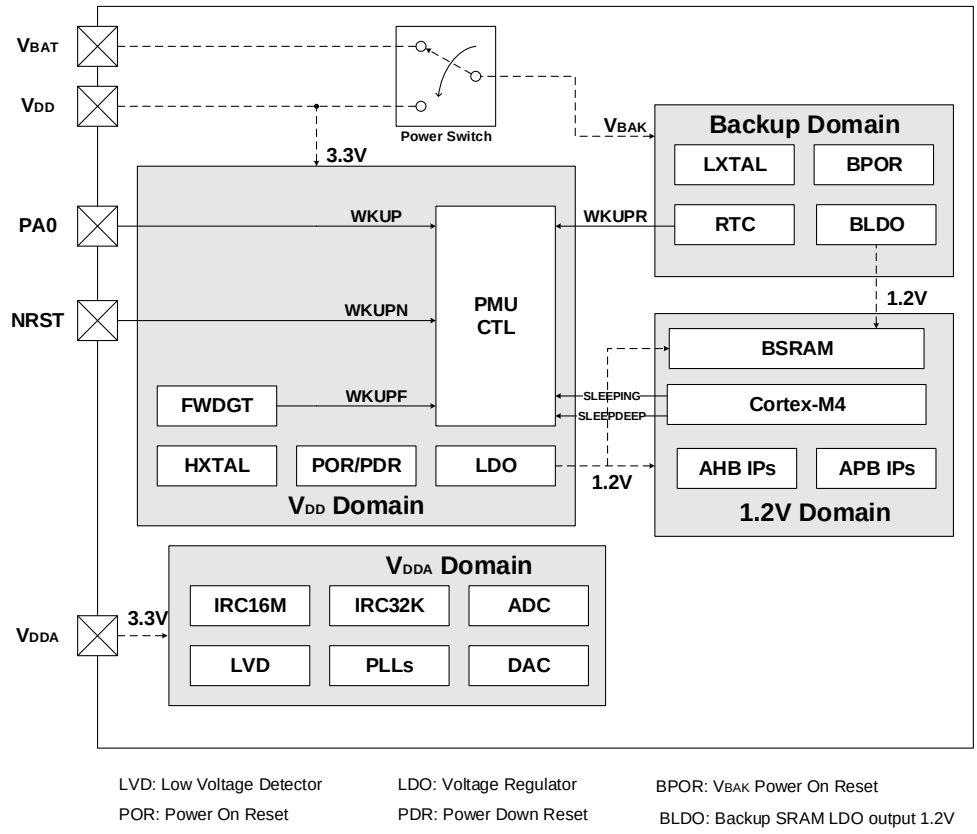
Type	Part Numbers
MCU	GD32F405xx series
	GD32F407xx series
	GD32F450xx series
	GD32F425xx series
	GD32F427xx series
	GD32F470xx series

2. Hardware design

2.1. Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32F4xx series products is 2.6 V ~ 3.6 V. For GD32F4xx series, there are three power domains, including V_{DD} / V_{DDA} domain, 1.2V domain, and Backup domain, as is shown in ***Figure 2-1. GD32F4xx Power supply overview***.The V_{DD}/V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.2 V domain. The backup domain power supply V_{BAK} can be powered by V_{DD} or V_{BAT} through the power switch Power Switch. When the V_{DD} power supply is turned off, the power switch can switch the power supply of the backup domain to the V_{BAT} pin. At this time, the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. GD32F4xx Power supply overview



LVD: Low Voltage Detector
LDO: Voltage Regulator
BPOR: V_{BAK} Power On Reset
POR: Power On Reset
PDR: Power Down Reset
BLDO: Backup SRAM LDO output 1.2V

2.1.1. Backup domain

The backup domain supply voltage range is 1.8V ~ 3.6V. The battery backup domain is powered by an internal power switch to select V_{DD} or V_{BAT} (battery) power, and then V_{BAK} powers the backup domain. In order to ensure the contents of the registers in the backup domain and the normal operation of the RTC, when V_{DD} is turned off, the V_{BAT} pin can be connected to a backup source such as a battery or other power supply. If there is no external battery-powered application, it is recommended to connect the V_{BAT} pin to the ground through

a 100nF capacitor and then connect it to the V_{DD} pin.

Note:

1、 During the V_{DD} power-on stage, the internal backup domain power supply of the chip is still connected to the V_{BAT} pin. If V_{DD}>V_{BAT}+0.6V at this time, the current may be injected into V_{BAT} through the internal diode between V_{DD} and V_{BAT}, causing V_{BAT} pulses.

2、 Regarding the power consumption of the V_{BAT} pin, theoretically, when the V_{DD} of the MCU is powered on, the swich inside the backup domain is connected to V_{DD}, and the V_{BAT} pin has no current. However, when the main program uses the ADC to measure the V_{BAT} voltage through the internal channel , due to the MCU design, the voltage on V_{BAT} will be divided by 4, and then enter the ADC channel, so it will cause additional power consumption on the V_{BAT} pin (tens of uA level).

2.1.2. V_{DD}/V_{DDA} domain

The V_{DD}/V_{DDA} power domain includes two parts: V_{DD} domain and V_{DDA} domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two should not exceed 300mV (the internal V_{DDA} and V_{DD} of the chip are connected through a back-to-back diode). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and the corresponding V_{SSA} is connected to V_{SS} through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. There is a V_{REF} pin (2.6 V ≤ V_{REFP} ≤ V_{DDA}, V_{REFN} = V_{SSA}) for ADC independent power supply on the large package.

- In the BGA package, the package chips with 100 pins and more contain V_{REFP} and V_{REFN}. V_{REFP} can use an external reference power supply, or can be directly connected to V_{DDA}, and V_{REFN} must be connected to V_{SSA}.
- In the LQFP package, the package chip with 100 pins and more contains V_{REFP}, and V_{REFP} can use an external reference power supply, or can be directly connected to V_{DDA}.
- The 64-pin package chip has no V_{REFP} and V_{REFN}, it is directly connected to V_{DDA} and V_{SSA} internally, and all analog modules are powered by V_{DDA} (including ADC/DAC)

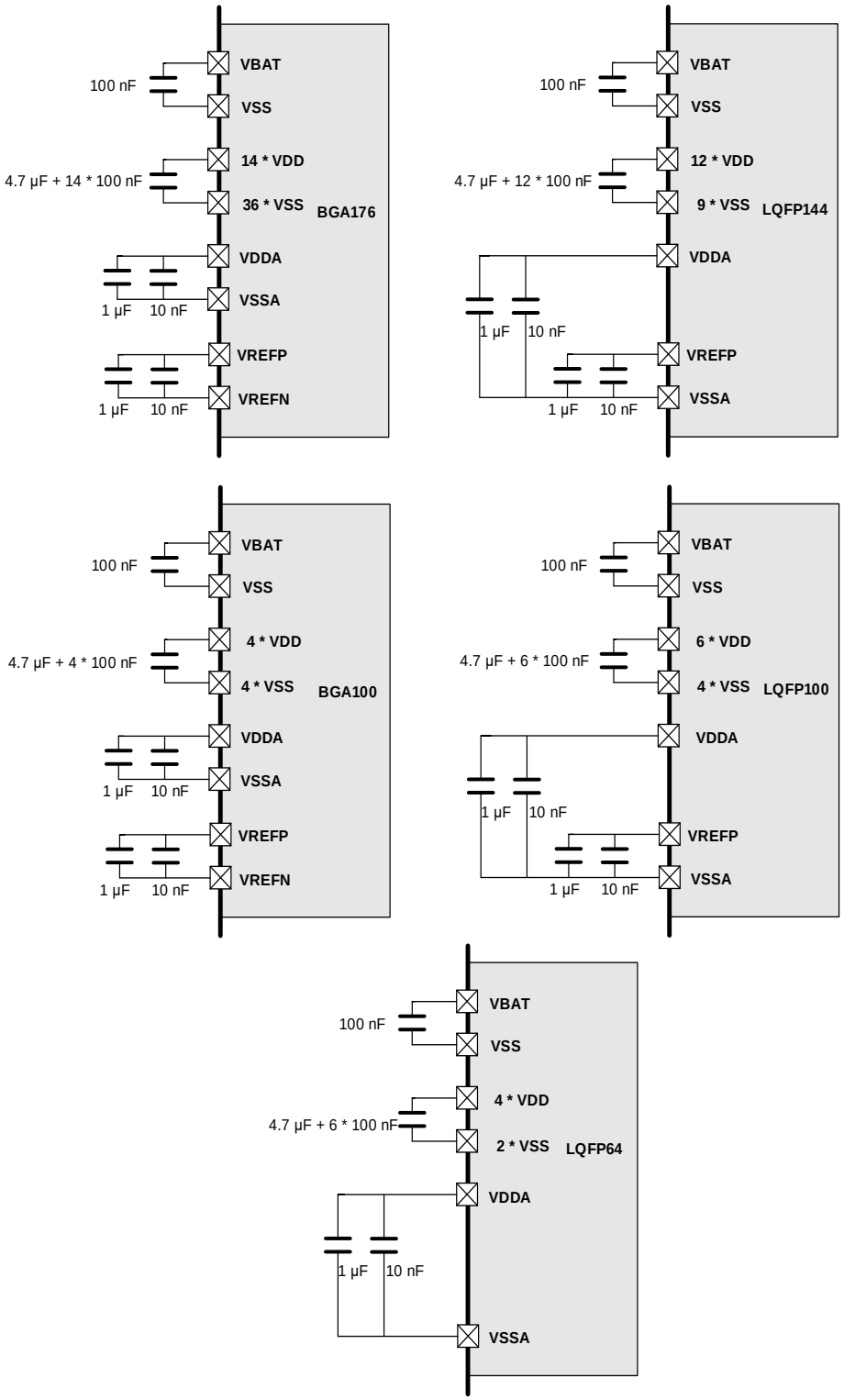
2.1.3. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF).
- The VDDA pin must be connected with an external capacitor (10nF+1uF ceramic capacitor is recommended).
- The VREF pin can be directly connected to VDDA, and a 10nF+1uF ceramic capacitor

should be connected between the VREF pin and ground.

Figure 2-2. GD32F4xx Recommended Power Supply Design



Note:

1. All decoupling capacitors must be placed close to the corresponding VDD, VDDA, VREF pins of the chip.

2. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
3. LQFP144: VREFN and VSSA are connected internally.
4. LQFP100: VREFN and VSSA are connected internally.
5. LQFP64: VREFN and VSSA are connected internally. VREFP and VDDA are connected internally.

2.2. Reset and power management

GD32F4xx series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain when the power is turned on. During the power and system reset process, NRST will maintain a low level until the reset is over. When the MCU cannot be executed, the NRST pin waveform can be monitored by an oscilloscope to determine whether the chip has been reset.

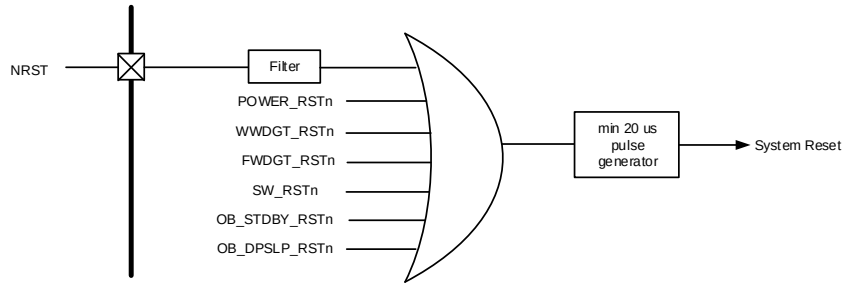
In addition, the MCU reset source can be searched by the register RCU_RSTSCK (0x40023874). This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register:

Figure 2-3. RCU_RSTSCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LP RSTF	WWDGTR STF	FWDGT RSTF	SW RSTF	POR RSTF	EP RSTF	BOR RSTF	RSTFC	Reserved							
r	r	r	r	r	r	r	rw								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														IRC32K STB	IRC32KEN
														r	rw

MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20μs.

Figure 2-4. System Reset Circuit



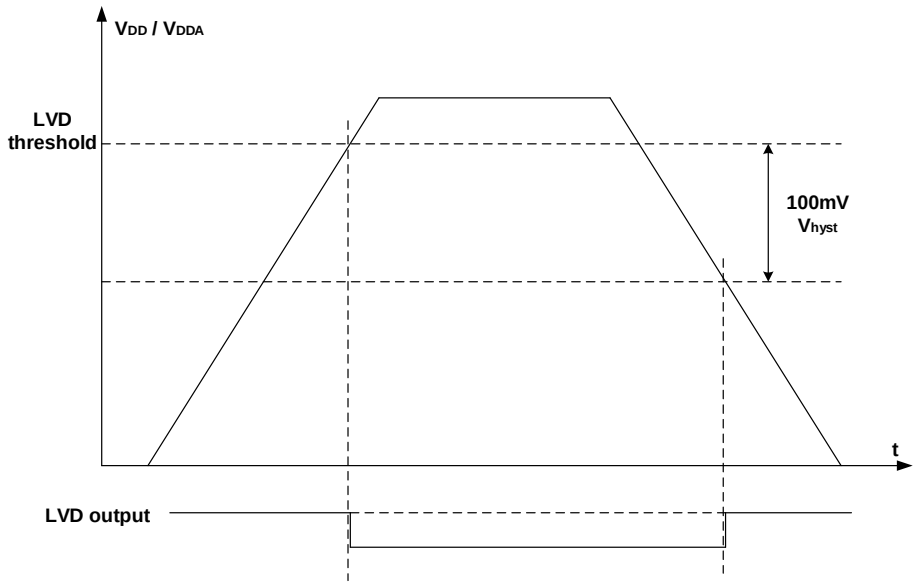
2.2.1. LVD

The function of LVD is to detect whether the VDD/VDDA supply voltage is lower than the low

voltage detection threshold (2.1 V ~ 3.1 V), which is configured by the LVDT[2:0] bits in the power control register (PMU_CTL). LVD is enabled by setting the LVDEN bit. The LVDF bit located in the power status register (PMU_CS) indicates whether VDD/VDDA is higher or lower than the LVD threshold voltage event. This event is connected to the 16th line of EXTI. The user can configure EXTI by Line 16 generates a corresponding interrupt. ***Figure 2-5. LVD Threshold Waveform*** shows the relationship between the VDD/VDDA supply voltage and the LVD output signal. (LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16). The value of the hysteresis voltage Vhyst is 100mV.

LVD application: When the MCU power supply is subject to external interference, such as a voltage drop, we can set the low voltage detection threshold (the threshold is greater than the PDR value) through LVD. Once it falls to the threshold, the LVD interrupt is turned on, which can be used in the interrupt function. Set operations such as soft reset to avoid other exceptions from the MCU.

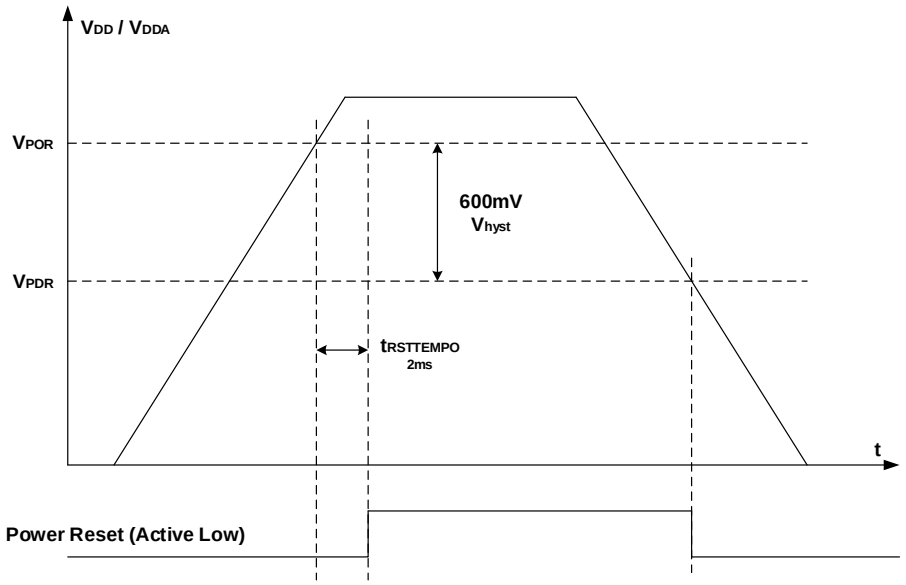
Figure 2-5. LVD Threshold Waveform



2.2.2. POR/PDR

The chip integrates a POR/PDR (power-on/power-down reset) circuit to detect VDD/VDDA and generate a power reset signal to reset the entire chip except the backup domain when the voltage is lower than a certain threshold. VPOR is the threshold voltage of power-on reset, and the typical value is about 2.4 V, and VPDR is the threshold voltage of power-down reset, and the typical value is about 1.8 V. The value of the hysteresis voltage Vhyst is about 600mV.

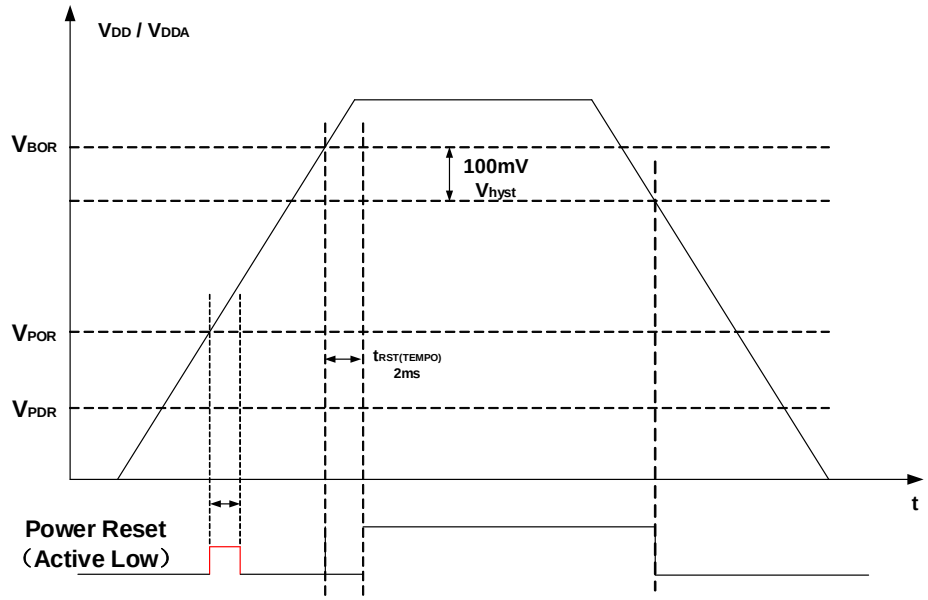
Figure 2-6. Power-on/power-down reset waveforms



2.2.3. BOR

The GD32F4xx series MCU also integrates a BOR circuit. The BOR circuit detects VDD/VDDA and generates a power reset signal to reset the entire chip except the backup domain when the voltage is lower than the threshold defined by BOR_TH of the option byte and the threshold is not 0b11 (default state: BOR_TH=0b11, BOR function is off). Regardless of whether the option byte BOR_TH has a value of 0b11, the POR/PDR (power-on/power-down reset) circuit will always be in the detection state.***Figure 2-7. BOR Threshold Waveform*** shows the relationship between the supply voltage and the BOR reset signal. VBOR represents the BOR reset threshold voltage, which is defined in the option byte BOR_TH. The value of the hysteresis voltage Vhyst is 100mV.

Figure 2-7. BOR Threshold Waveform



The BOR threshold is set through the option byte BOR_TH, and can set three different levels. Refer to the following table for the corresponding relationship:

Table 2-1. VBOR Threshold Voltage Setting

Symbol	Conditions	Typ
BOR_TH=00(BOR level3)	Falling edge	2.79 V
	Rising edge	2.88 V
BOR_TH=01(BOR level2)	Falling edge	2.49 V
	Rising edge	2.58 V
BOR_TH=10(BOR level1)	Falling edge	2.19 V
	Rising edge	2.29 V
BOR_TH=11(BOR off)	-	-

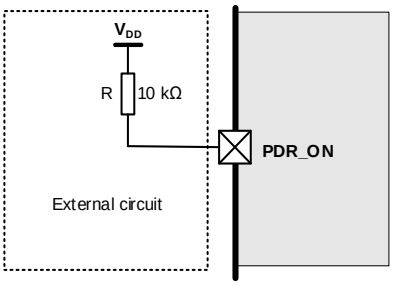
Regardless of whether BOR is enabled, the POR/PDR (Power-On/Power-Down Reset) circuit will always be in a detection state. Therefore, when VDD/VDDA rises to the threshold of POR, the level of NRST pin will be pulled high. Then if BOR is enabled this time, it will quickly pull down the NRST pin until VDD/VDDA rises to the threshold of BOR set by the option byte BOR_TH, at which point the level of NRST pin will be pulled high again.

In other words, when BOR is enabled, during the ramp-up phase of VDD/VDDA, the voltage on the NRST pin will experience a pulse when VDD/VDDA reaches the threshold of POR. This pulse lasts for a few milliseconds (the duration varies with different MCUs). This pulse does not affect the normal operation of the chip, as illustrated by the red pulse in the BOR threshold waveform shown in ***Figure 2-7. BOR Threshold Waveform.***

For the LQFP package, there is a PDR_ON pin on the 144pin and larger packages. For the BGA package, there is a PDR_ON pin on the BGA100 and larger packages. This pin enables the POR/PDR circuit inside the chip to ensure that the chip is with valid POR and PDR occurring during the power-up and power-down phase, this pin should pull up to VDD through

a resistor, as shown in the figure below.The user can flexibly adjust the value of the pull-up resistor R according to the specific scenario for a better performance.

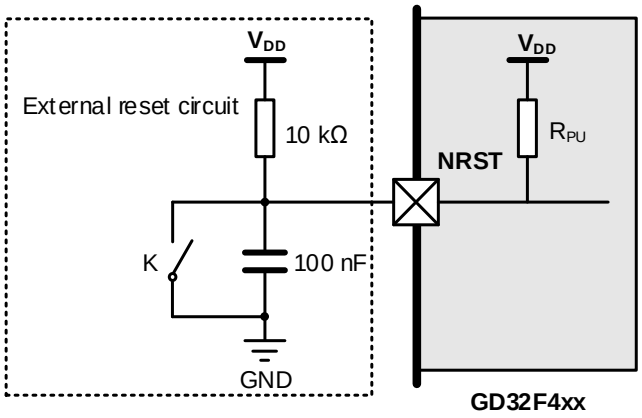
Figure 2-8. Recommend PDR_ON Pin Circuit Design



2.2.4. NRST PIN

MCU integrates a power-up/power-down reset circuit. When designing an external reset circuit, a capacitor (typical value of 100nF) is suggested to be placed on the NRST pin to Avoid false triggering.

Figure 2-9. Recommend External Reset Circuit



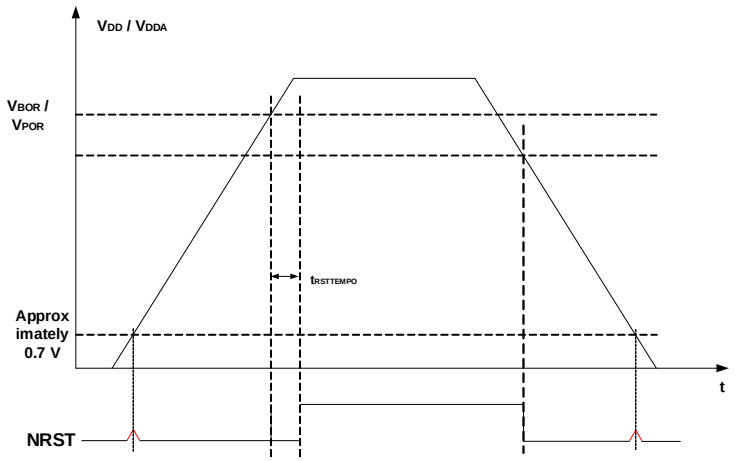
Note:

1. The pull-up resistor is recommended to be 10kΩ, so that voltage interference will not cause the chip to work abnormally.
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

Due to the threshold voltage characteristics of the MOS transistor, during the power-up and

power-down process of the chip, when VDD / VDDA < 0.7 V, the internal pull-down MOS transistor of the chip will not pull down the NRST pin. Therefore, during the power-up and power-down process, when VDD / VDDA ≈ 0.7 V, a small pulse occurs, which does not affect the normal operation of the chip, as shown by the red pulse in ***Figure 2-10. The illustration of the pulse of the NRST pin power-up/down MOS transistor.***

Figure 2-10. The illustration of the pulse of the NRST pin power-up/down MOS transistor

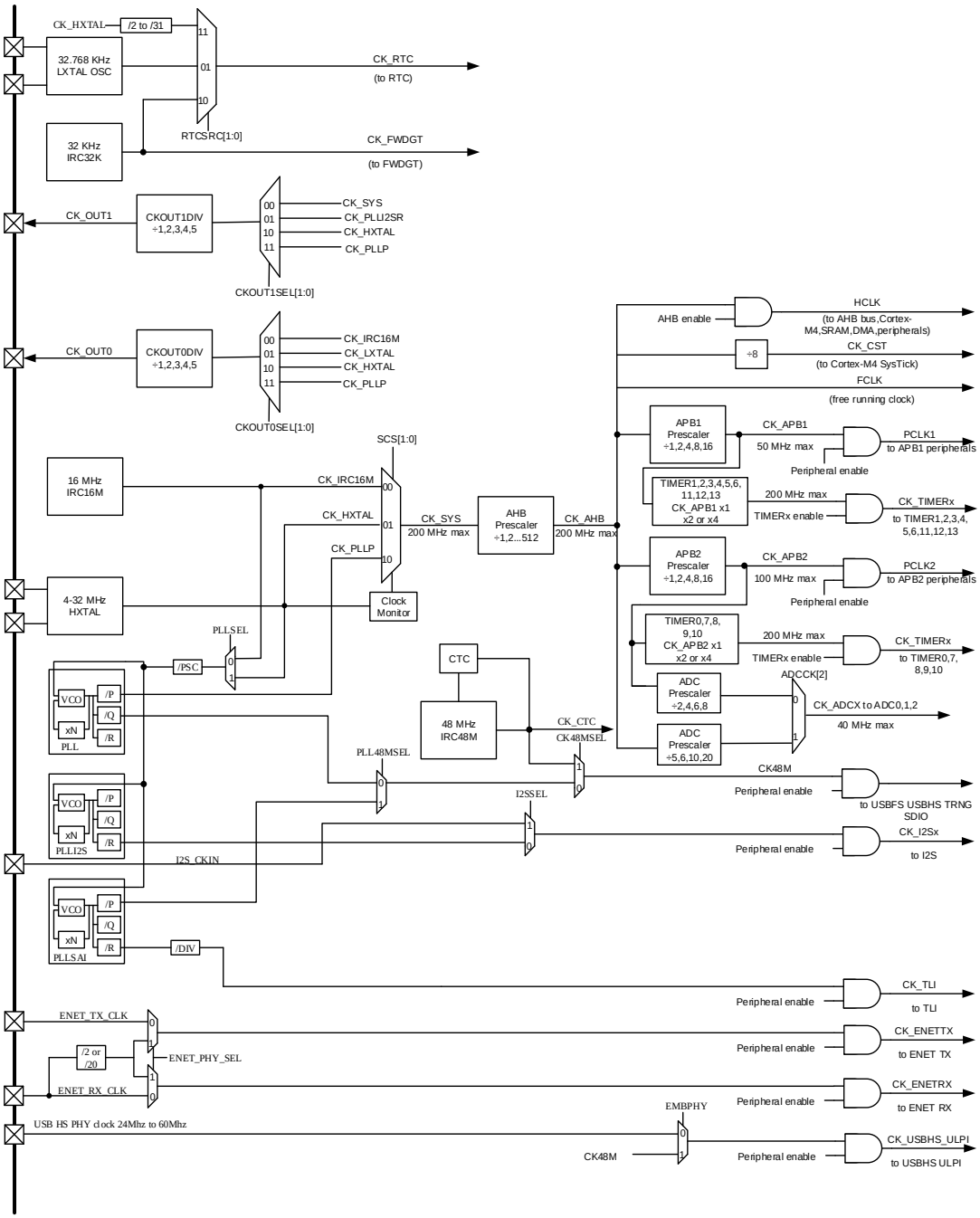


2.3. Clock

GD32F4xx series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

- 4-32 MHz external high-speed crystal oscillator (HXTAL)
- Internal 16 MHz RC oscillator (IRC16M)
- Internal 48 MHz RC oscillator (IRC48M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- Internal 32 kHz RC oscillator (IRC32K)
- PLL clock source can be selected from HXTAL or IRC16M
- HXTAL clock monitor

Figure 2-11. Clock Tree



Note: The highest frequency of GD32F405xx/ GD32F407xx series MCU is 168MHz. The highest frequency of GD32F425xx/ GD32F427xx/ GD32F450xx series MCU is 200MHz. The highest frequency of GD32F470xx series MCU is 240MHz.

2.3.1. External high-speed crystal oscillator clock (HXTAL)

4-32MHz external high-speed crystal oscillator (passive crystal) can provide accurate main clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input

mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSC_IN, and OSC_OUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-12. HXTAL External Crystal Circuit

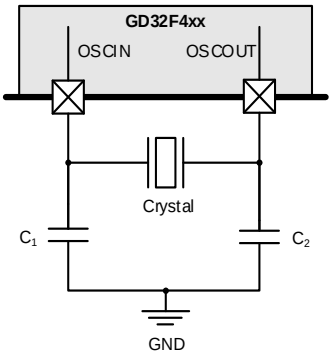
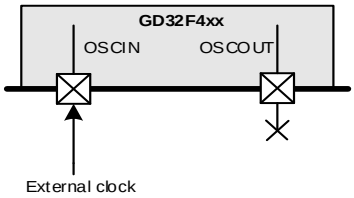


Figure 2-13. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC16M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}.
7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSC_OUT and OSC_IN pins due to the space

constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768 kHz low-speed external crystal (passive crystal), which can provide a low-power and high-precision clock source for RTC. The RTC module of the MCU is equivalent to a counter. The accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-14. LXTAL External Crystal Circuit

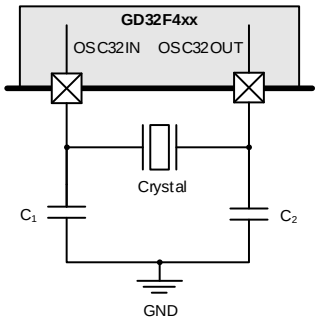
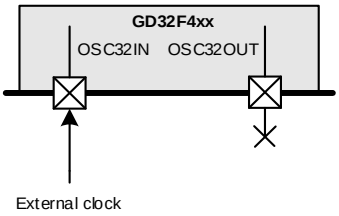


Figure 2-15. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32_IN, and OSC32_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.

3. When the RTC selects IRC32K as the clock source and uses V_{BAT} for external independent power supply, if the MCU is powered off at this time, the RTC will stop counting. After re-powering, the RTC will continue to count up with the previous count value. If the application needs to use V_{BAT} to power the RTC, the RTC can still time normally, and the RTC must select LXTAL as the clock source.
4. The MCU can set the drive capability of LXTAL. If it is found that the external low-speed crystal is difficult to vibrate during the actual debugging process, you can try to adjust the drive capability of LXTAL to high drive capability.
5. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the two crystal pins of the MCU due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.3. Clock Output Capability (CKOUT)

GD32F4xx series MCUs can output clocks from 32kHz to 200MHz. Different clock signals can be selected by setting the CK_OUT0 clock source selection bit field CKOUT0SEL in the clock configuration register 0 (RCU_CFG0). The CK_OUT1 clock output source selection is realized by setting the CKOUT1SEL bit field in the clock configuration register RCU_CFG0. The corresponding GPIO pins should be configured in Alternate Function I/O (AFIO) mode to output the selected clock signal. The IO port corresponding to CK_OUT0 is PA8, and the IO port corresponding to CK_OUT1 is PC9.

Table 2-2. CKOUT0SEL[1:0] Control Bits

CKOUT0SEL[1:0]	Clock Source
00	CK_IRC16M
01	CK_LXTAL
10	CK_HXTAL
11	CK_PLLP

Table 2-3. CKOUT1SEL[1:0] Control Bits

CKOUT1SEL[1:0]	Clock Source
00	CK_SYS
01	CK_PLLI2SR
10	CK_HXTAL
11	CK_PLLP

2.3.4. HXTAL Clock Monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the control register RCU_CTL, HXTAL can enable the clock monitoring function. This function must be enabled after the HXTAL start-up delay has elapsed and disabled after the HXTAL has been stopped. Once the HXTAL fault

is detected, the HXTAL will be automatically disabled, and the HXTAL clock blocking interrupt flag bit CKMIF in the interrupt register RCU_INT will be set to '1' to generate an HXTAL fault event. The interrupt caused by this fault is connected to the non-maskable interrupt NMI of the Cortex®-M4. If HXTAL is selected as the system or PLL clock source, HXTAL failure will cause the IRC16M to be selected as the system clock source and the PLL will be automatically disabled.

Note: If HXTAL is selected as the system or PLL clock source, HXTAL failure will cause the IRC16M to be selected as the system clock source and the PLL will be automatically disabled. The clock source of the RTC needs to be reconfigured.

2.3.5. PLL Spread Spectrum (SSCG)

In order to reduce EMI interference, the GD32F4xx PLL integrates the clock spread spectrum function (only applicable to the main PLL), which effectively reduces the energy of the main clock frequency and its odd harmonics. According to the set modulation frequency f_{mod} and modulation peak mdamp (Refer to ***Table 2-4. PLL spread spectrum clock generation (SSCG) characteristics***).

Calculate MODCNT and MODSTEP by formula 2-1 and formula 2-2, and fill in the PLL clock spread spectrum control register (RCU_PLLSSCTL). Note that the product of MODCNT and MODSTEP cannot be greater than 2^15-1. If it is greater than that, it is necessary to reduce the modulation peak mdamp and recalculate it.

Table 2-4. PLL spread spectrum clock generation (SSCG) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{mod}	Modulation frequency	—	—	—	10	kHz
mdamp	Peak modulation amplitude	—	—	—	2	%
MODCNT* MODSTEP	—	—	—	—	2^{15}-1	—

MODCNT and MODSTEP are obtained by the following formula:

$$MODCNT=round(f_{PLLIN}/4/f_{mod}) \quad (2\text{-}1)$$

$$MODSTEP = round(mdamp*PLLN*2^{14}/(MODCNT*100)) \quad (2\text{-}2)$$

f_{PLLIN} is the PLL input clock frequency, f_{mod} is the spread spectrum modulation frequency, mdamp is the spread spectrum modulation amplitude (expressed as a percentage), and PLLN is the PLL clock frequency multiplication factor.

For example, PLL reference clock source HXTAL = 8MHz, prescaler PLLM = 4, then f_{PLLIN} = 2MHz, set PLLN = 200 (at this time, the VCO frequency is 400MHz, and the system clock is 200MHz by dividing by two), the spread spectrum modulation frequency is 10kHz, and the modulation amplitude is 2 %, then MODCNT = 50 and MODSTEP = 1311 are calculated. At this time, MODCNT * MODSTEP> 2^15 - 1, which cannot be achieved. Reduce the modulation amplitude to 1%, then MODCNT=50, MODSTEP=655, at this time MODCNT * MODSTEP = 32750 < 2^15 - 1 meets the requirements.

According to the setting of SS_TYPE in the register RCU_PLLSSCTL, two types of spread

spectrum modulation can be selected, namely center spread spectrum and downward spread spectrum, and the PLL output frequency will change as the following waveform.

Figure 2-16. Center Spread Spectrum

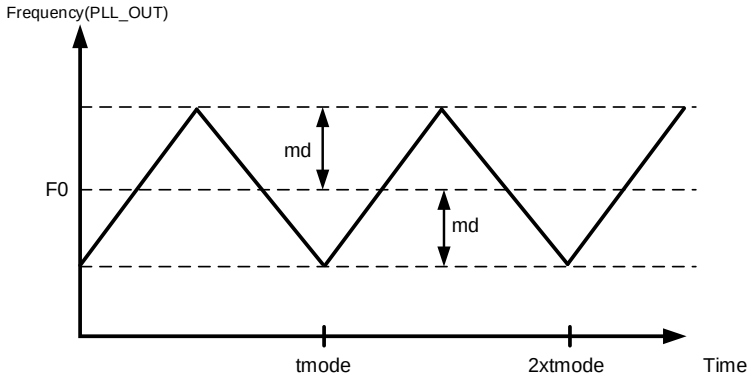
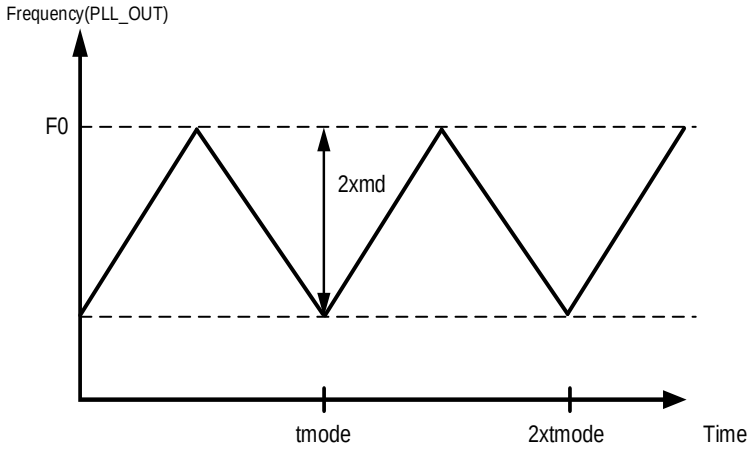


Figure 2-17. Down Spread Spectrum



Note: If the PLL spread spectrum function is enabled, the system clock frequency will fluctuate, and peripherals that require high clock accuracy may not work properly, such as Ethernet applications that use the MCU IO output clock as the PHY clock and USB related applications.

2.4. Startup Configuration

The GD32F4xx series provides three boot modes, which can be selected by the BOOT0 bit and the BOOT1 pin to determine the boot option. When designing the circuit, run the user program, the BOOT0 pin cannot be left floating, it is recommended to connect a 10kΩ resistor to GND; when running the System Memory to update the program, you need to connect the BOOT0 pin to high and the BOOT1 pin to low. After the update is completed, the user program can be run after the BOOT0 is connected to a low level; the SRAM execution program is mostly used in the debugging status.

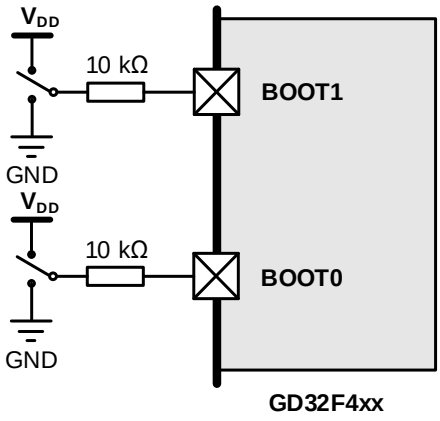
The embedded Bootloader is stored in the system storage space for reprogramming the

FLASH memory. Bootloader can interact with the outside world through USART0 (PA9 and PA10), USART2 (PB10 and PB11 or PC10 and PC11) or USB FS (PA9, PA11 and PA12).

Table 2-5. BOOT mode

BOOT mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-18. Recommend BOOT Circuit Design



Note:

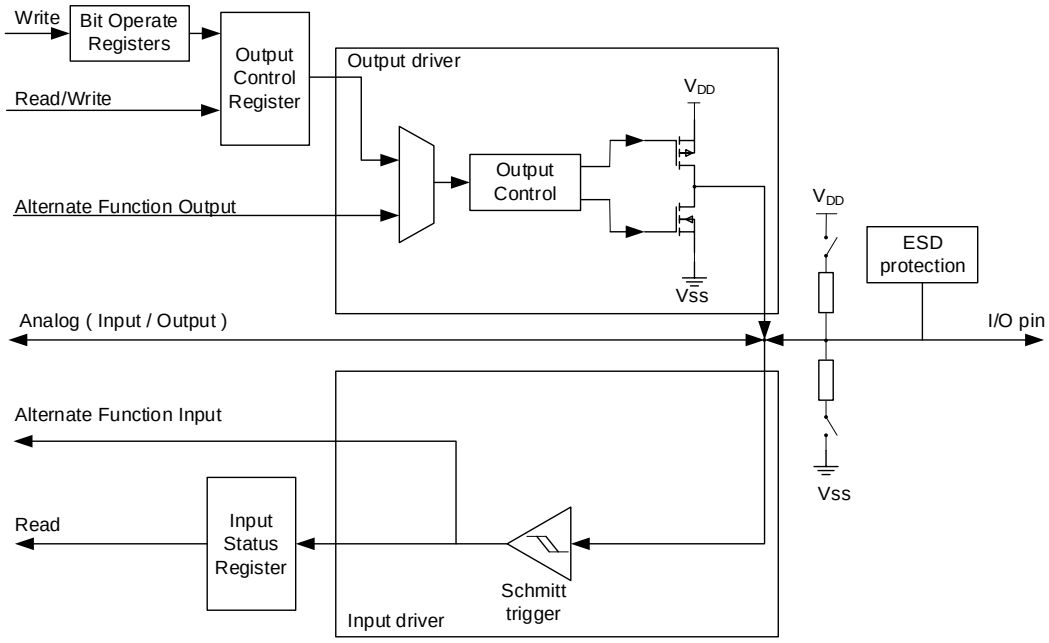
1. After the MCU is running, if the BOOT state is changed, it will take effect after the system is reset. MCU.
2. Once the BOOT1 pin state is sampled, it can be released for other purposes.

2.5. Typical Peripheral Modules

2.5.1. GPIO Circuit

GD32F4xx can support up to 140 general-purpose I/O pins (GPIO), which are PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH15, PI0 ~ PI11; each pin can be independently configured through registers, the basic structure of the GPIO port is shown in the following figure:

Figure 2-19. Basic structure of standard IO



Note:

1. The IO port is divided into 5V tolerant and non-5V tolerant. When using, pay attention to distinguish the IO port withstand voltage. For the GD32F4xx chip, except PA4 and PA5, the two pins are non-5V tolerant pins, and the other pins are 5V tolerant.
2. When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.
3. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
4. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
5. The four IO ports of PC13, PC14, PC15 and PI8 have weak drive capability and limited output current capability. When configured in output mode, their working speed cannot exceed 2MHz.
6. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.

2.5.2. ADC Circuit

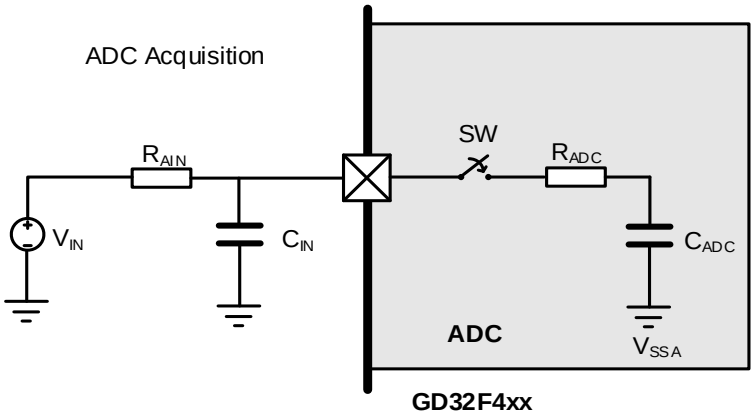
The GD32F4xx integrates a 12-bit SAR ADC with up to 19 channels, which can measure 16 external and 2 internal signal sources and 1 external battery monitoring signal source. The internal signal is the temperature sensor channel (ADC0_CH16), the internal reference voltage input channel (ADC0_CH17), and the external signal is the external monitoring battery

V_{BAT} power supply pin input channel (ADC0_CH18). The temperature sensor reflects the change in temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a regulated voltage output (1.2V) to the ADC and is internally connected to ADC0_C17. Provides the function of externally detecting the battery voltage of the V_{BAT} pin, and the converted value is $V_{BAT}/4$.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin. It is recommended to place a small capacitor of 500pF.

Figure 2-20. ADC Acquisition Circuit Design



When f_{ADC} = 40MHz, the relationship between the input impedance and the sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, and select a larger value for the sampling period. When designing external circuits, try to reduce the input Impedance, if necessary, use the op amp to follow to reduce the input impedance.

Table 2-6. f_{ADC} =40MHz Relationship between sampling period and external input impedance (applicable to GD32F405xx/ GD32F407xx/ GD32F450xx series MCU)

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (kΩ)
3	0.075	0.85
15	0.375	6.5
28	0.7	12.6
55	1.375	25.7
84	2.1	38.8
112	2.8	51.9
144	3.6	N/A
480	12	N/A

Table 2-7. f_{ADC} =40MHz Relationship between sampling period and external input

impedance (applicable to GD32F425xx/ GD32F427xx/ GD32F470xx series MCU)

T_S (cycles)	t_S (us)	$R_{AIN\ max}$ (KΩ)
3	0.075	1.3
15	0.375	9.1
28	0.7	17.4
55	1.375	34.8
84	2.1	53.5
112	2.8	71.5
144	3.6	92.4
480	12	308.6

2.5.3. DAC Circuit

The digital/analog converter of GD32F4xx series MCU can convert 12-bit digital data to voltage output on external pins. Data can be in 8-bit or 12-bit mode, left-justified or right-justified. When external triggering is enabled, DMA can be used to update digital data on the input. At the output voltage, higher drive capability can be obtained by enabling the DAC output buffer. The two DACs can work independently or concurrently.

Table 2-8. DAC Related Pin Description

Name	Description	Signal type
V_{DDA}	Analog power	Input, Analog power
V_{SSA}	Analog power ground	Input, Analog power ground
V_{REFP}	DAC positive reference voltage, $2.6V \le V_{REFP} \le V_{DDA}$	Input, Analog positive reference voltage
DAC_OUTx	DACx analog output	Analog output signal

Before enabling the DAC module, the GPIO port (PA4 corresponds to DAC0, PA5 corresponds to DAC1) should be configured in analog mode.

2.5.4. USB Circuit

GD32F4xx series MCU has two USB interfaces, one is USBFS interface and the other is USBHS interface. USBFS includes an internal full-speed USB PHY and eliminates the need for an external PHY chip. USBHS provides a ULPI interface for the external USB physical layer (PHY), and it also includes an internal full-speed USB PHY. Therefore, for full-speed operation, an external USB PHY is no longer required; if an external high-speed ULPI PHY is used, the maximum speed supported by USBHS is high-speed.

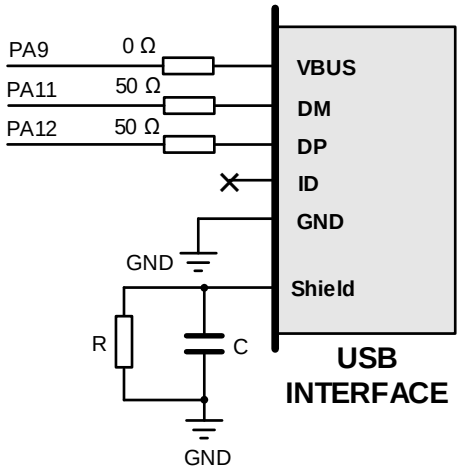
The USB protocol requires a clock accuracy of not less than 500ppm, and the internal clock may not be able to achieve such accuracy, so it is recommended to use an external crystal or an active crystal oscillator as the USB module clock source when using the USB function.

GD32F4xx series USB can be designed as both USB device and USB host. When designed as Device, if the VBUSIG control bit in the USBFS_GCCFG register has been configured to

1, there is no need to connect PA9 with V_{BUS}. If the VBUSIG control bit in the USBFS_GCCFG register has been configured to 0, PA9 must be connected to VBUS.

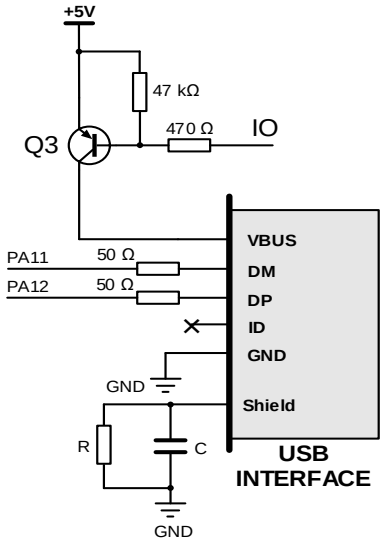
When designing the circuit, in order to improve the ESD performance of the USB, it is recommended to design a resistance-capacitance discharge isolation circuit for the USB case.

Figure 2-21. Recommend USB-Device Reference Circuit



Recommendation: R = 1MΩ, C = 4700pF

Figure 2-22. Recommend USB-Host Reference Circuit



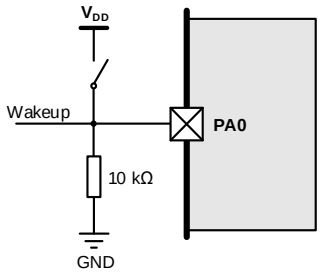
Recommendation: R = 1MΩ, C = 4700pF

2.5.5. Standby mode wake-up circuit

The GD32F4xx series supports three low-power modes, namely sleep mode, deep-sleep mode and standby mode. The standby mode with the lowest power consumption is the standby mode, which requires the longest wake-up time. Wake-up from Standby mode can be woken up by the rising edge of the WKUP pin. At this time, there is no need to configure the corresponding GPIO, just configure the WUPEN bit in the PMU_CS register. The

reference circuit design corresponding to the WKUP wake-up pin is as follows:

Figure 2-23. Recommend Standby external wake-up pin circuit design



Note: In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.

2.6. Download the debug circuit

GD32F4xx series cores support JTAG debug interface and SWD debug interface. The JTAG interface standard is a 20-pin interface, including 5 signal interfaces, and the SWD interface standard is a 5-pin interface, including 2 signal interfaces.

Note: After reset, the debug related ports are in input PU/PD mode, where:
PA15: JTDI is in pull-up mode.
PA14: JTCK/SWCLK in pull-down mode.
PA13: JTMS/SWDIO in pull-up mode.
PB4: NJTRST is in pull-up mode.
PB3: JTDO is floating mode.

Table 2-9. JTAG download debug interface assignment

Alternate function	GPIO port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-24. Recommend JTAG Wiring Reference Design

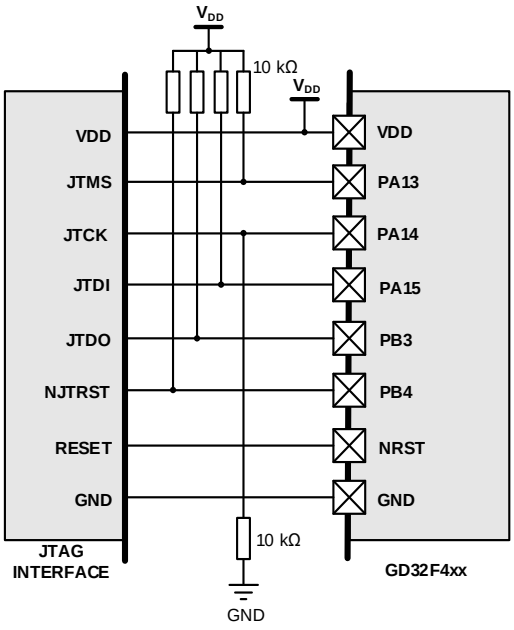
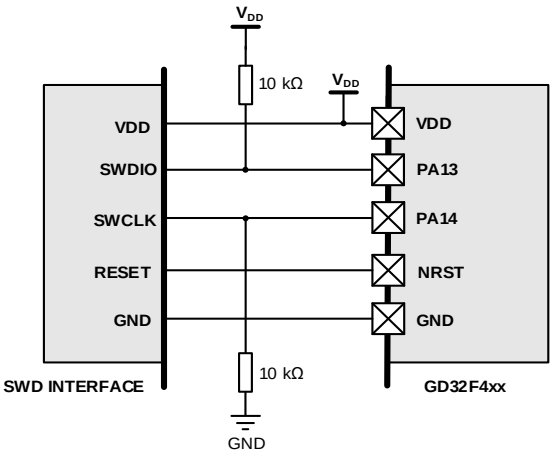


Table 2-10. SWD Download Debug Interface Assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-25. Recommend SWD Wiring Reference Design

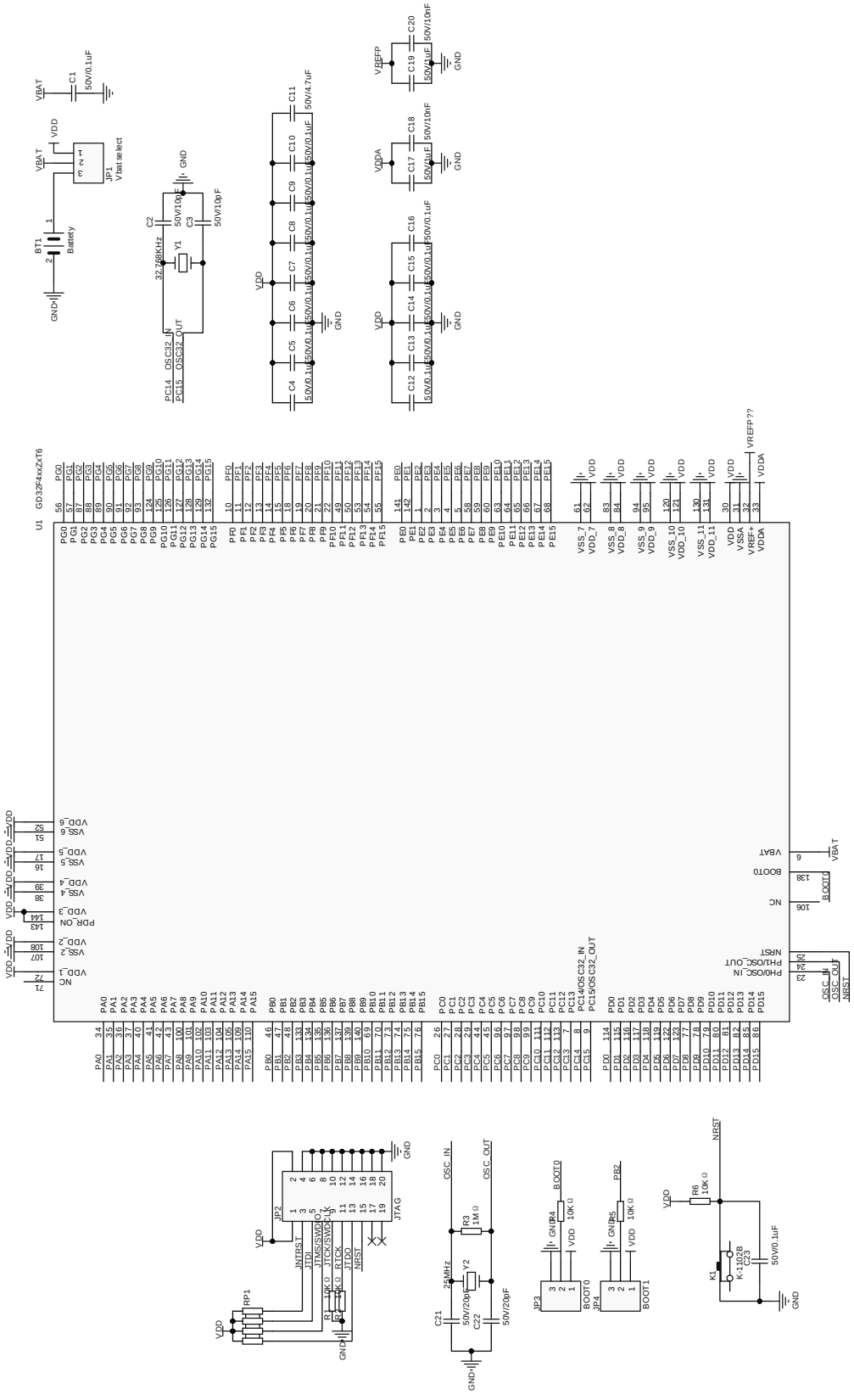


There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω~1kΩ resistor.

2.7. Reference Schematic Design

Figure 2-26. GD32F4xx Recommend Reference Schematic Design



3. PCB Layout Design

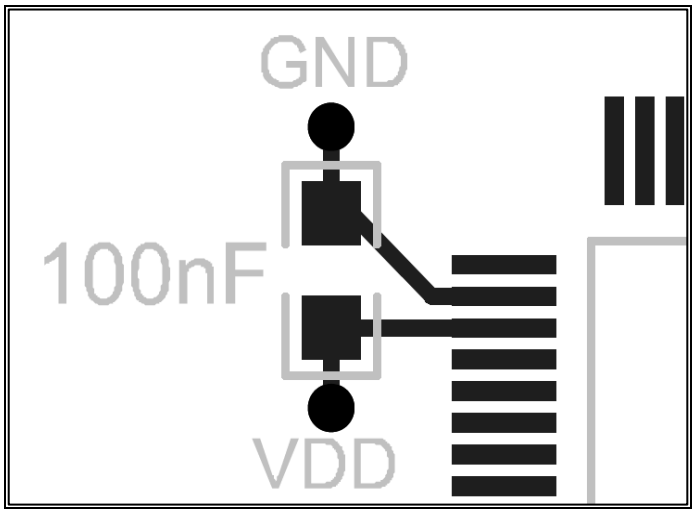
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32F4xx series power supply has three power supply pins: V_{DD}, V_{DDA} and V_{BAT}. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended to punch holes near the capacitor pad to connect with GND.

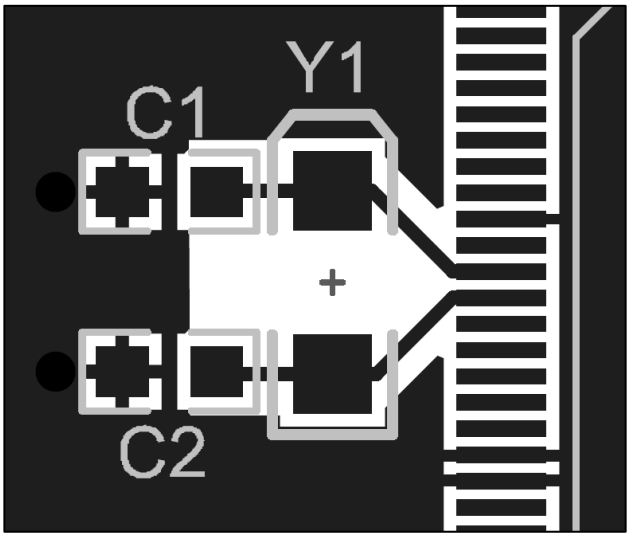
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32F4xx series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



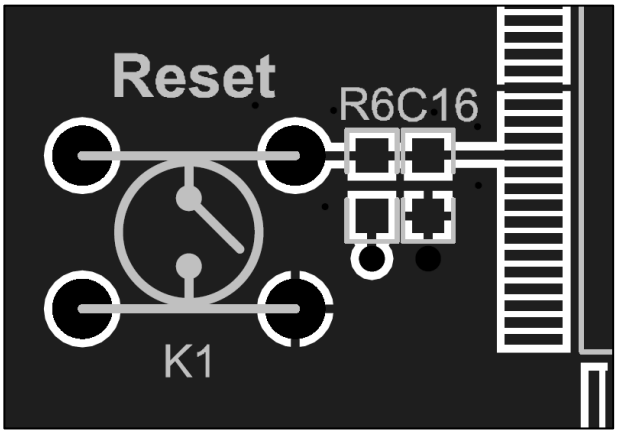
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design



Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better

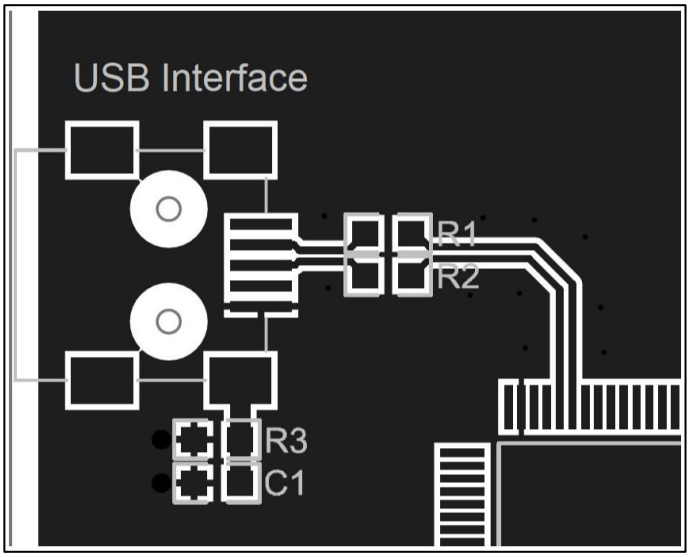
to wrap the NRST traces for better shielding effect.

3.4. USB Circuit

For the GD32F4xx MCU USB FS module, there are two differential signal lines, DM and DP. For the USB HS module, after connecting the external high-speed PHY, the PHY chip will also lead out two differential signal lines, DM and DP. It is recommended that the PCB traces require a characteristic impedance of 90ohm. , the differential traces are strictly in accordance with the rule of equal length and equal distance, and try to keep the traces as short as possible. If the two differential traces are not equal in length, use a serpentine wire at the terminal to compensate for the short trace. Due to impedance matching considerations, the series matching resistance is recommended to be about 50Ω.

The reference of DM and DP differential trace is as follows:

Figure 3-4. Recommend DM, DP Differential Trace Layout Design



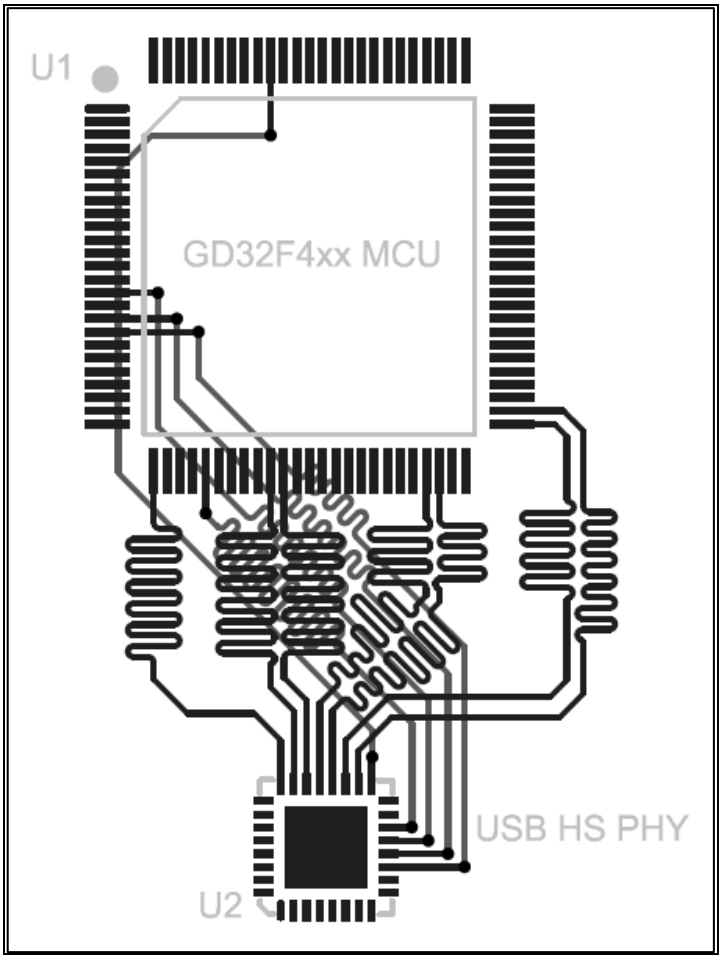
Recommendation: R1 = R2 = 50Ω, R3 = 1MΩ, C = 4700pF

Note:

1. Reasonable placement during layout to shorten the differential trace distance.
2. Draw differential lines first, try not to exceed two pairs of vias for a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring to ensure that the two lines are tightly coupled, avoiding 90°, arc or 45° wiring.
4. Devices such as resistance-capacitor, EMC connected to the differential traces, or test points should also be symmetrical.

For the USB HS module, the data line and signal control line between the MCU and the external HS PHY should be kept as short as possible, and a serpentine line should be used for equal-length processing. The reference is as follows:

Figure 3-5. Recommend MCU and PHY Layout Design



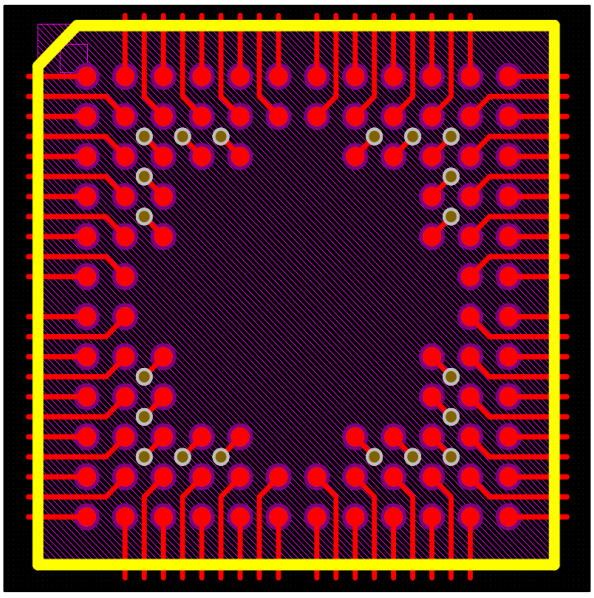
Note:

1. Only the connection between MCU and USB HS-PHY is drawn in the figure, other circuits are not drawn.
2. The layout should be placed reasonably, and the space between the USB HS-PHY chip and the MCU should be as compact as possible.
3. When wiring, take the longest one of the signal lines as the target, and compensate the other signal lines through the serpentine trace.

3.5. Fan-Out of BGA Package

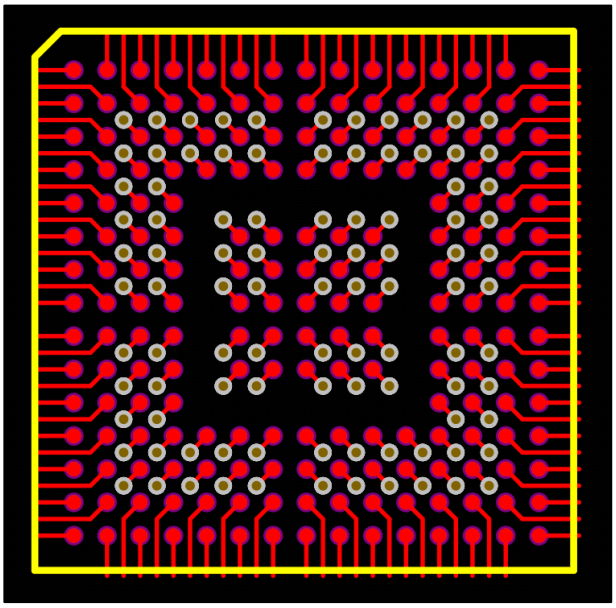
For some models of GD32F4xx series MCU, there are BGA176 (0.65mm Pitch) package and BGA100 (0.5mm Pitch) package, we recommend the following routing rules and fan-out methods.

Figure 3-6. Fan-Out Method of BGA100 Package



For the BGA package with 0.5 mm pitch, if the BGA pad size is set to 0.25/0.35, and the via-to-pad and line-width-to-line spacing is 3 mil, the dog bone type fan-out can be used. After the fan-out is shown in ***Figure 3-6. Fan-Out Method of BGA100 Package***. The distance between the via and the pad is 4.5mil; however, this kind of wiring has high requirements on the PCB manufacturer's process, and it is necessary to communicate with the PCB manufacturer before wiring. If the manufacturer's process does not meet the requirements, the BGA package can be plated Medium vias and blind buried vias.

Figure 3-7. Fan-Out Method of BGA176 Package



For the BGA package with 0.65 mm pitch, it is recommended to set 4 mil line width and line spacing, and use 8/12 mil (if the overcurrent is large, 8/13 mil can also be used, larger than 8/13 mil size, 4 mil line width line distance from the out-of-line) vias for fan-out, after the fan-out is shown in ***Figure 3-7. Fan-Out Method of BGA176 Package***. The via-to-pad distance is 6.2mil.

4. Package Description

GD32F405xx/ GD32F425xx series has a total of 4 package types, namely LQFP64, LQFP100, BGA100 and LQFP144.

GD32F407xx/ GD32F427xx series has 5 packages: LQFP64, LQFP100, BGA100, LQFP144 and BGA176.

GD32F450xx series has a total of 3 package types, namely LQFP100, LQFP144 and BGA176.

GD32F470xx series has a total of 4 package types, namely LQFP100, LQFP144, BGA100 and BGA176.

Table 4-1. Package Description

Ordering code	Package
GD32F40xRxT6	LQFP64(10x10, 0.5pitch)
GD32F42xRxT6	LQFP64(10x10, 0.5pitch)
GD32F40xVxT6	LQFP100(14x14, 0.5pitch)
GD32F42xVxT6	LQFP100(14x14, 0.5pitch)
GD32F40xVxH6	BGA100(7x7, 0.5pitch)
GD32F42xVxH6	BGA100(7x7, 0.5pitch)
GD32F40xZxT6	LQFP144(20x20, 0.5pitch)
GD32F42xZxT6	LQFP144(20x20, 0.5pitch)
GD32F407IxH6	BGA176(10x10, 0.65pitch)
GD32F427IxH6	BGA176(10x10, 0.65pitch)
GD32F4x0VxT6	LQFP100(14x14, 0.5pitch)
GD32F4x0ZxT6	LQFP144(20x20, 0.5pitch)
GD32F4x0IxH6	BGA176(10x10, 0.65pitch)
GD32F470VxH6	BGA100(7x7, 0.5pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.20, 2022
1.1	1.Update section 2.1.3 to provide all package power supply design drawings and connection of revelant pins within the chip 2.Update section 2.5.4 to give more details of the connection of PA9 and V_{BUS} under revelant registor configuration	Jun.21, 2023
1.2	1.Update section 2.1.3 to correct the content of VREFP pin 2.Refine the content related to power detection and reset, adding Section 2.2.	Dec.15,2024

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