GigaDevice Semiconductor Inc.

Device limitations of GD32F45x/F40x

Errata Sheet

Table of Contents

Table of Contents **2**
List of Figures **4**
List of Tables **5**
1. Introduction **6**
1.1. Revision identification **6**
1.2. Summary of device limitations **6**
2. Descriptions of device limitations **8**
2.1. RCU **8**
2.1.1. System operation fails due to system clock switching from high clock frequency to low clock frequency 8
2.2. GPIO **8**
2.2.1. Pin voltage level difference between PA11 and PA12 influences the power consumption in deep-sleep mode 8
2.3. DMA **8**
2.3.1. DMA channel counter reconfigures unsuccessfully 8
2.3.2. DMA burst transmission faults 9
2.4. IPA **9**
2.4.1. One extra pixel will be transferred 9
2.5. ADC **10**
2.5.1. ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment 10
2.5.2. ADC alignment mode is not consistent with the user manual description 10
2.6. RTC **11**
2.6.1. Calibrate abnormally when using both smooth digital calibration and FREQI calibration 11
2.7. TIMER **11**
2.7.1. The shadow preloaded value takes effect only on the rising edge of the counter after modification 11
2.7.2. Count error when timer works at single pulse mode 11
2.8. USART **12**
2.8.1. Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled 12
2.9. I2C **12**
2.9.1. I2C_FCTL register is only configurable on GD32F450xx 12
2.10. EXMC **12**
2.10.1. SDRAM controller can not be used time-shared with other EXMC controller 12

2.10.2. DSET bits and ASET bits configurations are invalid when NDWTEN bit is set 13
2.11. ENET 13
2.11.1. Data reception faults in MII mode 13
2.11.2. Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000 13
2.12. Core 13
2.12.1. VDIV or VSQRT instructions might not complete correctly when very short ISRs are used . 13
3. Revision history 15

List of Figures

Figure 1-1. Device revision code of GD32F45x/F40x 6

List of Tables

Table 1-1. Applicable products 6
Table 1-2. Device limitations 6
Table 2-1. Alignment mode of routine conversion 10
Table 3-1. Revision history 15

1. Introduction

This document applies to GD32F45x/F40x product series, as shown in ***Table 1-1. Applicable products***. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

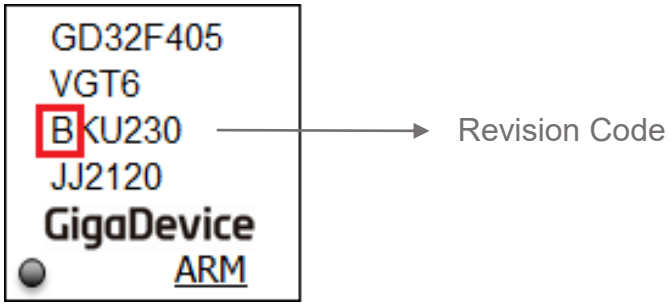
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32F405xx series
	GD32F407xx series
	GD32F450xx series

1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in ***Figure 1-1. Device revision code of GD32F45x/F40x***.

Figure 1-1. Device revision code of GD32F45x/F40x



1.2. Summary of device limitations

The device limitations of GD32F45x/F40x are shown in ***Table 1-2. Device limitations***, please refer to section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code B
RCU	*System operation fails due to system clock switching from high clock frequency to low clock frequency*	Y
GPIO	*Pin voltage level difference between PA11 and PA12 influences the power*	Y
DMA	*DMA channel counter reconfigures unsuccessfully*	Y
	DMA burst transmission faults	N

Module	Limitations	Workaround
		Rev. Code B
IPA	*One extra pixel will be transferred*	Y
ADC	*ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment*	Y
	ADC alignment mode is not consistent with the user manual description	Y
RTC	*Calibrate abnormally when using both smooth digital calibration and FREQI calibration*	Y
TIMER	*The shadow preloaded value takes effect only on the rising edge of the counter after modification*	N
	Count error when timer works at single pulse mode	Y
USART	*Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled*	Y
I2C	*I2C_FCTL register is only configurable on GD32F450xx*	N
EXMC	*SDRAM controller can not be used time-shared with other EXMC controller*	N
	DSET bits and ASET bits configurations are invalid when NDWTEN bit is set	N
ENET	*Data reception faults in MII mode*	Y
	Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000	Y
Core	*VDIV or VSQRT instructions might not complete correctly when very short ISRs are used*	Y

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. RCU

2.1.1. System operation fails due to system clock switching from high clock frequency to low clock frequency

Description & impact

System operation fails when system clock switching from high clock frequency (more than 120MHz) to low clock frequency.

Workarounds

Firstly, reduce the system frequency (such as HCLK / 2 or HCLK / 4); secondly, delay more than 20 HCLK clock; finally, switch to the low clock frequency.

2.2. GPIO

2.2.1. Pin voltage level difference between PA11 and PA12 influences the power consumption in deep-sleep mode

Description & impact

Pin level difference between PA11 and PA12 influences the power consumption in deep-sleep mode.

Workarounds

Keep the same pin level on PA11 and PA12.

2.3. DMA

2.3.1. DMA channel counter reconfigures unsuccessfully

Description & impact

DMA channel counter reconfigures unsuccessfully.

Workarounds

Clear full transfer finish flag (FTFIFx) and half transfer finish flag (HTFIFx) before reconfiguring the DMA channel counter.

2.3.2. DMA burst transmission faults

Description & impact

The rest of data bytes that is less than fifo depth generates transmission error when using DMA burst transmission.

Workarounds

Not available.

2.4. IPA

2.4.1. One extra pixel will be transferred

Description & impact

One extra pixel will be transferred when using register value to memory direction.

Workarounds

Before enable IPA to fill an area, try to find the address that will be clobbered by IPA fill function, save the data and then restore it. The reference code is as follows:

```
volatile uint16_t tmp_color1;
volatile uint16_t tmp_color2;
/* bytes_of_pixel depends on the DPF value of IPA_DPCTL register, when DPF equals to 0b010, bytes_of_pixel
= 2 */
volatile uint8_t bytes_of_pixel;
if(0 == (IPA_DPCTL&IPA_DPCTL_DPF)){
    bytes_of_pixel = 4;
}else if(1 == (IPA_DPCTL&IPA_DPCTL_DPF)){
    bytes_of_pixel = 3;
}else if(2 == (IPA_DPCTL&IPA_DPCTL_DPF)){
    bytes_of_pixel = 2;
}
……
/* find the address that will be corrupted by IPA fill, save the data */
tmp_color1 = *(volatile uint16_t*)(IPA_DMADDR + (((IPA_IMS&IPA_IMS_WIDTH)>>16) +
IPA_DLOFF&IPA_DLOFF_DLOFF)*bytes_of_pixel*(IPA_IMS&IPA_IMS_HEIGHT));
tmp_color2 = *(volatile uint16_t*)(IPA_DMADDR + (((IPA_IMS&IPA_IMS_WIDTH)>>16) +
IPA_DLOFF&IPA_DLOFF_DLOFF)*bytes_of_pixel*(IPA_IMS&IPA_IMS_HEIGHT) + 2);
IPA_CTL |= IPA_CTL_TEN;
……
/* restore them */
*(volatile uint16_t*)(IPA_DMADDR + (((IPA_IMS&IPA_IMS_WIDTH)>>16) +
```

```
IPA_DLOFF&IPA_DLOFF_DLOFF)*bytes_of_pixel*(IPA_IMS&IPA_IMS_HEIGHT)) = tmp_color1;
*(volatile uint16_t*)(IPA_DMADDR + (((IPA_IMS&IPA_IMS_WIDTH)>>16) +
IPA_DLOFF&IPA_DLOFF_DLOFF)*bytes_of_pixel*(IPA_IMS&IPA_IMS_HEIGHT) + 2) = tmp_color2;
```

2.5. ADC

2.5.1. ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment

Description & impact

ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment mode.

Workarounds

Use LSB alignment mode or use 8-bit sampling resolution.

2.5.2. ADC alignment mode is not consistent with the user manual description

Description & impact

ADC alignment mode is not consistent with the user manual description.

Workarounds

The right alignment mode description is as follow:

Table 2-1. Alignment mode of routine conversion

Alignment	Resolution	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LSB	12bit	0x0				data											
	10bit	0x0				data										0x0	
	8bit	0x0				data								0x0			
	6bit	0x0				data						0x0					
MSB	12bit	data												0x0			
	10bit	data										0x0					
	8bit	data								0x0							
	6bit	invalid															

2.6. RTC

2.6.1. Calibrate abnormally when using both smooth digital calibration and FREQI calibration

Description & impact

Using both smooth digital calibration and FREQI calibration will cause calibration result abnormal.

Workarounds

1) Use RTC shift function to replace smooth digital calibration, such as setting A1S bit and configuring appropriate SFS bits to satisfy the accuracy requirement.
2) Use two 16 seconds calibration window to replace one 32 seconds calibration window.

2.7. TIMER

2.7.1. The shadow preloaded value takes effect only on the rising edge of the counter after modification

Description & impact

The preloaded value takes effect only on the rising edge of the counter after modification which may cause problem to pwm applications with high timing requirements.

Workarounds

Not available.

2.7.2. Count error when timer works at single pulse mode

Description & impact

Timer works at single pulse mode and CK_APBx is CK_AHB / 4 and CK_TIMER is CK_AHB / 2, which causes count error.

Workarounds

1) Do not use above clock configuration.
2) Use timer update interrupt to clear error count.

2.8. USART

2.8.1. Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled

Description & impact

After mute mode is enabled, the operation on USART_CTL0 register will wake up USART from mute mode.

Workarounds

When mute mode is enabled and USART uses hardware method to detect idle frame wakeup, operation on USART_CTL0 register is not allowed. When mute mode is enabled and USART uses software method to detect idle frame wakeup, operation on USART_CTL0 register only be allowed when need to exit mute mode.

2.9. I2C

2.9.1. I2C_FCTL register is only configurable on GD32F450xx

Description & impact

The filter control register (I2C_FCTL) is only configurable on GD32F450xx but not on GD32F405xx or GD32F407xx.

Workarounds

Not available.

2.10. EXMC

2.10.1. SDRAM controller can not be used time-shared with other EXMC controller

Description & impact

SDRAM controller can not be used time-shared with other EXMC controller.

Workarounds

Not available.

2.10.2. DSET bits and ASET bits configurations are invalid when NDWTEN bit is set

Description & impact

Data setup time (DSET) and address setup time (ASET) configurations are invalid when wait function is enabled.

Workarounds

Not available.

2.11. ENET

2.11.1. Data reception faults in MII mode

Description & impact

ENET_MII_COL / ENET_MII_CRS / ENET_MII_RX_ER pins are floating on MCU and external PHY has no these pins,.which will cause data reception faults.

Workarounds

Configure ENET_MII_COL pin and ENET_MII_RX_ER pin as AF function and keep them low level. The ENET_MII_CRS pin mode and status can be ignored.

2.11.2. Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000

Description & impact

When enable hardware checksum and header checksum is 0x0000, this frame will be mistaken for error frame and dropped by hardware.

Workarounds

Use software checksum.

2.12. Core

2.12.1. VDIV or VSQRT instructions might not complete correctly when very short ISRs are used

This limitation refers to Arm ID number 776924 in “Cortex-M4 & Cortex-M4 with FPU Software

Developers Errata Notice".

Description & impact

The VDIV and VSQRT instructions take 14 cycles to execute. When an interrupt is taken a VDIV or VSQRT instruction is not terminated, and completes its execution while the interrupt stacking occurs. If lazy context save of floating point state is enabled then the automatic stacking of the floating point context does not occur until a floating point instruction is executed inside the interrupt service routine.

Lazy context save is enabled by default. When it is enabled, the minimum time for the first instruction in the interrupt service routine to start executing is 12 cycles. In certain timing conditions, and if there is only one or two instructions inside the interrupt service routine, then the VDIV or VSQRT instruction might not write its result to the register bank or to the FPSCR.

The failure occurring conditions are as follows:

1) The floating point unit is enabled.
2) Lazy context saving is not disabled.
3) A VDIV or VSQRT is executed.
4) The destination register for the VDIV or VSQRT is one of s0 - s15.
5) An interrupt occurs and is taken.
6) The interrupt service routine being executed does not contain a floating point instruction.
7) Within 14 cycles after the VDIV or VSQRT is executed, an interrupt return is executed.

A minimum of 12 of these 14 cycles are utilized for the context state stacking, which leaves 2 cycles for instructions inside the interrupt service routine, or 2 wait states applied to the entire stacking sequence (which means that it is not a constant wait state for every access).

In general, this means that if the memory system inserts wait states for stack transactions then this erratum cannot be observed.

The implications of this limitation is that the VDIV or VQSRT instruction does not complete correctly and the register bank and FPSCR are not updated, which means that these registers hold incorrect, out of date, data.

Workarounds

A workaround is only required if the floating point unit is enabled. A workaround is not required if the stack is in external memory.

There are two possible workarounds:

1) Disable lazy context save of floating point state by clearing LSPEN to 0 (bit 30 of the FPCCR at address 0xE000EF34).
2) Ensure that every interrupt service routine contains more than 2 instructions in addition to the exception return instruction.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	May.30 2022
1.1	1. Add workarounds of IPA limitations 2. Update note of chapter 1.2	Apr.4 2023
1.2	Add core limitation, referring to section 2.12.1	Oct.20 2023

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company under the intellectual property laws and treaties of the People’s Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as it’s suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as it’s suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products.

Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and Products and services described herein at any time, without notice.