GigaDevice Semiconductor Inc.

GD32L23x Hardware Development Guide

Application Note
AN069

Revision 1.4

(Dec. 2024)

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1. Introduction

The article is specially provided for developers of 32-bit general-purpose MCU GD32L23x series based on Arm® Cortex®-M23 architecture. It provides an overall introduction to the hardware development of GD32L23x series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32L23x series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32L23x series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32L23x series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32L23x series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32L23x series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32L23x series.
6. Reference circuit and PCB Layout design, mainly introduces GD32L23x series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32L23x series.

This document also satisfies the minimum system hardware resources used in application development based on GD32L23x series products.

Table 1-1. Applicable Products

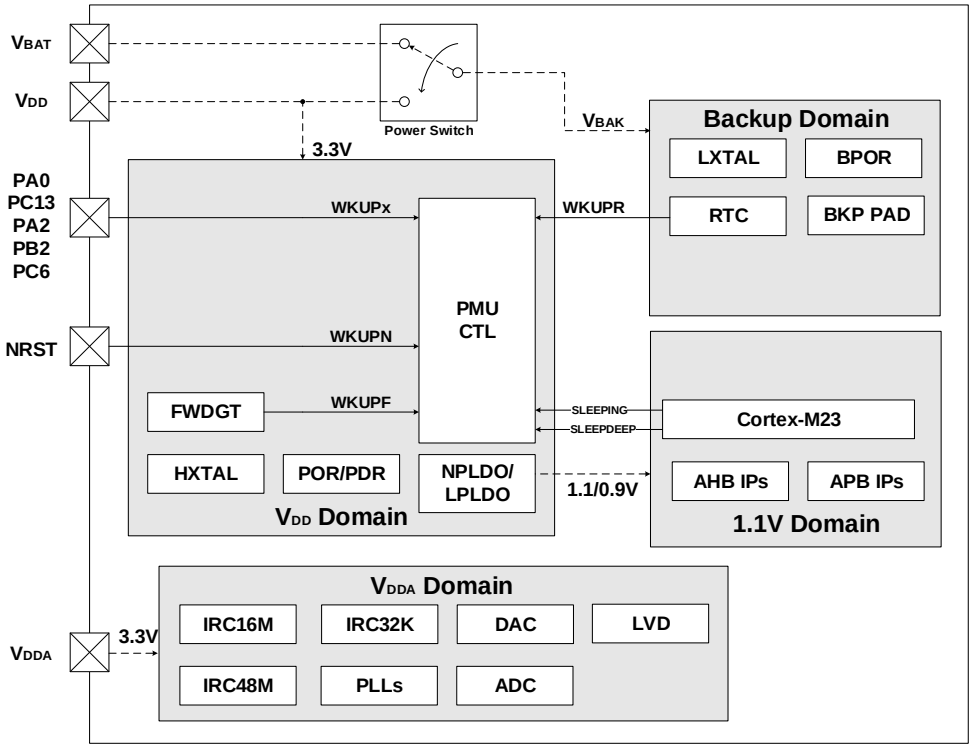
Type	Part Numbers
MCU	GD32L233xx series
	GD32L235xx series

2. Hardware design

2.1. Power supply

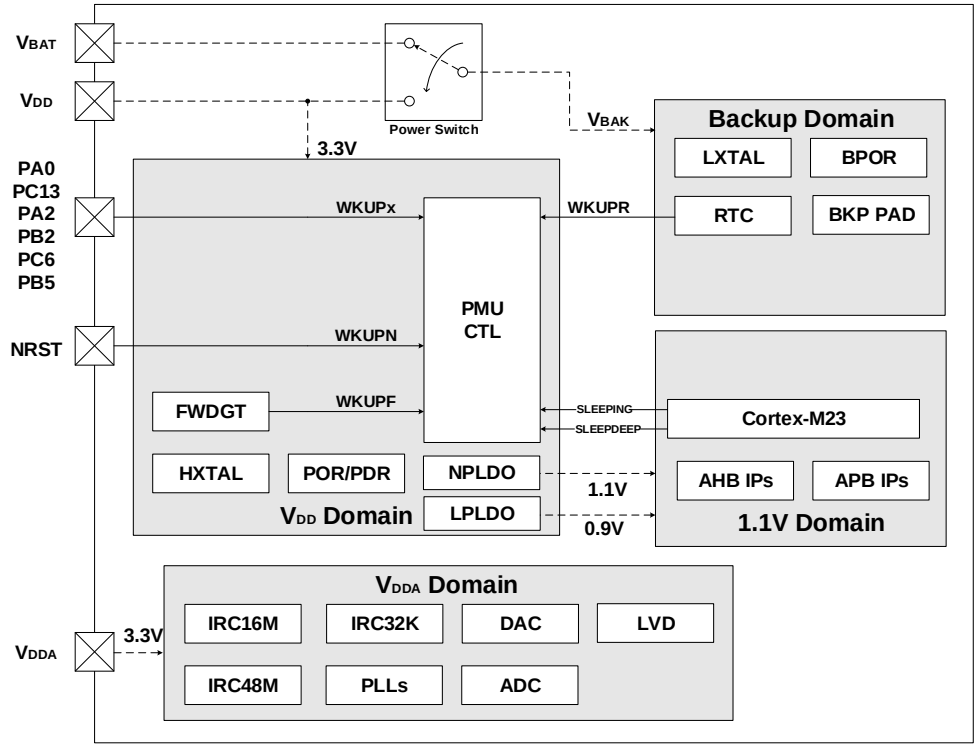
The V_{DD} / V_{DDA} operating voltage range of GD32L23x series products is 1.71 V ~ 3.63V. For GD32L23x series, there are three power domains, including V_{DD} / V_{DDA} domain, 1.1V domain, and Backup domain, as is shown in ***Figure 2-1. GD32L233 Power supply overview*** and ***Figure 2-2. GD32L235 Power supply overview***.The V_{DD}/V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.1 V domain. The backup domain power supply V_{BAK} can be powered by V_{DD} or V_{BAT} through the power switch Power Switch. When the V_{DD} power supply is turned off, the power switch can switch the power supply of the backup domain to the V_{BAT} pin. At this time, the backup domain is powered by the VBAT pin (battery).

Figure 2-1. GD32L233 Power supply overview



LVD: Low Voltage Detector
NPLDO: Normal power Voltage Regulator
BPOR: V_{BAK} Power On Reset
POR: Power On Reset
LPLDO: Low power Voltage Regulator
PDR: Power Down Reset

Figure 2-2. GD32L235 Power supply overview



LVD: Low Voltage Detector
POR: Power On Reset
NPLDO: Normal power Voltage Regulator
LPLDO: Low power Voltage Regulator
BPOR: V_{BAK} Power On Reset
PDR: Power Down Reset

2.1.1. Backup domain

The backup domain supply voltage range is 1.71V ~ 3.63V. The battery backup domain is powered by an internal power switch to select V_{DD} or V_{BAT} (battery) power, and then V_{BAK} powers the backup domain. In order to ensure the contents of the registers in the backup domain and the normal operation of the RTC, when V_{DD} is turned off, the VBAT pin can be connected to a backup source such as a battery or other power supply. If there is no external battery-powered application, it is recommended to connect the VBAT pin to the ground through a 100nF capacitor and then connect it to the VDD pin.

Note:

1、 During the V_{DD} power-on stage, the internal backup domain power supply of the chip is still connected to the VBAT pin. If V_{DD}>V_{BAT}+0.6V at this time, the current may be injected into V_{BAT} through the internal diode between V_{DD} and V_{BAT}, causing V_{BAT} pulses.

2、 Regarding the power consumption of the V_{BAT}, theoretically, when the V_{DD} of the MCU is powered on, the swich inside the backup domain is connected to VDD, and the VBAT pin has no current. However, when the main program uses the ADC to measure the V_{BAT} voltage through the internal channel , due to the MCU design, the voltage on V_{BAT} will be divided by 4, and then enter the ADC channel, so it will cause additional power consumption on the VBAT pin (tens of uA level).

2.1.2. V_{DD}/V_{DDA} domain

The V_{DD}/V_{DDA} power domain includes two parts: V_{DD} domain and V_{DDA} domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two should not exceed 300mV (the internal VDDA and VDD of the chip are connected through a back-to-back diode). To avoid noise, VDDA can be connected to VDD through an external filter circuit, and the corresponding VSSA is connected to VSS through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. There is a VREFP pin (For GD32L233 series, 1.8 V≤V_{REF}≤V_{DDA}. For GD32L235 series, 1.71 V≤V_{REF}≤V_{DDA}) for ADC independent power supply on the large package.

- The package chip with 48 pins and more contains VREFP pin, and V_{REF} can use an external reference power supply, or can be directly connected to V_{DDA}.
- The 32-pin package chip has no VREFP pin, it is directly connected to V_{DDA}, and all analog modules are powered by V_{DDA} (including ADC/DAC).

2.1.3. V_{REF} domain

In order to improve the performance of ADC/DAC, a precise internal voltage reference circuit is integrated in the GD32L23x series chip, which provides accurate reference voltage for ADC/DAC, and can also supply VREFP pin through external power supply. For GD32L233 series, the typical value of V_{REF} is generated internally: 2.5V. The GD32L235 series internally generates a typical V_{REF} value of 2.5V or 1.5V, which can be selected by configuring the VREFS bit in the REF_CS register. The precision reference is enabled by set the VREFEN bit in VREF_CS register (the SYSCFGEN bit in RCU_APB2EN register needs to be set to 1 before that), producing reference voltage and connecting to VREFP pin. When VREFEN is disabled, off-chip reference voltage could be injected to VREFP pin to source ADC/DAC. If there is no VREFP pin (refer to datasheet), the VREFP is connected to VDDA and the VREFEN bit must keep 0.

It is recommended to connect a 10nF+1uF ceramic capacitor to the ground outside the VREF pin.

2.1.4. Power supply design

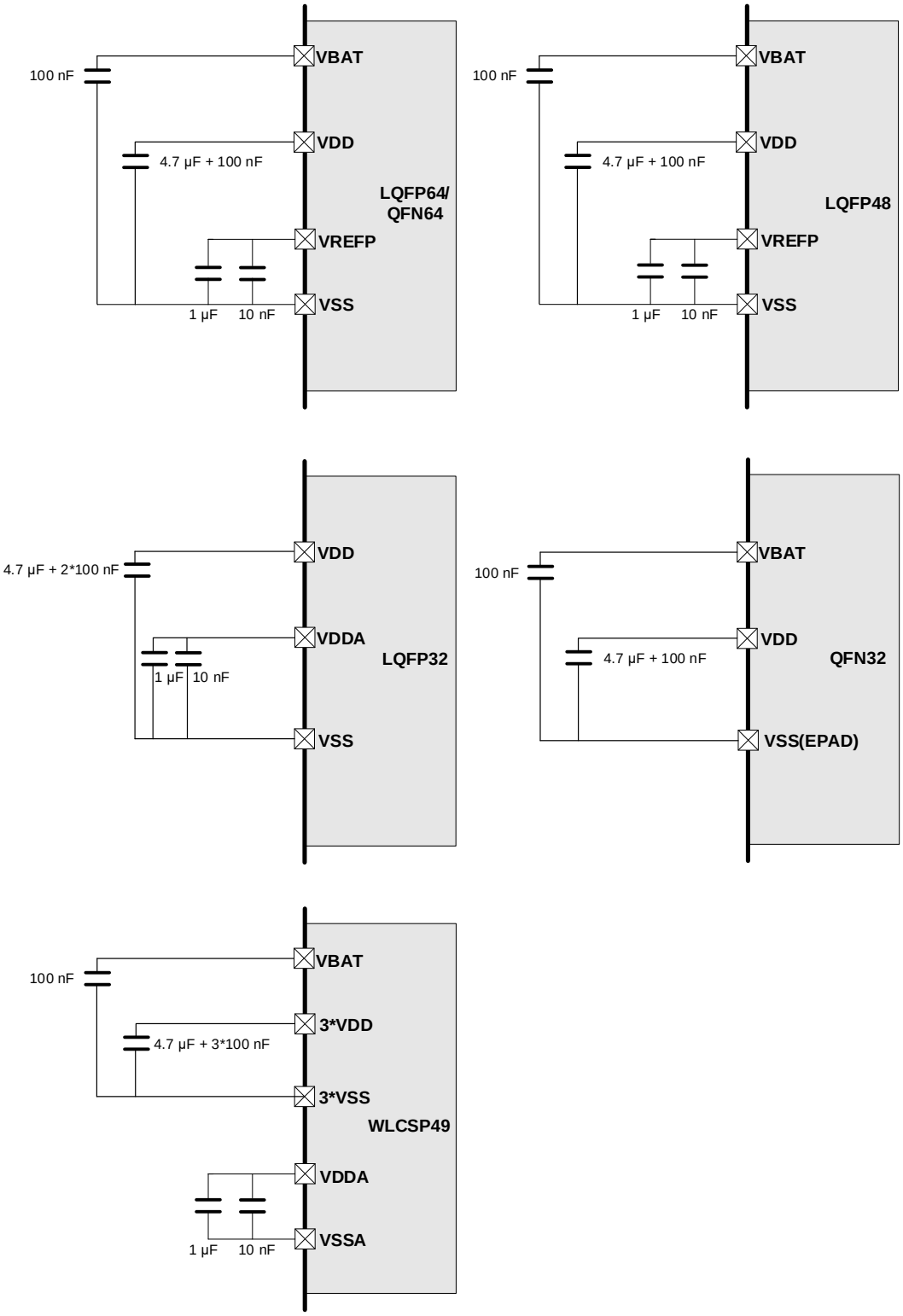
The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF).
- The VDDA pin must be connected with an external capacitor (10nF+1uF ceramic

capacitor is recommended).

- V_{REF} can be generated internally or directly to the VDDA.
- VBAT pin must be connected to an external battery (1.71 V ~ 3.63 V). If there is no external battery, it is recommended to connect the VBAT pin to the ground through a 100nF capacitor and then connect it to the VDD pin.

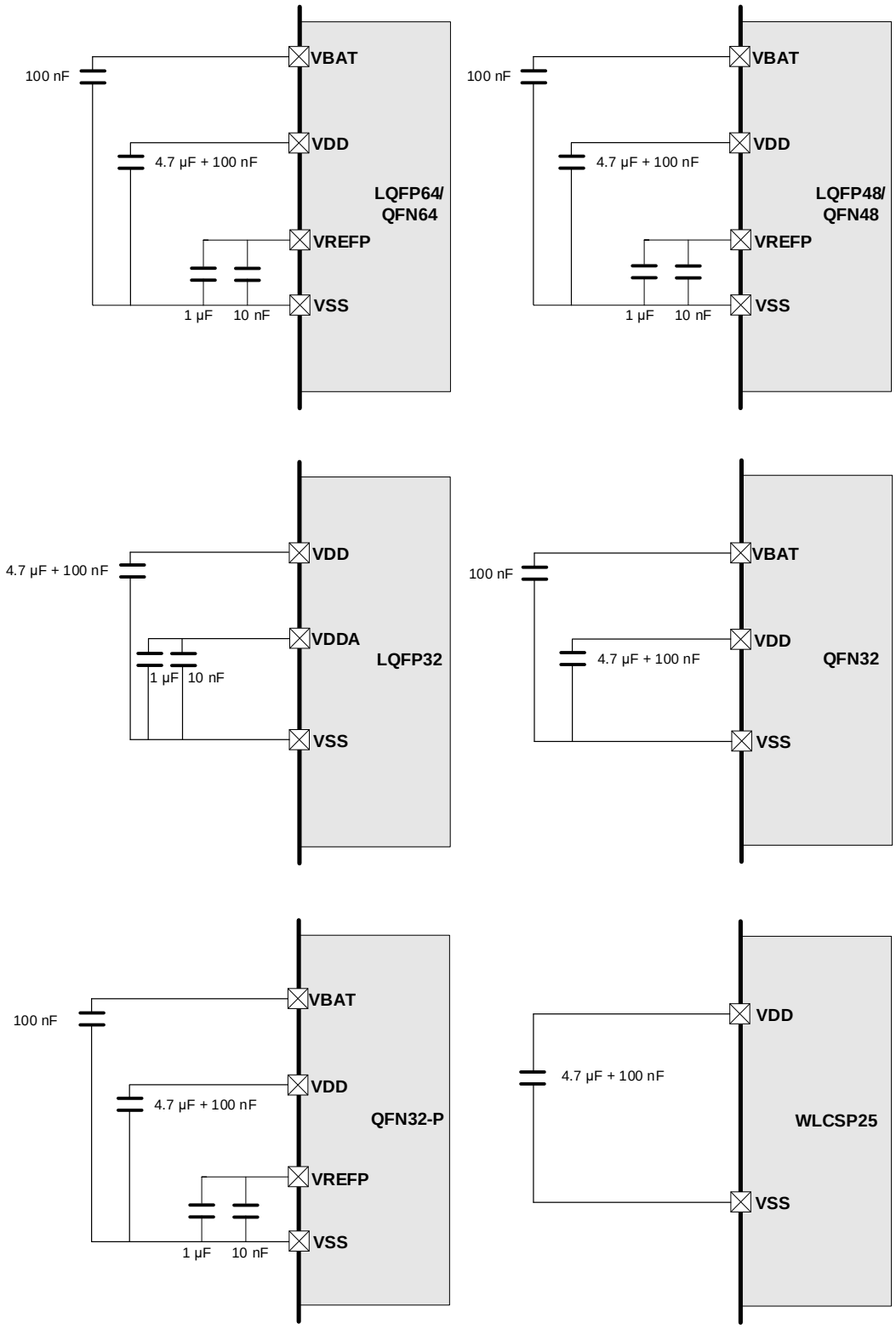
Figure 2-3. GD32L233 Recommended Power Supply Design



Note:

1. All decoupling capacitors need to be as close as possible to the pins on the PCB board.
2. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
3. LQFP64/QFN64: VSS, VSSA, VREFN are connected internally, VDD and VDDA are connected internally.
4. LQFP48: VSS, VSSA, VREFN are connected internally, VDD and VDDA are connected internally.
5. LQFP32: VSS, VSSA, VREFN are connected internally, VREFP and VDDA are connected internally.
6. QFN32: VREFP, VDD and VDDA are connected internally, VSS, VSSA, VREFN are connected with EPAD internally.
7. WLCSP49: VSSA and VREFN are connected internally, VREFP and VDDA are connected internally.

Figure 2-4. GD32L235 Recommended Power Supply Design



Note:

1. All decoupling capacitors need to be as close as possible to the pins on the PCB board.
2. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.

3. LQFP64: VSS, VSSA, VREFN are connected internally, VDD and VDDA are connected internally.
4. QFN64: VDD and VDDA are connected internally, VSS, VSSA, VREFN are connected with EPAD internally.
5. LQFP48: VSS, VSSA, VREFN are connected internally, VDD and VDDA are connected internally.
6. QFN48: VDD and VDDA are connected internally, VSS, VSSA, VREFN are connected with EPAD internally.
7. LQFP32: VREFP and VDDA are connected internally, VSS, VSSA, VREFN are connected internally,
8. QFN32: VREFP, VDD and VDDA are connected internally, VSS, VSSA, VREFN are connected with EPAD internally.
9. QFN32-P: VDD and VDDA are connected internally, VSS, VSSA, VREFN are connected with EPAD internally.
10. WLCSP25: VREFN, VSSA and VSS are connected internally, VREFP, VDDA and VDD are connected internally.

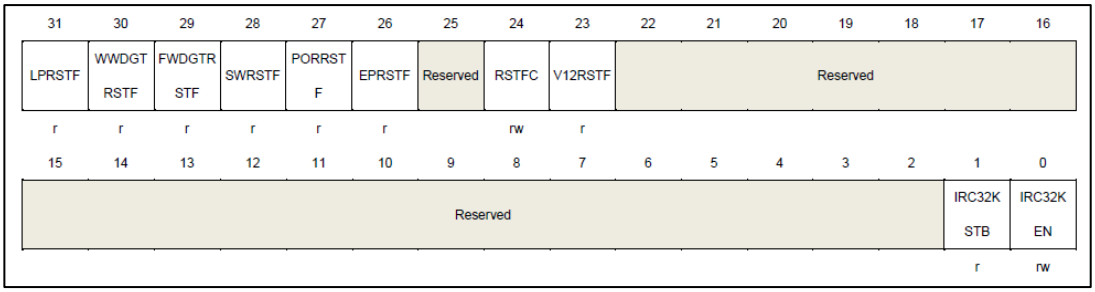
2.2. Power supply detection and reset

In this section, the default VDD and VDDA pins remain connected and are powered by the same power supply.

GD32L23x series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain when the power is turned on. During the power and system reset process, NRST will maintain a low level until the reset is over. When the MCU cannot be executed, the NRST pin waveform can be monitored by an oscilloscope to determine whether the chip has been reset.

In addition, the MCU reset source can be searched by the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register:

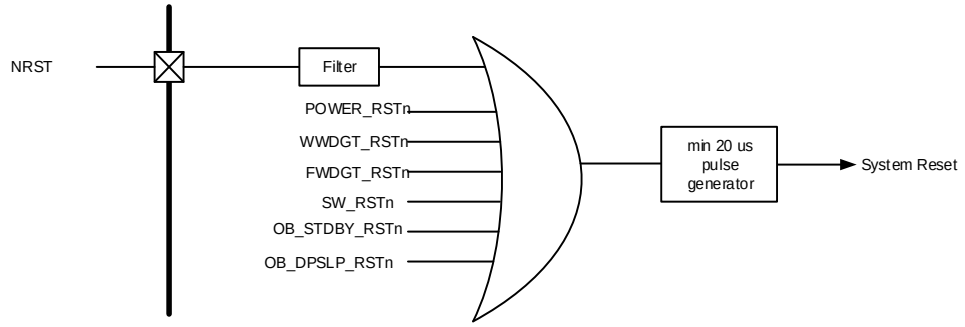
Figure 2-5. RCU_RSTSCK Register



MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level

pulse delay of at least 20μs. To prevent a false trigger reset, the NRST pin is recommended to place a capacitor (typically 100nF).

Figure 2-6. System Reset Circuit



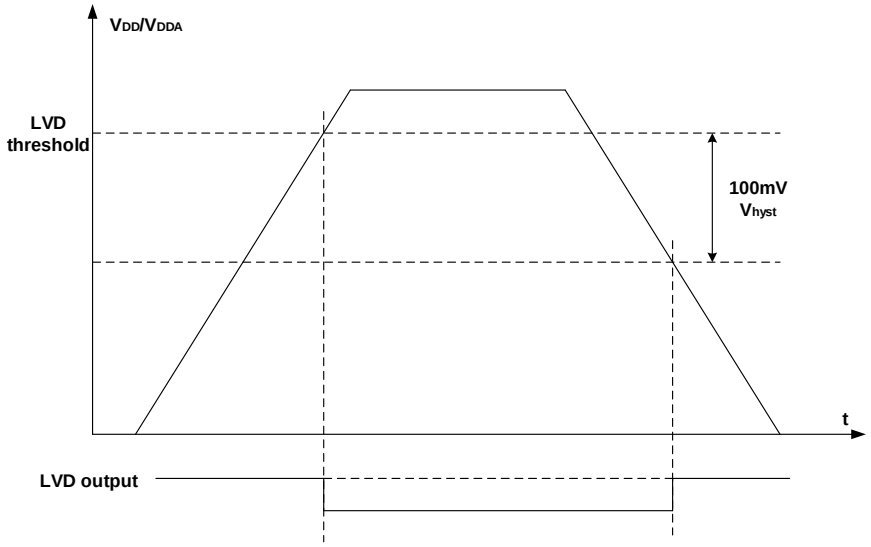
2.2.1. LVD

The LVD is used to detect whether the V_{DD} / V_{DDA} supply voltage is lower than a programmed threshold selected by the LVDT[2:0] bits in the power control register0 (PMU_CTL0). The LVD is enabled by setting the LVDEN bit, and LVDF bit, which in power control and status register (PMU_CS), indicates if V_{DD} / V_{DDA} is higher or lower than the LVD threshold. This event is internally connected to the EXTI line 16 and can generate an interrupt if it is enabled through the EXTI registers. ***Figure 2-7. LVD Threshold Waveform*** shows the relationship between the LVD threshold and the LVD output (LVD interrupt signal depends on EXTI line 16 rising or falling edge configuration). The following figure shows the relationship between the supply voltage and the LVD signal. The hysteresis voltage (V_{hyst}) is 100mV.

Note: When LVDT[2:0] is configured as "111", the input voltage on PB7 is compared with 0.8v, LVDF indicates if the input voltage is higher or lower than 0.8v.

LVD application: When the MCU power supply is subject to external interference, such as a voltage drop, we can set the low voltage detection threshold (the threshold is greater than the PDR value) through LVD. Once it falls to the threshold, the LVD interrupt is turned on, which can be used in the interrupt function. Set operations such as soft reset to avoid other exceptions from the MCU.

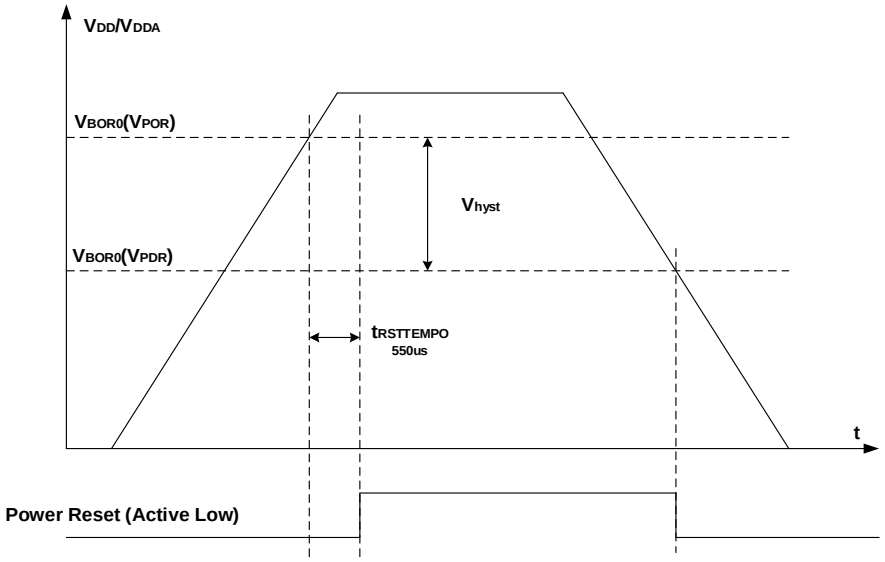
Figure 2-7. LVD Threshold Waveform



2.2.2. POR / PDR

The chip integrates a POR/PDR (power-on/power-down reset) circuit to detect V_{DD}/V_{DDA} and generate a power reset signal to reset the entire chip except the backup domain when the voltage is lower than a certain threshold. $V_{BOR0}(V_{POR})$ is the threshold voltage of power-on reset, the typical value of the GD32L233 series is about 1.60 V, and the typical value of the GD32L235 series is about 1.56 V. $V_{BOR0}(V_{PDR})$ is the threshold voltage of power-down reset, the typical value of the GD32L233 series is about 1.56 V, and the typical value of the GD32L235 series is about 1.48 V. The value of the hysteresis voltage V_{hyst} of the GD32L233 series is about 40 mV, and the value of the GD32L235 series is 80 mV.

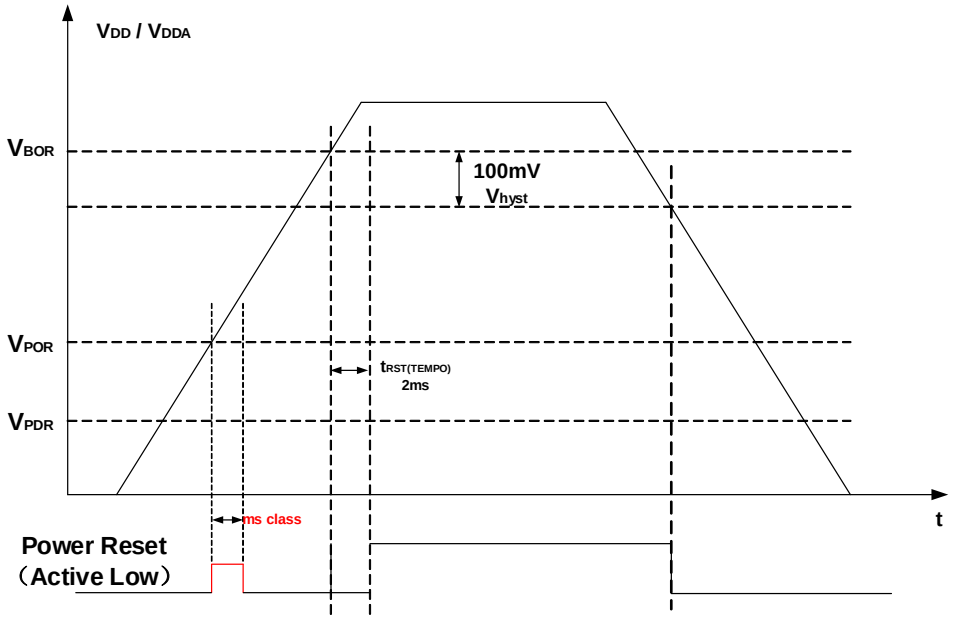
Figure 2-8. Power-on/power-down reset waveforms



2.2.3. BOR

The GD32L23x series MCU also integrates a BOR circuit. The BOR circuit is used to detect V_{DD} / V_{DDA} and generate the power reset signal which resets the whole chip except the Backup domain when the supply voltage is lower than the specified threshold which defined in the BOR_TH bits in option bytes. ***Figure 2-9. BOR Threshold Waveform*** shows the relationship between the supply voltage and the BOR reset signal. V_{BOR} represents the BOR reset threshold voltage, which is defined in the option byte BOR_TH. The value of the hysteresis voltage V_{hyst} is 100mV.

Figure 2-9. BOR Threshold Waveform



The BOR threshold is set through the option byte BOR_TH, and can set five different levels. Refer to the following table for the corresponding relationship.

Table 2-1. V_{BOR} Threshold Voltage Setting

Symbol	Conditions	Typ	
		GD32L233	GD32L235
BOR_TH=100(BOR level4)	Rising edge	2.90 V	2.90 V
	Falling edge	2.80 V	2.80 V
BOR_TH=011(BOR level3)	Rising edge	2.60 V	2.60 V
	Falling edge	2.50 V	2.50 V
BOR_TH=010(BOR level2)	Rising edge	2.30 V	2.30 V
	Falling edge	2.20 V	2.20 V
BOR_TH=001(BOR level1)	Rising edge	2.10 V	2.10 V
	Falling edge	2.00 V	2.00 V
BOR_TH=000/101/110/111 (BOR level0)	Rising edge	1.60 V	1.56 V
	Falling edge	1.56 V	1.48 V

The POR/PDR (power-on/power-off reset) circuit is always in the detection state. Therefore, the power reset level will be pulled up once when V_{DD}/V_{DDA} rises to V_{POR}, and then quickly

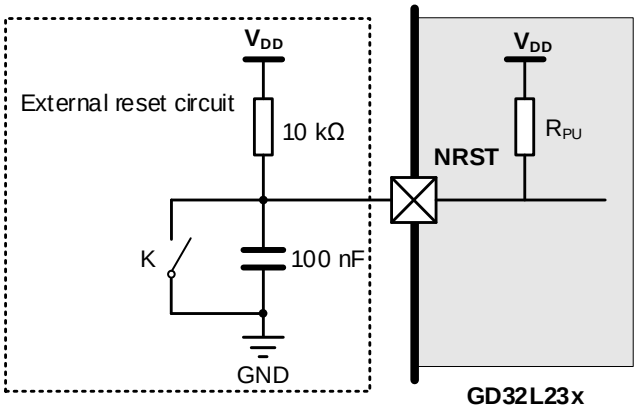
pulled down until V_{DD}/V_{DDA} rises to VBOR set by option byte BOR_TH, and the power reset level will be pulled up again.

That is, when V_{DD}/V_{DDA} rises the edge, the NRST pin voltage will have a pulse when V_{DD}/V_{DDA} reaches VPOR. The duration of the pulse is ms class. The pulse will not affect the normal operation of the chip, which is shown in the red pulse in the waveform diagram of the ***Figure 2-9. BOR Threshold Waveform***.

2.2.4. NRST Pin

For the NRST pin of the MCU, it is recommended to place a capacitor (typically 100 nF) in the NRST pins to prevent a false trigger reset.

Figure 2-10. Recommend External Reset Circuit

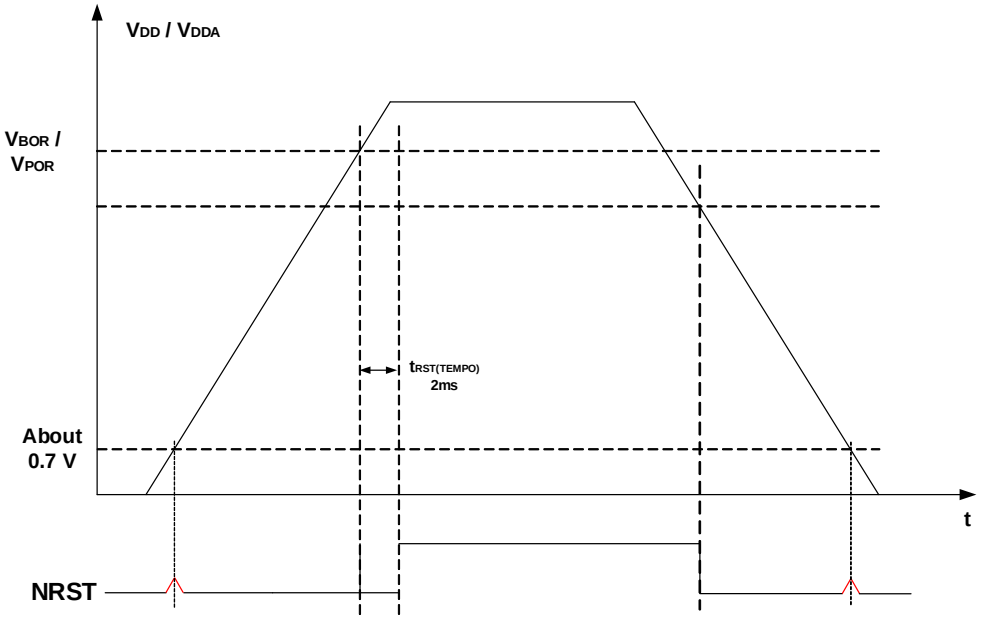


Note:

1. The pull-up resistor is recommended to be 10kΩ, so that voltage interference will not cause the chip to work abnormally.
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

Due to the threshold voltage characteristics of MOS transistors, during the power-up and power-down process of the chip, when V_{DD} / V_{DDA} is less than 0.7V, the internal pull-down MOS transistor of the chip will not pull the NRST pin low. In other words, during the power-up and power-down process, when V_{DD} / V_{DDA} is approximately 0.7V, a small pulse may occur, which does not affect the normal operation of the chip. This is illustrated by the red pulse shown in ***Figure 2-11. NRST Pin Power-On/Power-Down MOSFET Pulse Diagram***.

Figure 2-11. NRST Pin Power-On/Power-Down MOSFET Pulse Diagram



Due to the difference in charging and discharging speeds, the duration of the pulse on the falling edge is slightly longer than on the rising edge, with both durations being in the millisecond range.

2.3. Clock

GD32L23x series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

- 4-32 MHz external high-speed crystal oscillator (HXTAL)
- Internal 16 MHz RC oscillator (IRC16M)
- Internal 48 MHz RC oscillator (IRC48M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- Internal 32 kHz RC oscillator (IRC32K)
- PLL clock source can be selected from HXTAL, IRC16M or IRC48M.
- HXTAL and LXTAL clock monitor

Figure 2-12. Clock tree of GD32L233xx devices

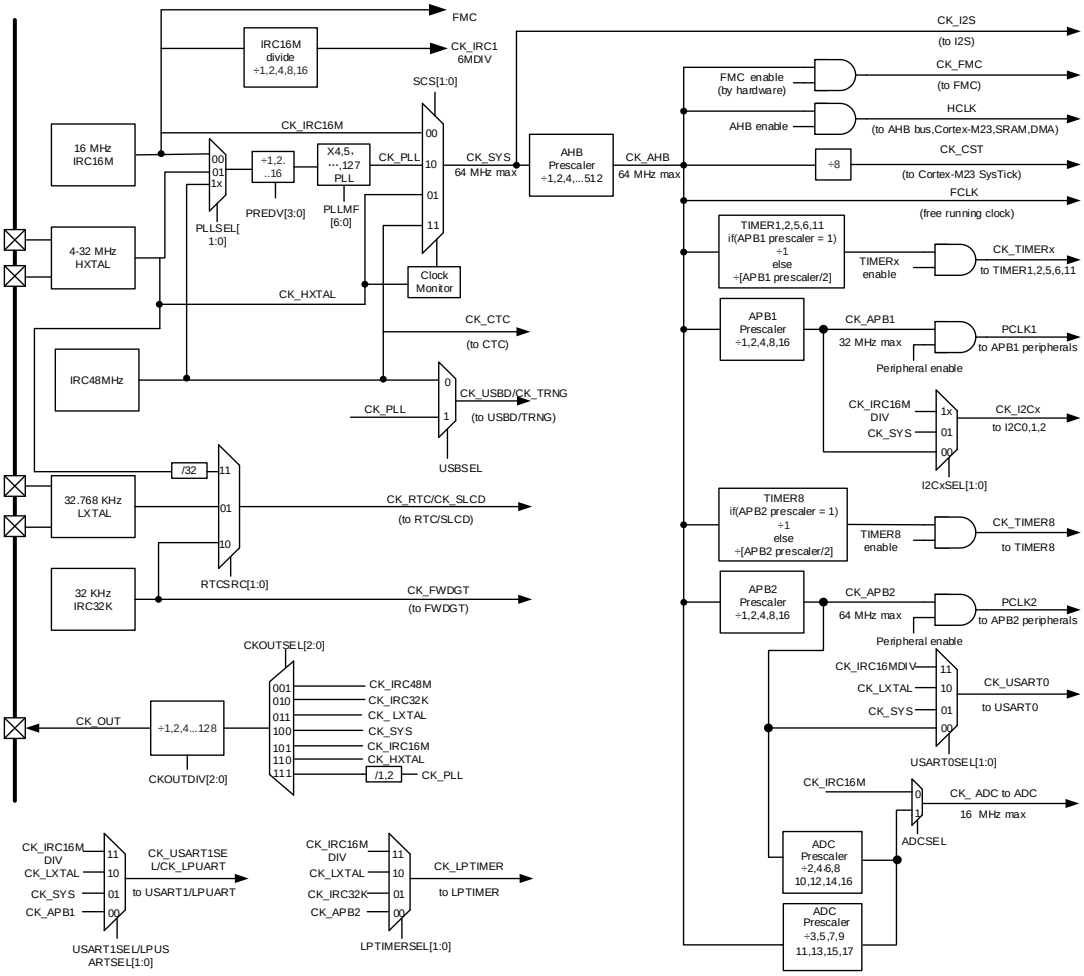
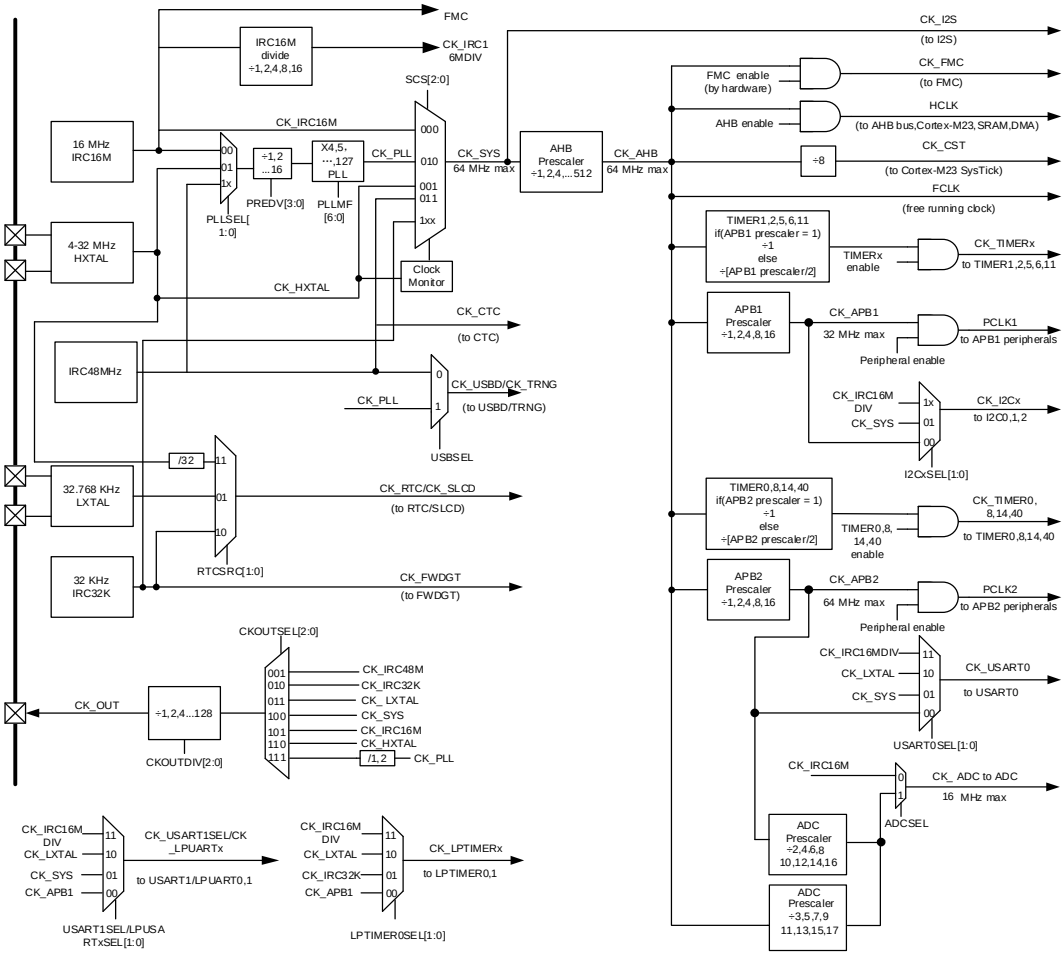


Figure 2-13. Clock tree of GD32L235xx devices



2.3.1. External high-speed crystal oscillator clock (HXTAL)

4-32MHz external high-speed crystal oscillator (passive crystal) can provide accurate main clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSC_IN, and OSC_OUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-14. HXTAL External Crystal Circuit

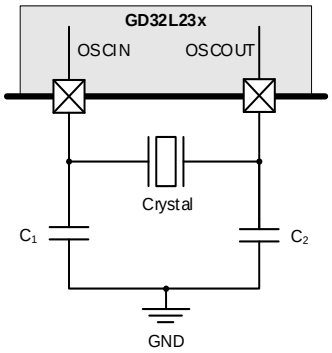
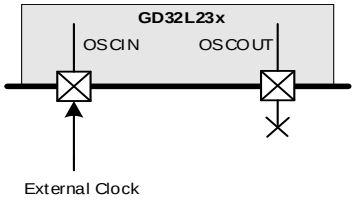


Figure 2-15. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC16M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}.
7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSC_OUT and OSC_IN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate

the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768 kHz low-speed external crystal (passive crystal), which can provide a low-power and high-precision clock source for RTC. The RTC module of the MCU is equivalent to a counter. The accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-16. LXTAL External Crystal Circuit

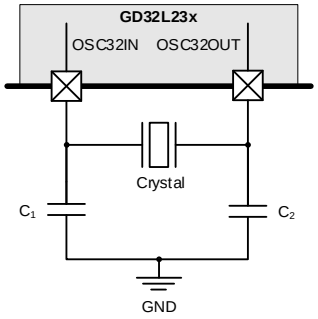
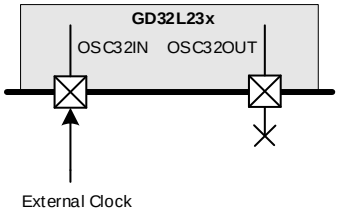


Figure 2-17. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32_IN, and OSC32_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. When the RTC selects IRC32K as the clock source and uses V_{BAT} for external independent power supply, if the MCU is powered off at this time, the RTC will stop counting. After re-powering, the RTC will continue to count up with the previous count value. If the application needs to use V_{BAT} to power the RTC, the RTC can still time

normally, and the RTC must select LXTAL as the clock source.

4. The MCU can set the drive capability of LXTAL. If it is found that the external low-speed crystal is difficult to vibrate during the actual debugging process, you can try to adjust the drive capability of LXTAL to high drive capability.
5. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the two crystal pins of the MCU due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.3. Clock Output Capability (CKOUT)

GD32L23x series MCUs can output clocks from 32kHz to 64MHz. There are several clock signals can be selected via the CK_OUT clock source selection bits, CKOUTSEL, in the configuration register 0 (RCU_CFG0). The corresponding GPIO pin (PB13, PA8, PA9) should be configured in the properly alternate function I/O (AFIO) mode to output the selected clock signal.

Table 2-2. CKOUT0SEL[1:0] Control Bits

CKOUTSEL[2:0]	Clock source
000	No Clock
001	CK_IRC48M
010	CK_IRC32K
011	CK_LXTAL
100	CK_SYS
101	CK_IRC16M
110	CK_HXTAL
111	CK_PLL or CK_PLL/2

2.3.4. HXTAL Clock Monitor (CKM)

The HXTAL clock monitor function is enabled by the HXTAL clock monitor enable bit, CKMEN, in the control register, RCU_CTL. This function should be enabled after the HXTAL start-up delay and disabled when the HXTAL is stopped. Once the HXTAL failure is detected, the HXTAL will be automatically disabled. The HXTAL Clock Stuck Flag, CKMIF, in the interrupt register, RCU_INT, will be set and the HXTAL failure event will be generated. This failure interrupt is connected to the Non-Maskable Interrupt, NMI, of the Cortex®-M23.

Note: If the HXTAL is selected as the clock source of CK_SYS or PLL, the HXTAL failure will force the CK_SYS source to IRC16M and the PLL will be disabled automatically.

2.3.5. LXTAL Clock Monitor (LCKM)

A clock monitor on LXTAL can be activated by software writing the LXTALCKMEN bit in the control register (RCU_CTL). LXTALCKMEN can not be enabled before LXTAL and IRC32K are enabled and ready.

The clock monitor on LXTAL is working in all modes except VBAT. If a failure is detected on the external 32 kHz oscillator, an interrupt can be sent to CPU.

The software must then disable the LXTALCKMEN bit, stop the defective 32 kHz oscillator, and change the RTC clock source, or take any required action to secure the application.

A 4-bits plus one counter will work at IRC32K domain when LXTALCKMEN enable. If the LXTAL clock has stuck at 0 / 1 error or slow down about 20KHz, the counter will overflow. The LXTAL clock failure will been found.

2.4. Startup Configuration

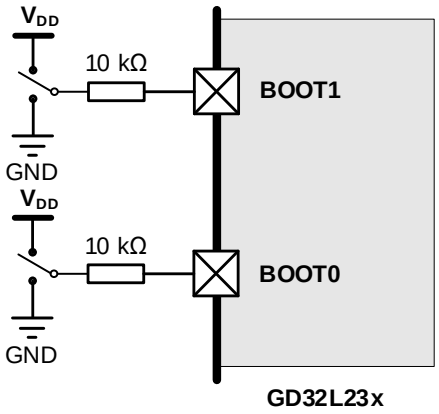
The GD32L23x series provides three boot modes, which can be selected by the BOOT0 bit and the BOOT1 pin to determine the boot option. When designing the circuit, run the user program, the BOOT0 pin cannot be left floating, it is recommended to connect a 10kΩ resistor to GND; when running the System Memory to update the program, you need to connect the BOOT0 pin to high and the BOOT1 pin to low. After the update is completed, the user program can be run after the BOOT0 is connected to a low level; the SRAM execution program is mostly used in the debugging status.

The embedded Bootloader is stored in the system storage space for reprogramming the FLASH memory. Bootloader can interact with the outside world through USART0 (PA9 and PA10), USART1 (PA2 and PA3) or USBD (PA11 and PA12).

Table 2-3. BOOT mode

BOOT mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-18. Recommend BOOT Circuit Design



Note:

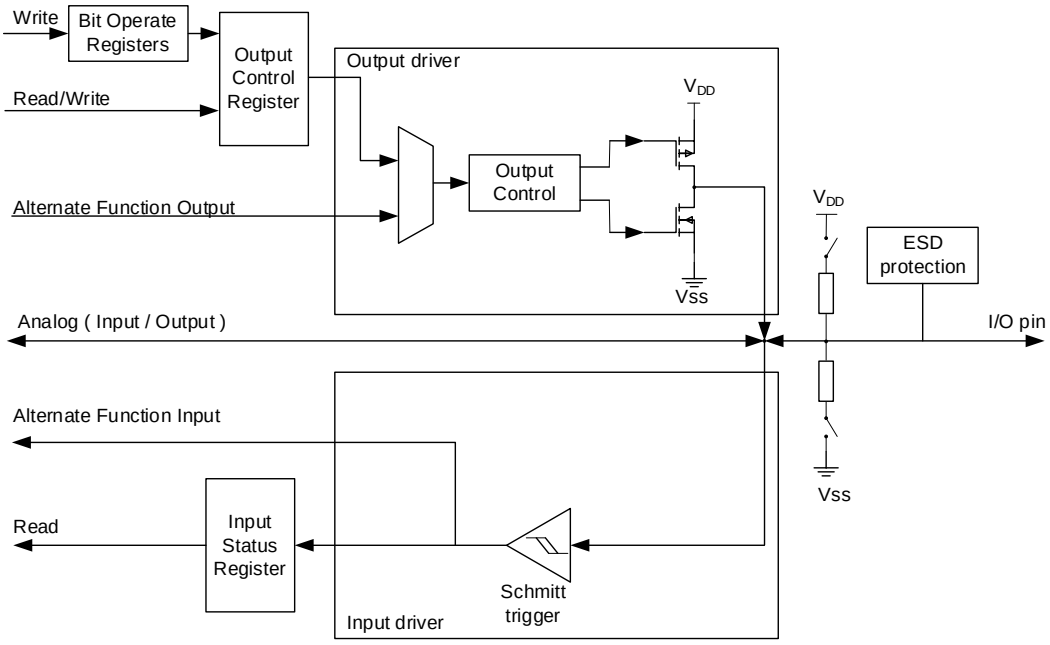
1. After the MCU is running, if the BOOT state is changed, it will take effect after the system is reset. MCU.
2. Once the BOOT1 pin state is sampled, it can be released for other purposes.

2.5. Typical Peripheral Modules

2.5.1. GPIO Circuit

GD32L23x can support up to 59 general-purpose I/O pins (GPIO), which are PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD6, PD8 ~ PD9, PF0 ~ PF1; each pin can be independently configured through registers, the basic structure of the GPIO port is shown in the following figure:

Figure 2-19. Basic structure of standard IO



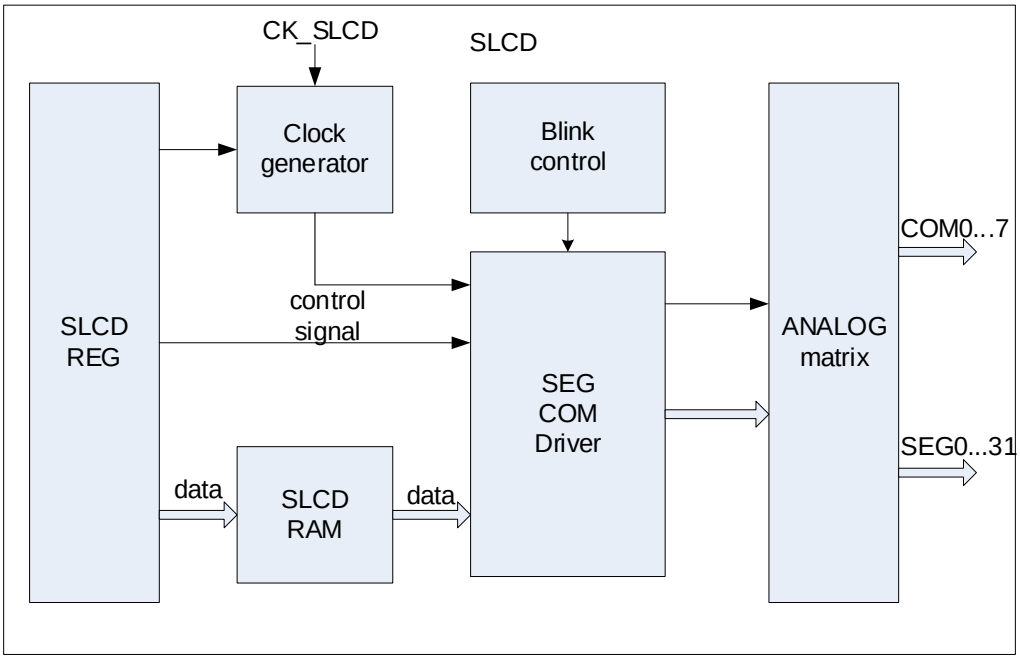
Note:

1. The IO port is divided into 5V tolerant and non-5V tolerant. When using, pay attention to distinguish the IO port withstand voltage.
2. When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.
3. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
4. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
5. The four IO ports of PC13, PC14, PC15 have weak drive capability and limited output current capability. When configured in output mode, their working speed cannot exceed 2MHz.
6. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.

2.5.2. SLCD Circuit

The SLCD controller directly drives LCD displays by creating the AC segment and common voltage signals automatically. It can drive the monochrome passive liquid crystal display (LCD) which composed of a plurality of segments (pixels or complete symbols) that can be converted to visible or invisible. The SLCD controller can support up to 32 segments and 8 commons. The block diagram of the SLCD controller is shown as follows:

Figure 2-20. ADC Acquisition Circuit Design



The SLCD REG is the register of SLCD controller, which configured by APB bus, and generate interrupt to CPU. It includes SLCD_CTL, SLCD_CFG, SLCD_STAT, SLCD_STATC, SLCD_DATAx registers.

The Clock generator generates SLCD clock from input clock. The SLCD clock drivers the blink control and SEG/COM driver. The Blink control generates blink frequency and blink pixels. The SEG/COM driver generates segment and common signals to ANALOG matrix. The ANALOG matrix implements segment and common voltages.

Note: The SLCD can selected the internal voltage source or external voltage source by the VSRC bit of the SLCD_CTL register. The precautions for using internal/external voltage sources for SLCD are as follows:

1. When the SLCD selects the internal voltage source, the PD6 pin needs to be configured in analog mode, and an external 1uF capacitor should be connected to GND.
2. When the SLCD selects an external voltage source, the PD6 pin needs to be configured in analog mode and connected to an external voltage source.

2.5.3. ADC Circuit

The GD32L23x integrates a 12-bit SAR ADC with up to 20 channels, which can measure 16 external and 2 internal signal sources and 1 external battery monitoring signal source, 1 SLCD voltage monitoring signal source. The internal signal is the temperature sensor channel (ADC_CH16), the internal reference voltage input channel (ADC_CH17), and the external signal is the external monitoring battery V_{BAT} power supply pin input channel (ADC_CH18), input channel for monitoring V_{SLCD} (ADC_CH19).

The temperature sensor reflects the change in temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external

temperature sensor must be used. The internal reference voltage V_{REFINT} provides a regulated voltage output (1.2V) to the ADC. Provides the function of externally detecting the battery voltage of the V_{BAT} pin, and the converted value is V_{BAT}/3, the converted value of V_{SLCD} is V_{SLCD} /3.

The GD32L233 series supports only single-ended input mode, and the GD32L235 series supports single-ended input mode and differential input mode. For GD32L235 series products, when the ADC is disabled (ADCON = 0), the user can configure channels as differential input mode or single-ended input mode. The channel n voltage is the difference between positive input and negative input. The positive input is external voltage V_{INn}, and there is a difference of the negative input between single-ended mode and differential input mode. In single-ended input mode, the negative input is V_{REFN}, in differential input mode, the negative input is $V_{IN(n+1)}$. And therefore, channel (n+1) is no longer usable in single-ended mode or in differential mode and must never be configured to be converted.Channel 15, 16, 17, 18 and 19 are forced to single-ended configuration (corresponding bits DIFCTL[n] is always zero), because they are connected to internal channels.When the channel is used in differential input mode, the input voltages should be differential signals (common mode voltage is V_{REFP}/ 2), and the input ranges are still (V_{REFN} ~ V_{REFP}).

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin. It is recommended to place a small capacitor of 500pF.

Figure 2-21. ADC single-ended input mode Acquisition Circuit Design

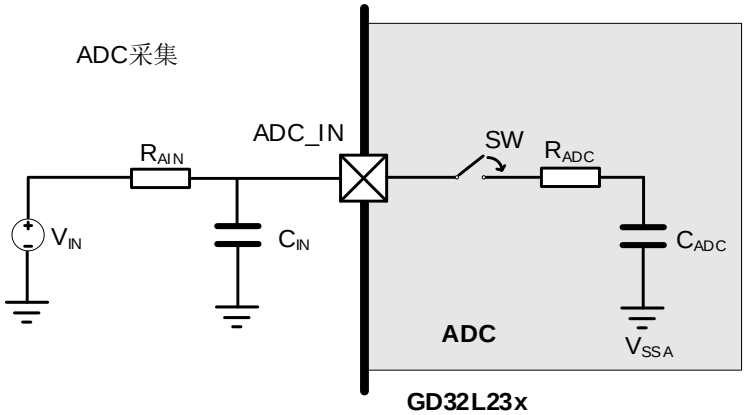
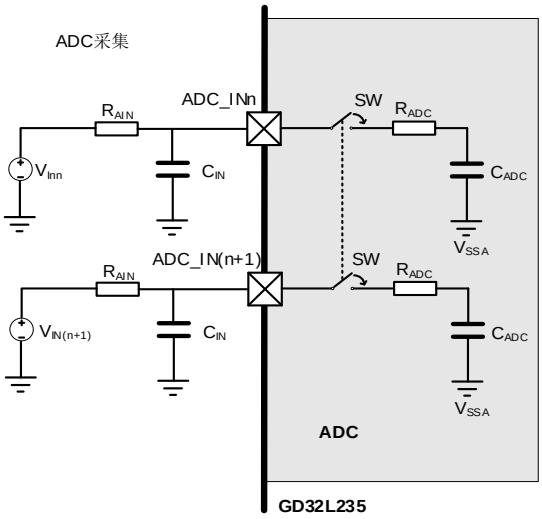


Figure 2-22. ADC differential input mode Acquisition Circuit Design



When f_{ADC} = 16MHz, the relationship between the input impedance and the sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, and select a larger value for the sampling period. When designing external circuits, try to reduce the input Impedance, if necessary, use the op amp to follow to reduce the input impedance.

Table 2-4. f_{ADC} =16MHz Relationship between sampling period and external input impedance of GD32L233 series

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (kΩ)
2.5	0.16	4.8
7.5	0.47	15.6
13.5	0.85	28.4
28.5	1.79	60.6
41.5	2.60	88.5
55.5	3.47	118.6
71.5	4.47	153.0
239.5	14.97	513.6

Table 2-5. f_{ADC} =16MHz Relationship between sampling period and external input impedance of GD32L235 series

Resolution	Sampling cycles @16MHz	R_{AIN} max (kΩ)	
		V_{DDA} < 2.4V	V_{DDA} ≥ 2.4V
12 bits	2.5	N/A	1.0
	7.5	0.6	5.2
	13.5	5.7	10.3
	28.5	18.4	23.0
	41.5	29.4	34.0
	55.5	41.3	45.9
	71.5	54.8	59.4
	239.5	197.2	201.8

Resolution	Sampling cycles @16MHz	R_{AIN} max (kΩ)	
		V_{DDA} < 2.4V	V_{DDA} ≥ 2.4V
10 bits	2.5	N/A	1.3
	7.5	1.7	6.3
	13.5	7.6	12.2
	28.5	22.4	27.0
	41.5	35.3	39.9
	55.5	49.1	53.7
	71.5	64.9	69.5
	239.5	231.0	235.6
8 bits	2.5	N/A	1.8
	7.5	3.9	7.7
	13.5	11.6	14.9
	28.5	31.0	32.7
	41.5	47.7	48.1
	55.5	65.7	64.7
	71.5	86.4	83.7
	239.5	302.8	283.0
6 bits	2.5	N/A	2.6
	7.5	5.4	10.0
	13.5	14.3	18.9
	28.5	36.5	41.1
	41.5	55.8	60.4
	55.5	76.6	81.2
	71.5	100.3	104.9
	239.5	349.4	354.0

2.5.4. DAC Circuit

The digital/analog converter of GD32L23x series MCU can convert 12-bit digital data to voltage output on external pins. Data can be in 8-bit or 12-bit mode, left-justified or right-justified. When external triggering is enabled, DMA can be used to update digital data on the input. At the output voltage, higher drive capability can be obtained by enabling the DAC output buffer. The two DACs can work independently or concurrently.

Table 2-6. DAC Related Pin Description

Name	Description	Signal type
V_{DDA}	Analog power	Input, Analog power
V_{SSA}	Analog power ground	Input, Analog power ground
V_{REFP}	DAC positive reference voltage	Input, Analog positive reference voltage
DAC_OUTx	DACx analog output	Analog output signal

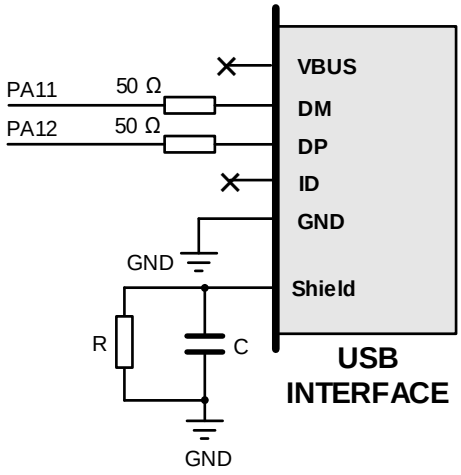
Before enabling the DAC module, the GPIO port (PA4 corresponds to DAC0) should be

configured in analog mode.

2.5.5. USB Circuit

GD32L23x can only be designed as a USB device. USB-Device Reference Circuit is recommended as follows, When designing the circuit, in order to improve the ESD performance of the USB, it is recommended to design a resistance-capacitance discharge isolation circuit for the USB case.

Figure 2-23. Recommend USB-Device Reference Circuit

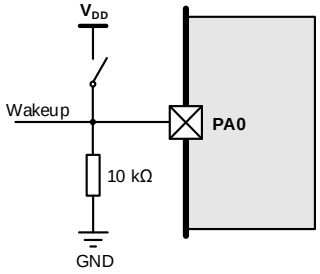


Recommendation: R = 1MΩ, C = 4700pF

2.5.6. Standby mode wake-up circuit

The power consumption is regarded as one of the most important issues for the devices of GD32L23x series. For GD32L233xx devices, power management unit (PMU) provides ten types of power saving modes, including Run, Run1, Run2, Sleep, Sleep1, Sleep2, Deep-sleep, Deep-sleep 1, Deep-sleep 2 and Standby mode. For GD32L235xx devices, power management unit (PMU) provides six types of power saving modes, including Run, Sleep, Deep-sleep, Deep-sleep 1, Deep-sleep 2 and Standby mode. The lowest power consumption is the standby mode, which requires the longest wake-up time. Wake-up from Standby mode can be woken up by the rising edge of the WKUP pin. At this time, there is no need to configure the corresponding GPIO, just configure the WUPENx bit in the PMU_CS register. The reference circuit design corresponding to the WKUP wake-up pin is as follows.

Figure 2-24. Recommend Standby external wake-up pin circuit design



Note:

1. In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.
2. If WUPEN0 is set before entering the power saving mode, a rising edge on the WKUP pin0 wakes up the system from the power saving mode. As the WKUP pin0 is active high, the WKUP pin0 is internally configured to input pull down mode. And set this bit will trigger a wakup event when the input is aready high.As the same with other WKUP bit. Learing more can refer to use manual

2.6. Download the debug circuit

The GD32L23x series cores only support SWD debug interface, not JTAG interface. The SWD interface standard is a 5-pin interface, of which 2 are signal interfaces.

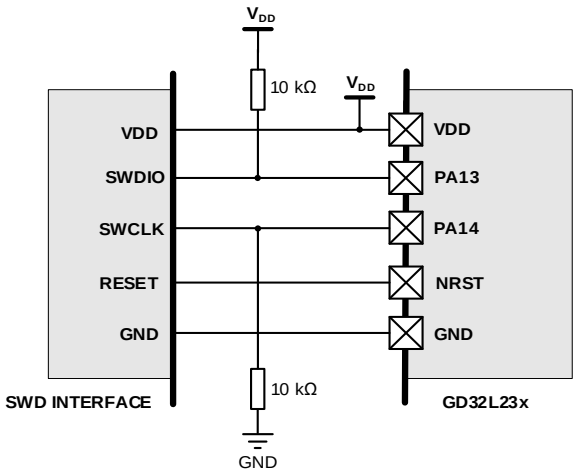
Note: After reset, the debug related ports are in input PU/PD mode, where:

PA13: JTMS/SWDIO in pull-up mode.
PA14: JTCK/SWCLK in pull-down mode.

Table 2-7. SWD Download Debug Interface Assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-25. Recommend SWD Wiring Reference Design

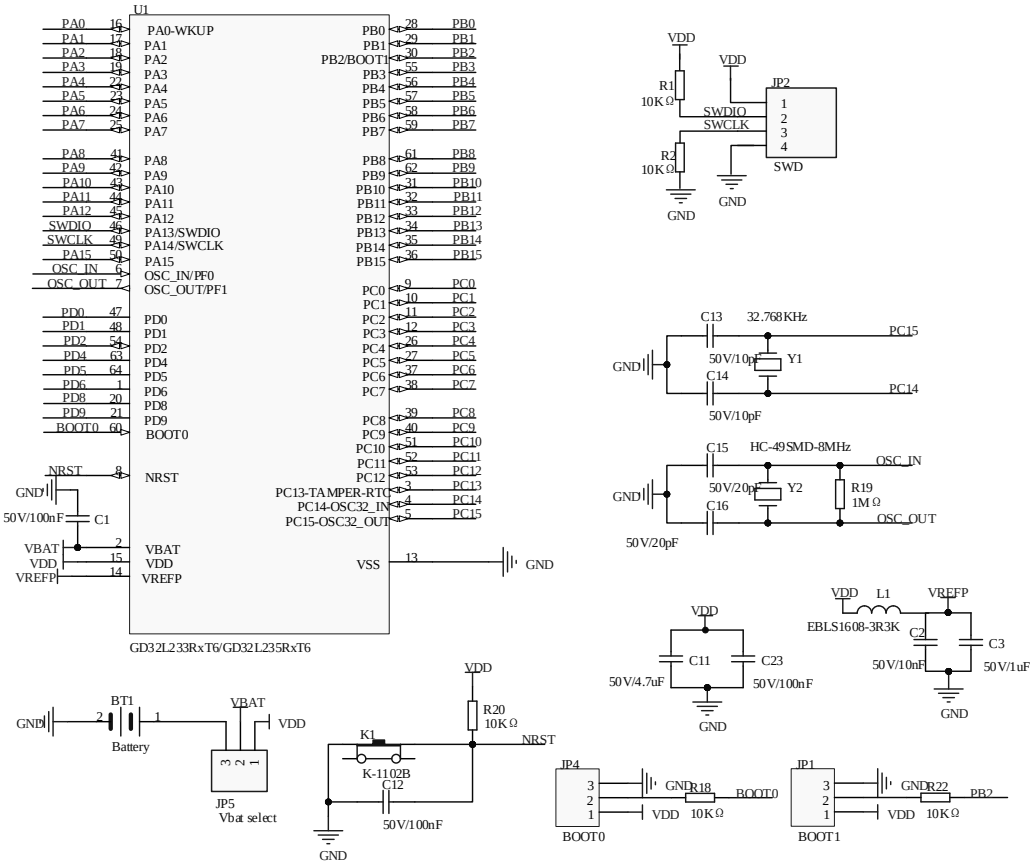


There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω~1kΩ resistor.

2.7. Reference Schematic Design

Figure 2-26. GD32L23x Recommend Reference Schematic Design



3. PCB Layout Design

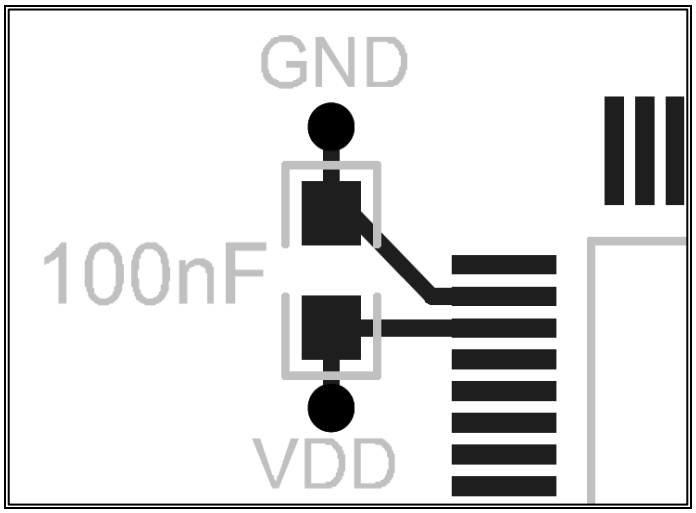
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32L23x series power supply has three power supply pins: V_{DD}, V_{DDA} and V_{REFP}. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended to punch holes near the capacitor pad to connect with GND.

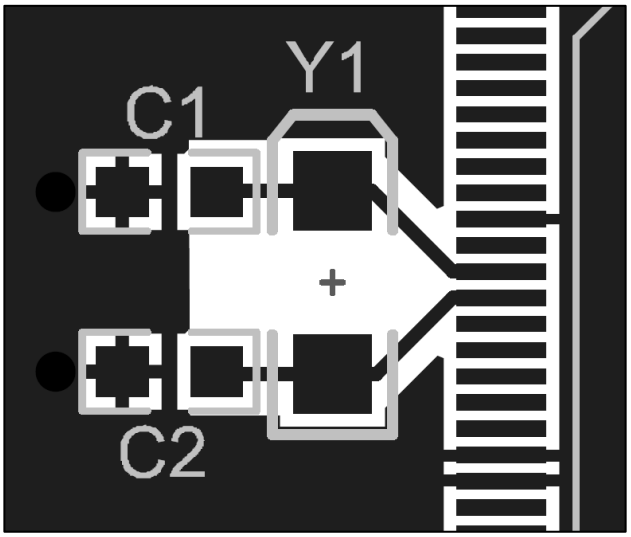
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32L23x series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



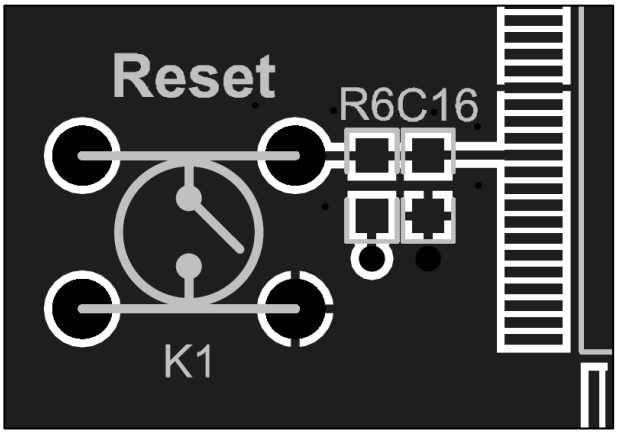
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design



Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better

to wrap the NRST traces for better shielding effect.

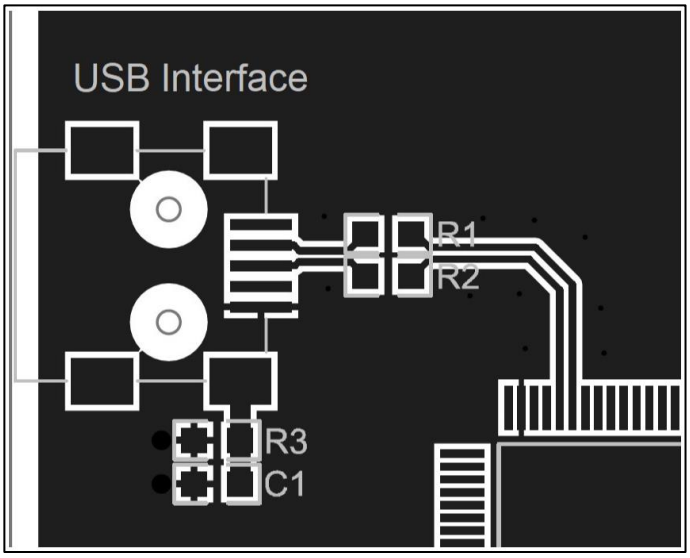
3.4. USB Circuit

The USB module has two differential signal lines, DM and DP. It is recommended that the PCB traces require a characteristic impedance of 90ohm. The differential traces should be run in strict accordance with the rule of equal length and equal distance, and the traces should be kept as short as possible. If the two differential lines are not equal in length , the short line can be compensated with a serpentine line at the terminal.

Due to impedance matching considerations, the series matching resistance is recommended to be about 50Ω.

The reference of DM and DP differential trace is as follows:

Figure 3-4. Recommend DM, DP Differential Trace Layout Design



Recommendation: R1 = R2 = 50Ω, R3 = 1MΩ, C = 4700pF

Note:

1. Reasonable placement during layout to shorten the differential trace distance.
2. Draw differential lines first, try not to exceed two pairs of vias for a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring to ensure that the two lines are tightly coupled, avoiding 90°, arc or 45° wiring.
4. Devices such as resistance-capacitor, EMC connected to the differential traces, or test points should also be symmetrical.

4. Package Description

GD32L233 series has a total of 6 package types, namely LQFP64, QFN64, WLCSP49, LQFP48, LQFP32 and QFN32.

GD32L235 series has a total of 7 package types, namely LQFP64, QFN64, LQFP48, QFN48, LQFP32, QFN32 and WLCSP25.

Table 4-1. Package Description

Ordering code	Package
GD32L233RxTx	LQFP64(10x10, 0.50pitch)
GD32L233RxO6	QFN64(7x7, 0.35pitch)
GD32L233CCY6	WLCSP49(3x3, 0.40pitch)
GD32L233CxTx	LQFP48(7x7, 0.50pitch)
GD32L233KxT6	LQFP32(7x7, 0.80pitch)
GD32L233KxQ6	QFN32(4x4, 0.40pitch)
GD32L235RxT6	LQFP64(10x10, 0.50pitch)
GD32L235RxO6	QFN64(7x7, 0.35pitch)
GD32L235CxT6	LQFP48(7x7, 0.50pitch)
GD32L235CxO6	QFN48(5x5, 0.35pitch)
GD32L235KxT6	LQFP32(7x7, 0.80pitch)
GD32L235KxQ6/ GD32L235KxQ6P	QFN32(4x4, 0.40pitch)
GD32L235ExY6	WLCSP25(2.092x1.975, 0.35pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.20, 2022
1.1	Update section 2.1.4 to provide all packaging power supply design drawings, explaining the connection of relevant pins within the chip	Jun.21, 2023
1.2	The L233 cores only support SWD debug, so modify 2.7 reference schematic design	Jan.02, 2024
1.3	1. Changed the name to GD32L23x Series Hardware Development Guide, added GD32L235 related content. 2. Figure 2-3. GD32L233 Recommended Power Supply Design added QFN64 and WLCSP49 packaging content.	Apr.09, 2024
1.4	1 Refine the content related to power supply detection and reset, and add section 2.2.	Dec.15, 2024

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