GigaDevice Semiconductor Inc.

GD30SP2200x
OVP Load Switch with Adjustable OVLO

Datasheet

Table of Contents

List of Figures

List of Tables

1 Features

- 2.5V to 30V Wide Input Voltage Range
- Up to 3A output current
- 100μA Low Quiescent Current
- Internal Fixed OVLO threshold 6.8V
- Wide Adjustable OVLO Threshold Range from 4V to 15V
- Low R_{DS_ON} for Internal Switches :50mΩ
- Fast Turn-off Response time when OVP: 450ns
- Over Temperature Protection
- RoHS Compliant and Halogen Free
- Compact Package: DFN8L(2X2)

2 Applications

- True Wireless Stereo (TWS）
- Bluetooth Speaker
- Portable and mobile devices
- Smart phones
- Low voltage peripherals

3 General description

The GD30SP2200x is an Over-Voltage-Protection (OVP) load switch of 50mΩ with adjustable over-voltage-lock-out (OVLO) threshold voltage. The device will turn off the internal MOSFET switch in a fast response of 450ns when the input voltage is over the pre-set OVLO threshold.

When the OVLO is connected to GND, the internal fixed OVLO threshold is set at 6.8V. The OVLO threshold voltage can be adjusted with an external resistor divider and the range is between 4V and 15V. The IC allows a maximum 3A current from IN to OUT. An over temperature protection (OTP) function is implemented internally and monitors the chip temperature to protect the device.

The GD30SP2200x is available in a green small foot print DFN8L(2X2) package.

4 Device overview

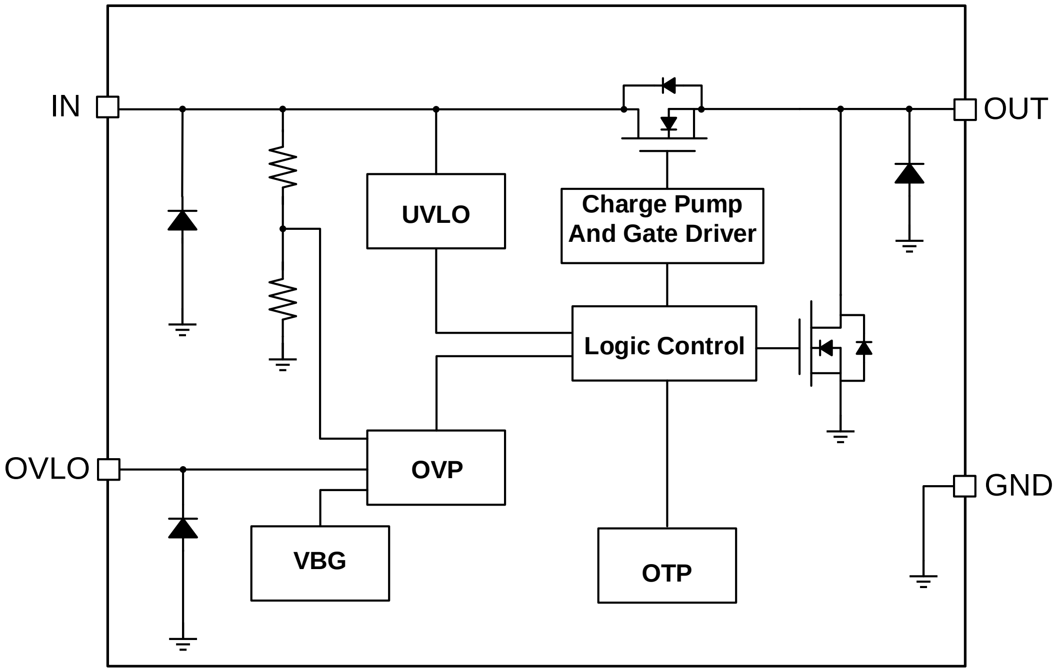
4.1 Device information

Table 4-1 Device Information for GD30SP2200x

Part Number	Package	Function	Description
GD30SP2200x	DFN8L(2X2)	Over-Voltage-Protection	OVP Load Switch with Adjustable OVLO

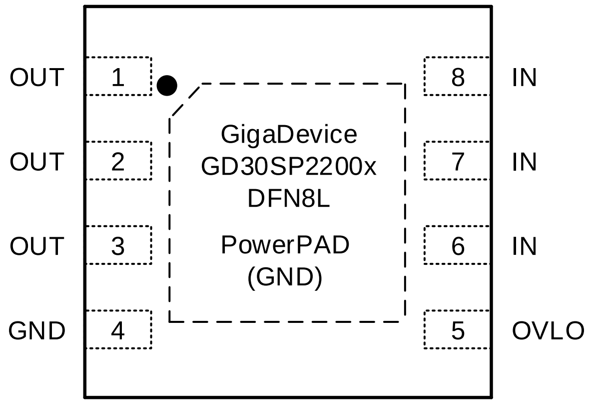
4.2 Block diagram

Figure 4-1 Block diagram for GD30SP2200x



4.3 Pinout and pin assignment

Figure 4-2 GD30SP2200x DFN8L(2X2) pinouts



4.4 Pin definitions

Table 4-2. GD30SP2200x DFN8L(2X2) pin definitions

Pin Name	Pins	Pin Type	Functions description
OUT	1,2,3	O	**Output of the Regulator**. A general 1uF ceramic capacitor should be placed as close as possible to this pin.
GND	4	G	**Ground**. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
OVLO	5	I/O	**OVLO Threshold Set**. Connect a resistor-divider to set different OVLO threshold, V_{OVLO}=1.2x(1+R1/R2) as shown in typical application.
IN	6,7,8	I	**Power Supply Voltage Input**. A general 1uF ceramic capacitor should be placed as close as possible to this pin.
PowerPAD	9	G	**Thermal pad**. connect to ground.

Notes:

(1) Type: I = input, O = output, I/O = input or output, G = Ground.

5 Functional description

5.1 Detailed Description

The GD30SP2200x is placed between the power supply and the low-voltage load to be protected. The device consists of a slew-rate controlled, low resistance OVP switch of typical 50mΩ and over-voltage monitor and protection (OVLO). The device can protect low voltage systems against voltage faults up to 28V. If the input voltage exceeds the OVLO threshold, the internal switch is turned off to prevent damage to downstream components. A 16ms de-bounce time is built into the device to prevent false turn-on of the internal switch during startup.

In normal operation the OVP switch acts as a slew-rate controlled load switch, connecting and disconnecting the power supply from IN to OUT. A low resistance N-channel MOSFET is utilized to minimize the voltage drop between the voltage source and the load and to reduce power dissipation. When the input voltage is over the programmed OVLO threshold, the device turns off the internal switch in a fast response of 450ns and disconnects the load from the abnormal input, preventing damage to downstream components.

Other protection features implemented in the device include over temperature protection. In the event that the power dissipation causes the IC temperature to exceed its maximum temperature setting, the GD30SP2200x will turn off.

5.1.1 Internal Switch

The GD30SP2200x incorporate an internal N-MOSFET with a 50mΩ (TYP) R_{ON}. The MOSFET is driven by an integrated charge pump which generates the necessary voltage above IN.

5.1.2 OVLO threshold

The GD30SP2200x has a 1.2V over-voltage trip reference on the OVLO pin. With a resistor-divider on OVLO pin from IN to GND, the over-voltage protection point of IN can be programmed between 4V and 15V. Fixed OVLO threshold is set with an internal resistor-divider providing a 6.8V-threshold. To activate the internal fixed OVP, the OVLO pin should be connected to GND.

5.1.3 Protection features

To avoid mis-operation of the device at low input voltages, the GD30SP2200x shuts down at voltages lower than V_{UVLO} with V_{UVLO_HYS} hysteresis.

The GD30SP2200x enters thermal shutdown once the junction temperature exceeds typically T_{OT}. Once the device temperature falls below the threshold with hysteresis, the device returns to normal operation automatically.

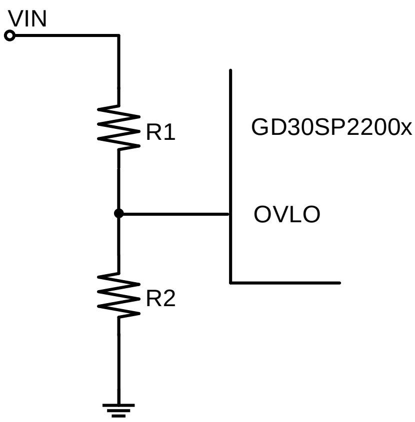
5.2 Application information

5.2.1 OVLO threshold set up

If OVLO is connected to ground, the internal OVLO comparator uses the internally set OVLO value. Once the OVLO pin voltage exceeds the OVLO select voltage, V_{OVLO_SELECT}, an external resistor divider is used to set the OVLO threshold. By selecting R1 and R2, the OVLO voltage is programmed to the desired value.

$$V_{OVLO} = 1.2 \times (1 + \frac{R_1}{R_2})$$

Figure 5-1 Feedback resistor divider



Note1: R1 and R2 are only required for external ovp, otherwise connect OVLO to GND
Note2: Recommend 10K≤R2≤50K; add unidirection TVS close to VIN

5.2.2 Input capacitor selection

A 1µF or larger capacitor is typically recommended for C_{IN}. C_{IN} should be located close to the device IN pin. Ceramic capacitors are recommended for C_{IN}. Select capacitors with a voltage rating at least 5V higher than the maximum possible voltage during surge. The 50V- rated capacitors are ideal for most applications.

5.2.3 Output capacitor selection

In order to ensure stability while the current limit is active, a small output capacitance of approximately 1µF is required at the output. The output capacitor has no specific capacitor ESR requirement. If desired, C_{OUT} may be increased to accommodate any load transient condition.

6 Electrical characteristics

6.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 6-1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{IN}	Power supply pin	-0.3	30	V
V_{OUT}	Output	-0.3	V_{IN}+0.3	V
V_{OVLO}	OVLO trip voltage setting	-0.3	17	V
I_{IN}	Continuous current	—	3	A
Thermal characteristics				
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C
P_{max}	Maximum power dissipation @T_A=25°C	—	0.5	W

6.2 Recommended operation conditions

Table 6-2 Recommended operation conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Power supply pin	2.5	—	28	V
V_{OVLO}	OVLO trip	0	—	5	V
Thermal characteristics					
T_A	Operating ambient temperature	–40	—	85	°C
T_J	Operating junction temperature	–40	—	125	°C

6.3 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on I-test methods.

Table 6-3 Electrostatic Discharge and Latch-up characteristics

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; JS-001-2017	±4000	V

$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; JS-002-2018	±2000	V
Latch up	I-test	T_A = 25 °C; JESD78E	200	mA

6.4 Power supplies voltages and currents

Table 6-4 Power supplies voltages and currents

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_Q	Quiescent current	V_{IN} = 5V, No switching, T_J =25°C	—	100	—	µA
t_{OVP}	OVP Turn-off time	V_{IN} > V_{OVLO}, C_{IN}=C_L=0pF	—	450	—	ns
V_{OVLO_TH}	Over voltage lockout reference	—	1.17	1.2	1.23	V
V_{OVLO_HYS}	Over voltage lockout reference hysteresis	—	—	35	—	mV
V_{OVLO}	Range of OVLO threshold	—	4	—	15	V
I_{IN}	Maximum through current	—	—	—	3	A
R_{ON}	Internal switch ON resistance	V_{IN} = 5V, I_{OUT}=1A	—	50	—	mΩ
t_{ON}	Turn-on time	V_{IN}>V_{UVLO} to V_{OUT}=V_{IN}*90% C_L=0	—	16	—	ms
V_{UVLO}	VIN under voltage lockout	V_{IN} rising	—	2.25	2.37	V
V_{UVLO_HYS}	VIN under voltage lockout hysteresis	V_{IN} rising to falling threshold	—	250	—	mV
V_{OVLO_SELECT}	External OVLO select Threshold	—	—	0.25	—	V

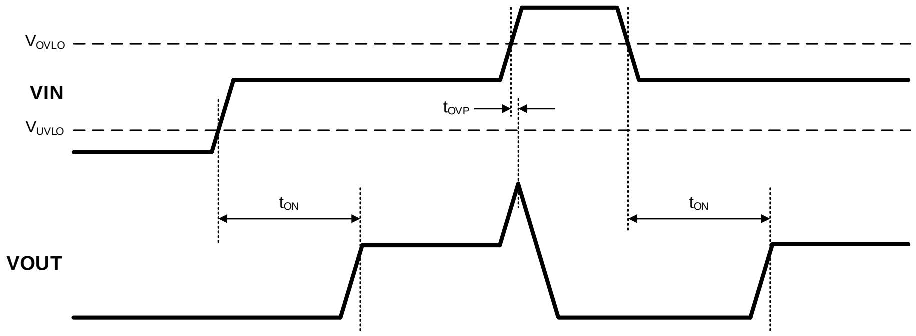
6.5 Protections

Table 6-5 Over temperature characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{OT}	Thermal shutdown temperature	Die temperature, T_J	135	150	165	°C
T_{HYS}	Thermal hysteresis	Die temperature, T_J	—	20	—	°C

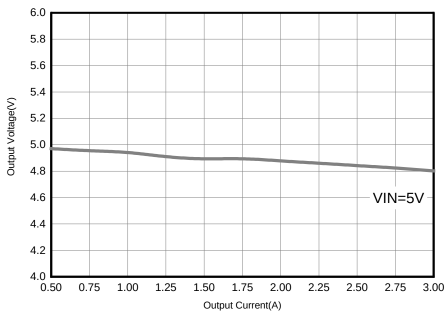
6.6 Timing Diagram

Figure 6-1 Timing Diagram

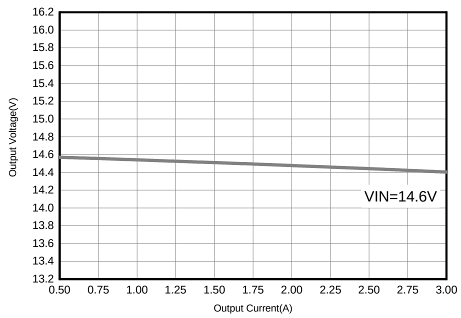


6.7 Typical Characteristics

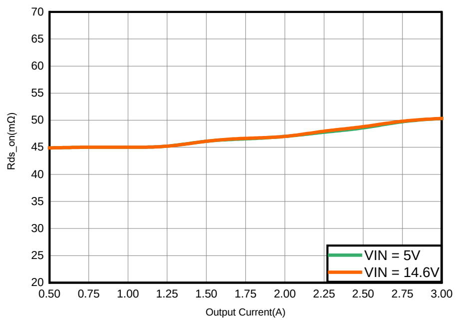
TA = +25°C, V_{IN} = 5V, C_{IN} = 1μF and C_{OUT} = 1μF, unless otherwise specified.



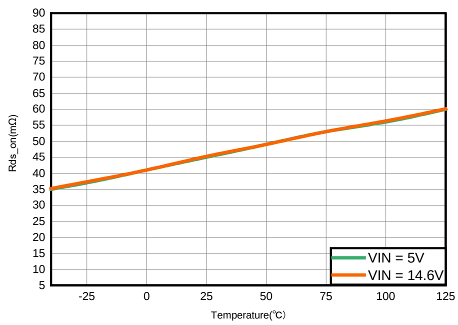
Output Voltage vs. Output Current by V_{IN} = 5V



Output Voltage vs. Output Current by V_{IN} = 14.6V



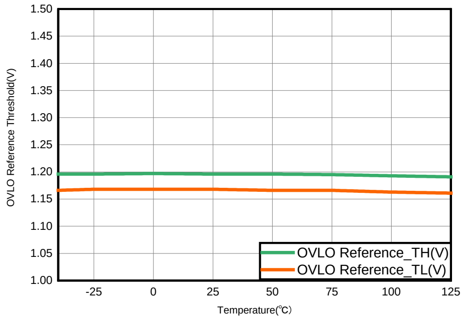
R_{DS_ON} Resistance vs. Load Current



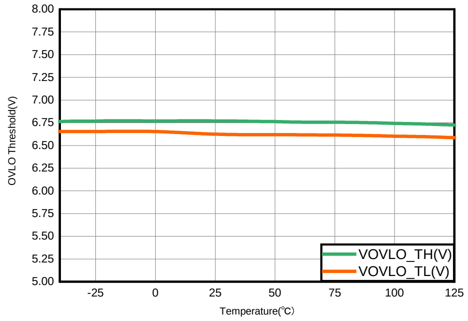
R_{DS_ON} Resistance vs. Temperature

Typical Characteristics

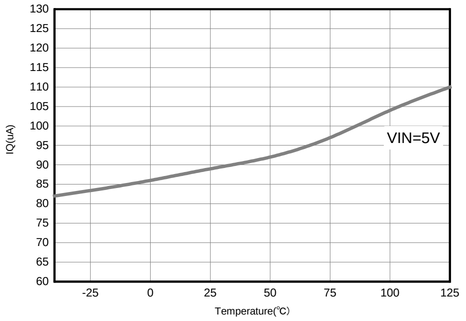
TA = +25°C, V_{IN} = 5V, C_{IN} = 1μF and C_{OUT} = 1μF, unless otherwise specified.



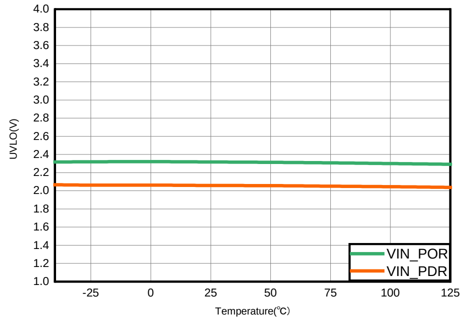
OVLO Reference Threshold vs. Temperature



OVLO Threshold vs. Load Current



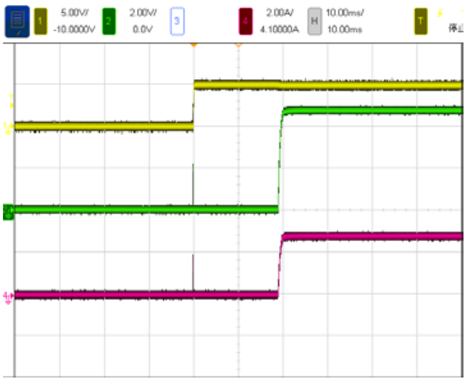
Quiescent Current vs. Temperature



UVLO vs. Temperature

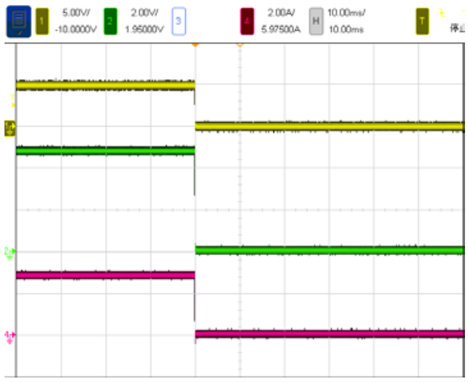
Typical Characteristics

TA = +25°C, V_{IN} = 5V, C_{IN} = 1μF and C_{OUT} = 1μF, unless otherwise specified.



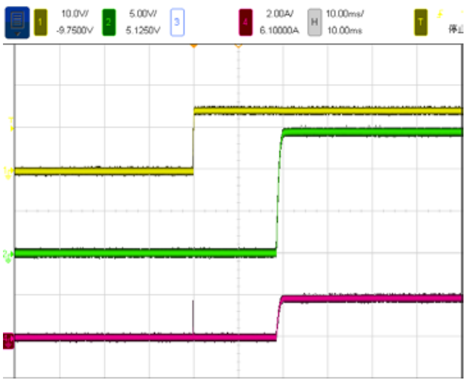
CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

Power On by V_{IN} = 5V, IOUT = 3A



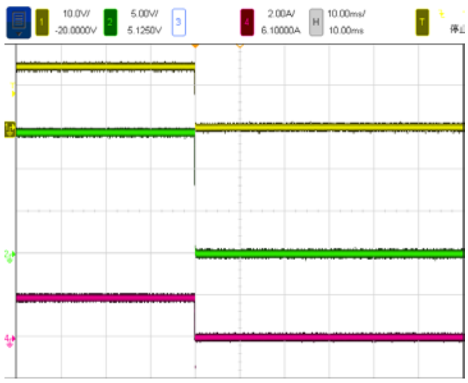
CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

Power Off by V_{IN} = 5V, IOUT = 3A



CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

Power On by V_{IN} = 14.6V, IOUT = 2A

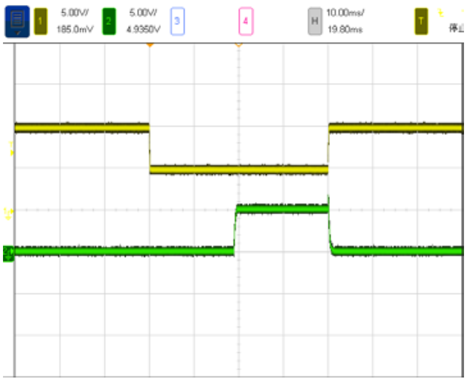


CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

Power Off by V_{IN} = 14.6V, IOUT = 2A

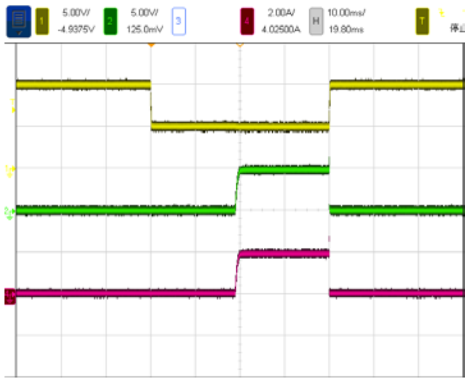
Typical Characteristics

TA = +25°C, V_{IN} = 5V, C_{IN} = 1μF and C_{OUT} = 1μF, unless otherwise specified.



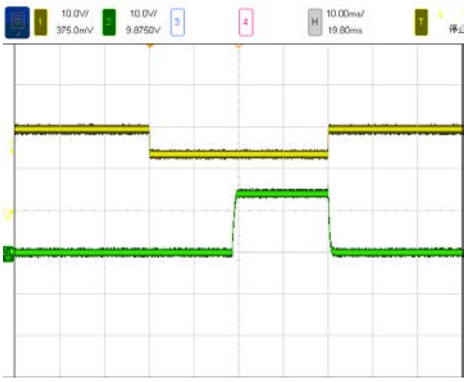
CH1 = V_{IN}, CH2 = V_{OUT}

OVP and OVP Recovery by OVP = 6.8V, IOUT = 0A



CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

OVP and OVP Recovery by OVP = 6.8V, IOUT = 2A



CH1 = V_{IN}, CH2 = V_{OUT}

OVP and OVP Recovery by OVP = 16V, IOUT = 0A

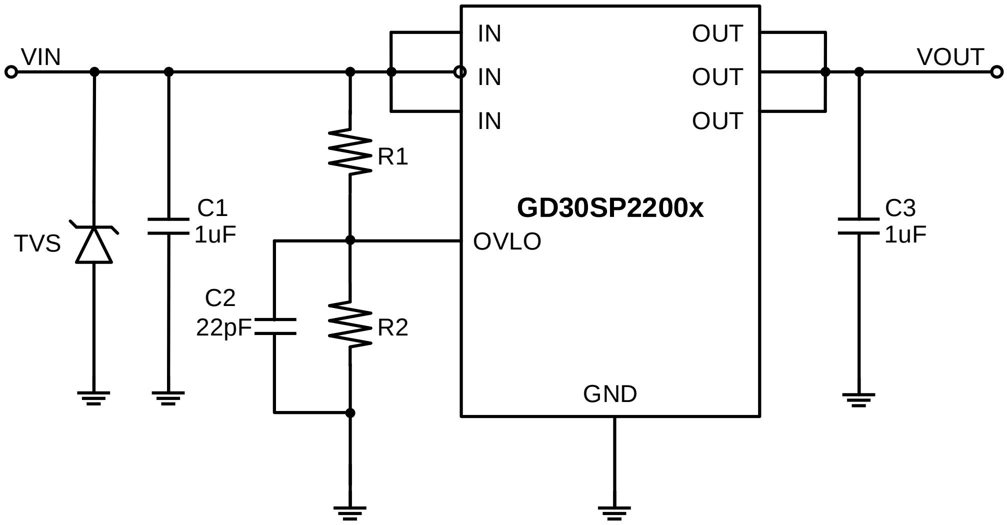
CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

OVP and OVP Recovery by OVP = 16V, IOUT = 2A

7 Typical application circuit

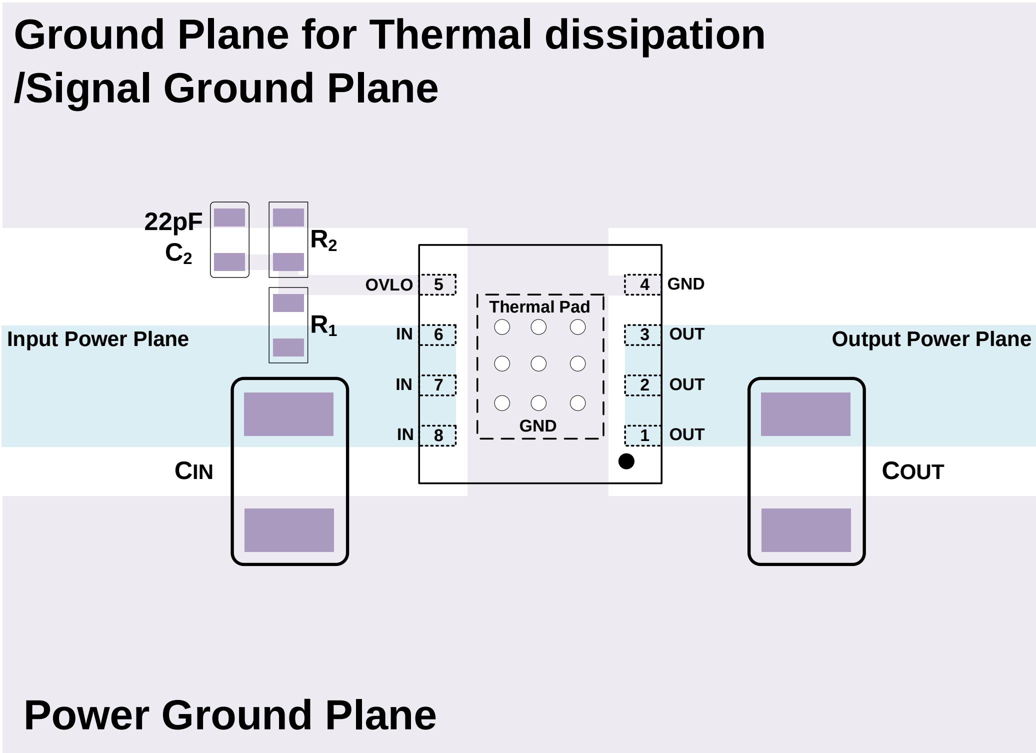
Figure 7-1 Typical GD30SP2200x Application Circuit

The over-voltage protection with external OVLO Threshold setting.



8 Layout guideline

To make fully use of the performance of GD30SP2200x, the guidelines below should be followed.



1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the GD30SP2200x) and close to IN pin, and place the output capacitor C_{OUT} on the top layer(same layer as the GD30SP2200x) and close to OUT pin.

2. IN pin routing passes through the external TVS firstly, and then connect GD30SP2200x.

3. If R1 and R2 are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.

9 Package information

9.1 DFN8L(2X2) package outline dimensions

Figure 9-1 DFN8L(2X2) package outline

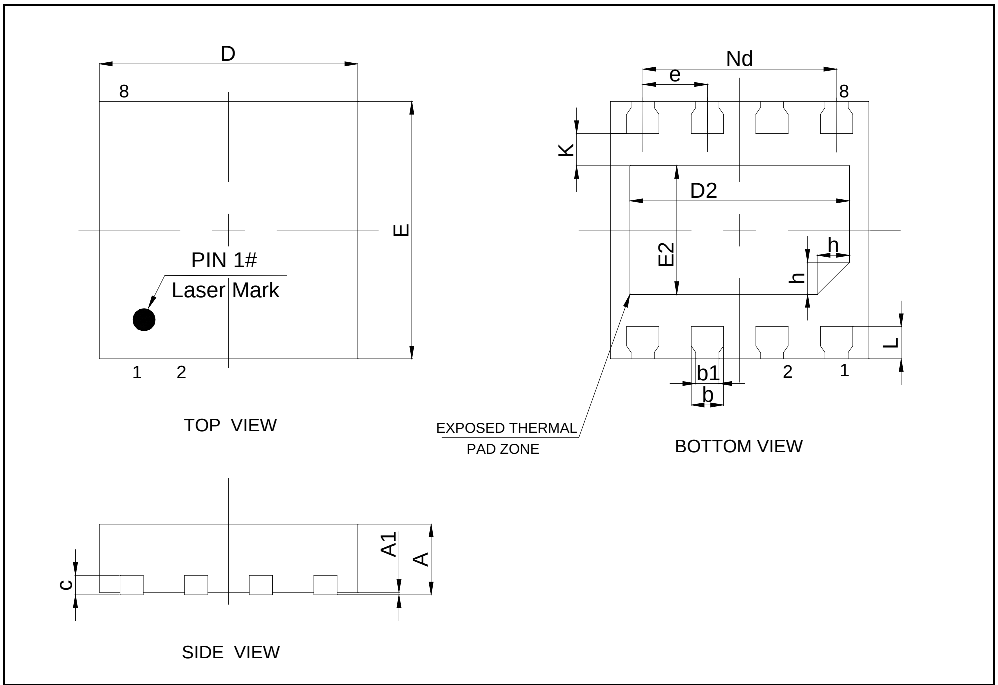
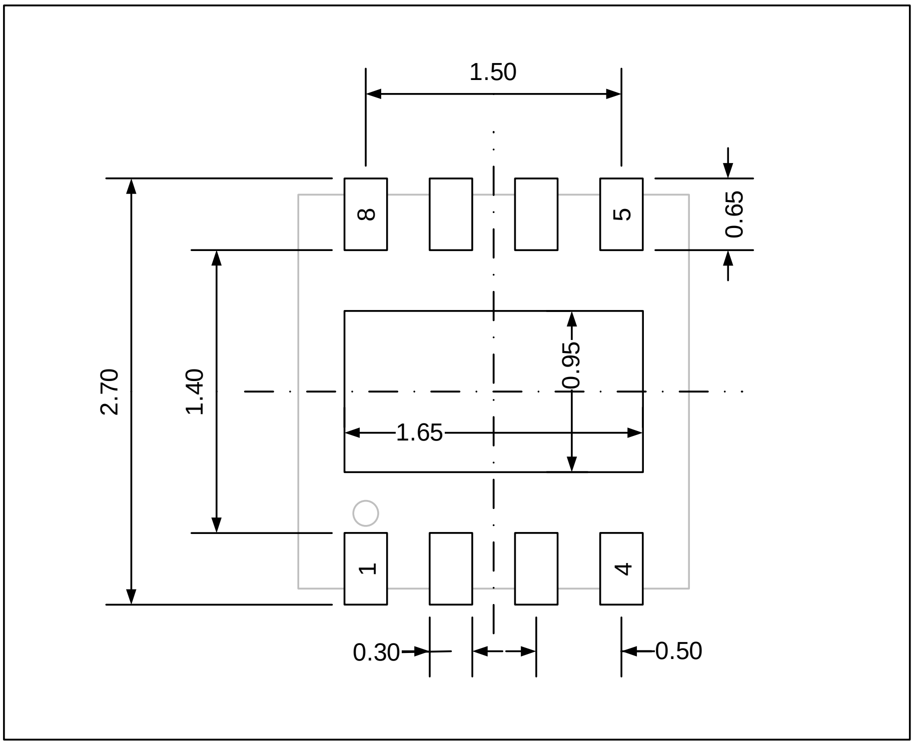


Table 9-1 DFN8L(2X2) package dimensions (in mm)

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	—	0.18	—
c	—	0.152	—
D	1.90	2.00	2.10
D2	1.60	1.70	1.80
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e	—	0.50	—
h	0.20	0.25	0.30
K	—	0.25	—
L	0.20	0.25	0.30
Nd	—	1.50	—

Figure 9-2 DFN8L(2X2) recommended footprint



(Original dimensions are in millimeters)

9.2 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "Θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$\Theta_{JA} = (T_J - T_A)/P_D$

$\Theta_{JB} = (T_J - T_B)/P_D$

$\Theta_{JC} = (T_J - T_C)/P_D$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

Θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 9-2 Package Thermal Characteristics[1]

Symbol	Condition	Package	Value	Unit
Θ_{JA}	Natural convection, 2S2P PCB	DFN8L	86.45	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	DFN8L	36.25	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	DFN8L	47.13	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	DFN8L	36.20	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	DFN8L	3.61	°C/W

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

(2) The PCB board is JEDEC standard 2S2P FR-4 PCB board, the PCB Dimension(LXM) 114.3X76.2mm, the PCB thickness 1.6mm, 1oz copper.

(3) Power dissipation is calculated by $P_D = (V_{IN}-V_{OUT}) \times I_{OUT}$.

10 Ordering information

Table 10-1 Part order code for GD30SP2200x devices

Ordering Code	Package	Package Type	Packing Type	MOQ	Temperature Operating Range
GD30SP2200WFTR	DFN8L(2X2)	Green	Tape&Reel	3000	Industrial -40°C to +85°C

11 Revision history

Table 11-1 Revision history

Revision No.	Description	Date
1.0	Initial Release	Aug.15, 2022

Important Notice