GigaDevice Semiconductor Inc.

EMC Application Guideline of GD32MCU

Application Note
AN062

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1. Introduction

With the shrinking of the semiconductor process and the improvement of performance, the MCU faces a more complex electromagnetic environment. In other words, the immunity to noise and external electromagnetic radiation will also be more complicated. This paper introduces the principles and characteristics of EMC specifically for GD32 MCU products, and provides recommendations based on experience gained in various applications.

2. Definitions

2.1. EMC

Electromagnetic compatibility (EMC) is the ability of the system to work completely (no performance degradation). In a normal environment, EMC requires that the device or system is not disturbed by the surrounding electromagnetic field and does not produce electromagnetic interference to affect other devices.

2.2. EMS

Electromagnetic susceptibility (EMS) is the anti-interference ability of equipment or systems to noise interference. The higher the EMS level, the better the immunity of the equipment; on the contrary, the equipment with the lower EMS level is extremely sensitive to the electromagnetic environment, and its working state is affected by the surrounding electromagnetic environment. (So many places translate electromagnetic susceptibility to electromagnetic sensitivity, but considering that "susceptibility" is not the same as "sensitivity", we will use electromagnetic susceptibility).

EMS mainly consists of electrical fast transient/burst immunity and system-level ESD. The measurement is used to determine the reliability level of the device when operating in a less-than-ideal electromagnetic environment.

2.3. EMI

Electromagnetic interference (EMI) refers to the level of electromagnetic waves emitted from the equipment as the source of interference to the surrounding environment. The emitted electromagnetic waves are divided into conducted emissions and radiated emissions. Conducted emissions propagate along cables or interconnecting lines, while radiated emissions propagate through free space.

2.4. EMS&EMI Testing Standard

Table 2-1.Standard form of the International Electrotechnical Commission

Standard	Description
IEC61000-4-2	Electrostatic Discharge (ESD) Immunity Test
IEC61000-4-4	Electrical Fast Transient (EFT) Burst Immunity Test
IEC61967-2	Measurement of radiated emission-TEM cell and wideband TEM cell method

According to IEC62132-1, system-level ESD and EFT for MCU can be divided into five categories of failure modes. Among them, grade A is no problem, B/C/D is soft failure, and E is hard failure.

Table 2-2. Classification of MCU Performance Degradation

Class	Description
A	All functions of the IC perform as designed during and after exposure to a disturbance.
B	All functions of the IC perform as designed during exposure, however, one or more of them may go beyond the specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain in class A.
C	A function of the IC doesn't perform as designed during exposure but returns automatically to normal operation after exposure is removed.
D	A function of the IC doesn't perform as designed during exposure and doesn't return to normal operation until exposure is removed and the IC is reset by simple operator action (e.g.: put off supply...).
E	One or more functions of an integrated circuit do not perform as designed during and after exposure and cannot be returned to proper operation.

3. EMS characterization of MCU

3.1. EMS-Electromagnetic susceptibility

EMS mainly consists of electrical fast transient/burst immunity and system-level electrostatic discharge ESD.The EMC characteristics in the GD32MCU Datasheet include system-level EMS Electromagnetic susceptibility and absolute electrical sensitivity test results.

Figure 3-1. The representation of EMS parameters in the datasheet

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the ***Table 4-9. EMS characteristics***(1), based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-9. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = + 25 °C LQFP144, f_{HCLK} = 120 MHz conforms to IEC 61000-4-2	3A
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 3.3 V, T_A = +25 °C LQFP144, f_{HCLK} = 120 MHz conforms to IEC 61000-4-4	4A

(1) Based on characterization, not tested in production.

The system-level EMS test is to run the system robustness of the GD32MCU in the power-on test application in the smallest system. The program logic is to switch the running lights through two LEDs to indicate normal operation. By applying system-level ESD or EFT to the running MCU, the system is monitored in real time during the disturbance test to determine whether there will be soft failures (systematic disturbances) as well as hard failures.

Absolute electrical sensitivity includes component-level ESD (HBM/CDM) and LU. Component-level ESD (HBM/CDM) and LU are tested on unpowered devices, and MCU pin function and integrity are checked by FT test after interference test.

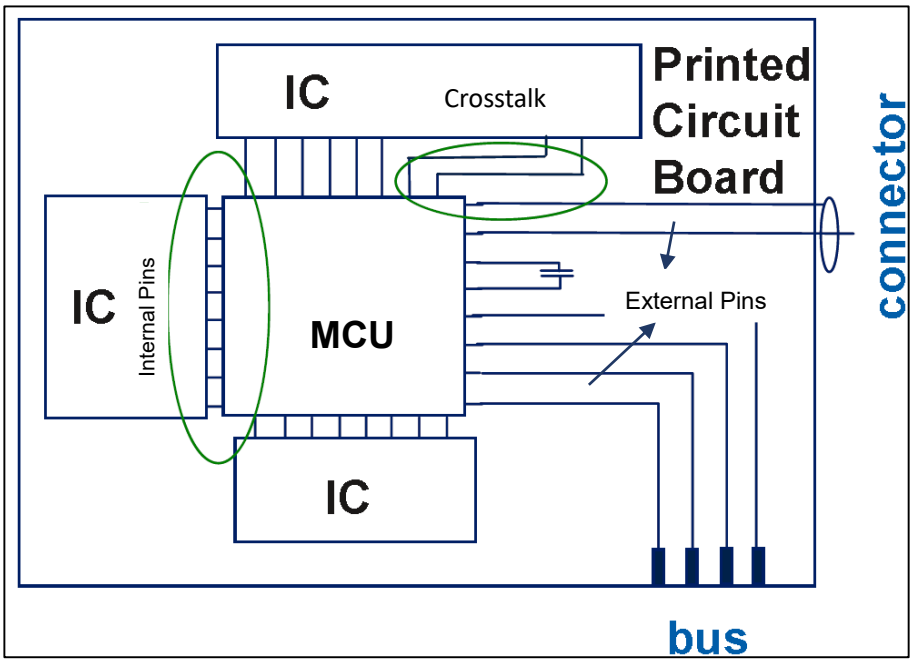
3.2. System level ESD test IEC61000-4-2

All GD32 series MCUs will carry out this test. By applying positive/negative voltages for each level 10 times to the test pins, the test levels are tested sequentially from low to high until an abnormal phenomenon occurs. This allows for internal fault investigation of the chip and does not provide further application protection circuitry for protecting the MCU's sensitive pins from ESD.

The two test pins can cover 5VT and non-5VT pins, and they are located in the middle of the

distribution of the two power pins (VDD and GND). In addition, the test pins will try to select external pins. As the control core, MCU inevitably needs to be connected to external ports, and the risk of introducing ESD to external connectors or buses is high. We define the pins directly connected between the MCU and the outside of the system as external pins. In addition, the layout traces and the pin traces adjacent to the external pin traces are also at risk of interference. Other pins of the MCU that are not led out of the system and are not at risk of crosstalk from external pins are called internal pins. Generally, internal pins are less exposed to system-level ESD risks. Therefore, in protecting system-level ESD, external pin protection is critical. The screenshot is shown in ***Figure 3-2. External and Internal Pins***.

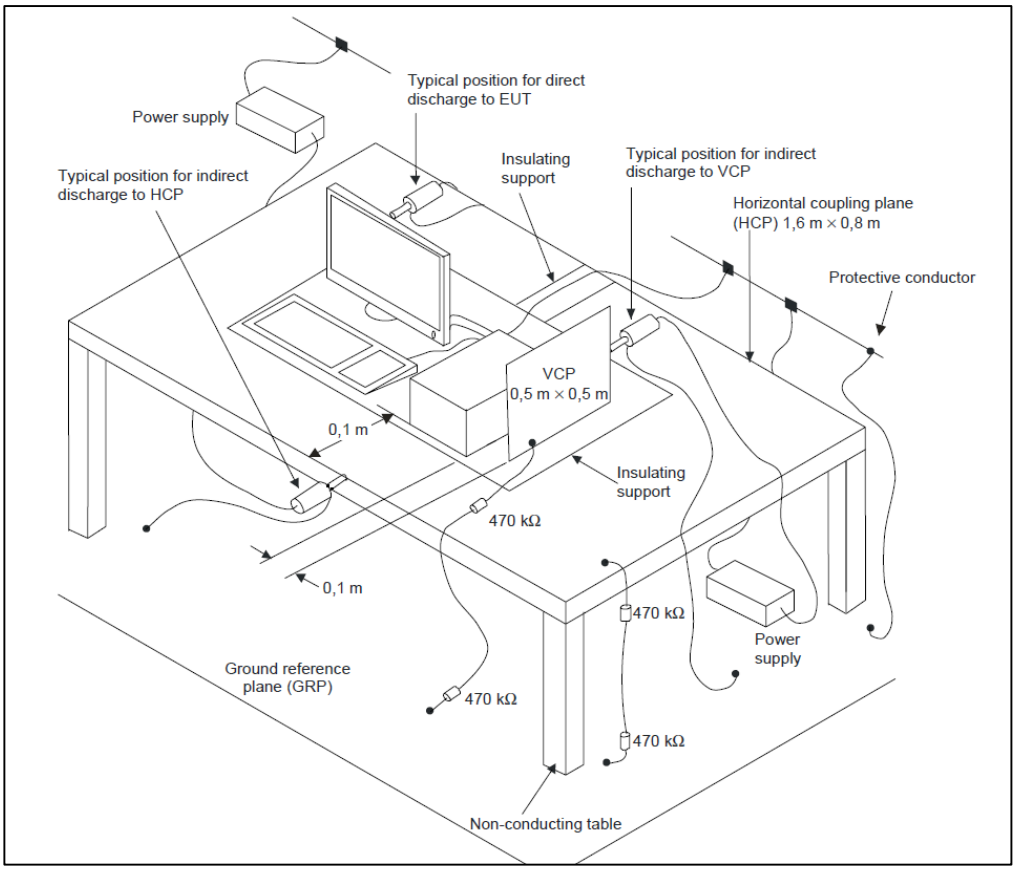
Figure 3-2. External and Internal Pins



3.2.1. Equipment of system level ESD

The device used to perform system-level ESD verification is an IEC 61000-4-2 compliant ESD generator. The discharge is applied directly to the test pins of the MCU. Both contact mode and air mode are tested. The test level is from low to high, and positive and negative voltages are applied to each level of static electricity >= 10pcs until the operation of the system is abnormal. ESD console layout and grounding requirements are shown in ***Figure 3-3. IEC61000-4-2 console layout and grounding requirements***.

Figure 3-3. IEC61000-4-2 console layout and grounding requirements



3.2.2. Target level of system level ESD

The system-level ESD test mode can be divided into contact mode (CD) and air mode (AD). In the contact mode, the tip of the ESD gun touches the metal part of the EUT for electrostatic discharge; while the air mode uses the ESD round head to the gap between the EUT; screen and buttons and other non-metals to discharge static electricity. Both CD and AD belong to the direct contact test, in addition to the indirect contact test, that is, the electrostatic gun discharges static electricity to the horizontal coupling plate and the vertical coupling plate, and the coupling plate indirectly radiates ESD to the EUT.

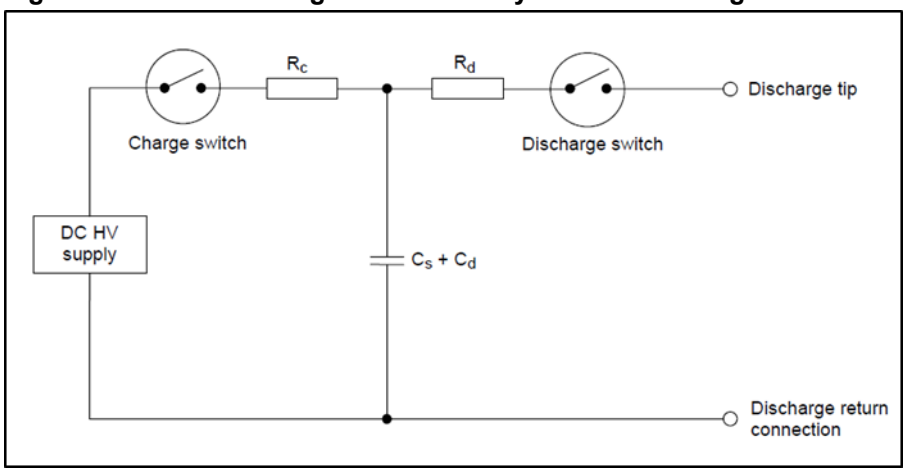
Table 3-1.System-level ESD levels

Contact discharge		Air discharge	
Level	Test voltage (kV)	Level	Test voltage (kV)
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
x [a]	Special	x [a]	Special
a "x" can be any level, above, below or in between the others. The level shall be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment may be needed.			

3.2.3. Waveform of system level ESD

The ideal discharge model for a system-level ESD generator is as follows:

Figure 3-4. Ideal discharge model for a system-level ESD generator



Typical value for Cs+Cd is 150pF, typical value for Rd is 330 ohms

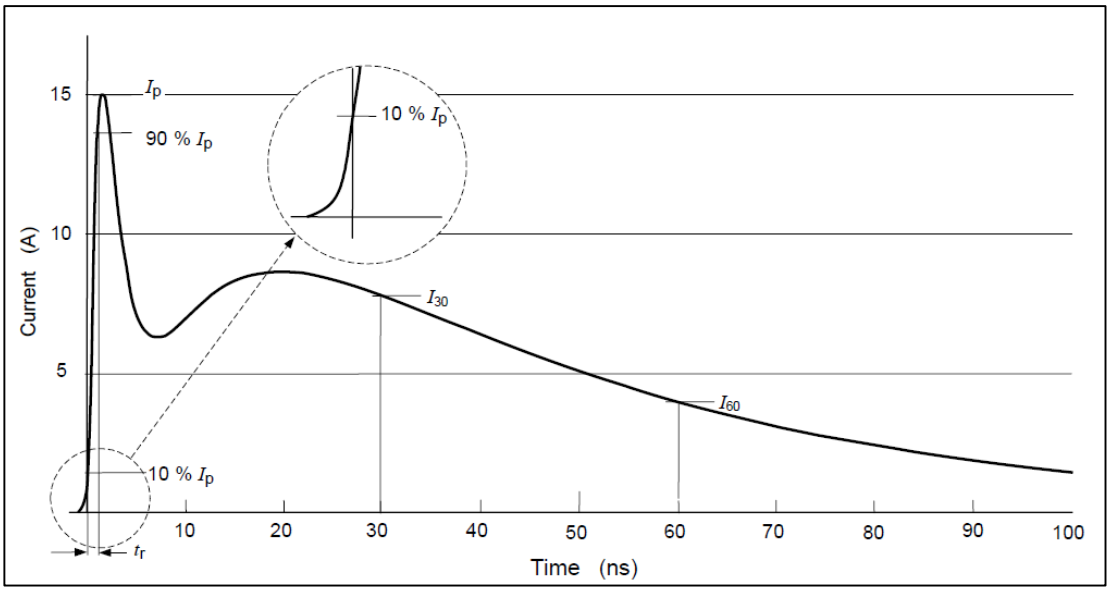
The current waveform parameters of contact discharge are as follows:

Figure 3-5. System-level ESD contact discharge current waveform parameters

Level	Indicated voltage kV	First peak current of discharge ±15 % A	Rise time t_r (±25 %) ns	Current (±30 %) at 30 ns A	Current (±30 %) at 60 ns A
1	2	7,5	0,8	4	2
2	4	15	0,8	8	4
3	6	22,5	0,8	12	6
4	8	30	0,8	16	8
The reference point for measuring the time for the current at 30 ns and 60 ns is the instant when the current first reaches 10 % of the 1st peak of the discharge current. NOTE The rise time, t_r, is the time interval between 10 % and 90 % value of 1st peak current.					

The ideal current waveform of 4kV contact discharge is as follows:

Figure 3-6. Ideal contact discharge current waveform at 4 kV



3.3. EFT Electrical Fast Transient Immunity Test IEC61000-4-2

When inductive loads (such as relays/motors/encoders) are de-energized, short-duration high-frequency transient pulses are generated on the power distribution system. When the power supply is connected or pulled out, it will also generate an instantaneous sudden change pulse. A common cause of power line transients is electrical sparks, which can occur whenever an AC power line is plugged in, or when equipment is turned off, or circuit breakers are opened or closed. Transient noise from the power system can be coupled to the end equipment through the power lines.

IEC61000-4-4 specifies test voltage waveforms used to simulate transients caused by switching inductive loads on AC power lines, this specification also defines immunity requirements for repetitive electrical fast transients, and The test method required by the system.

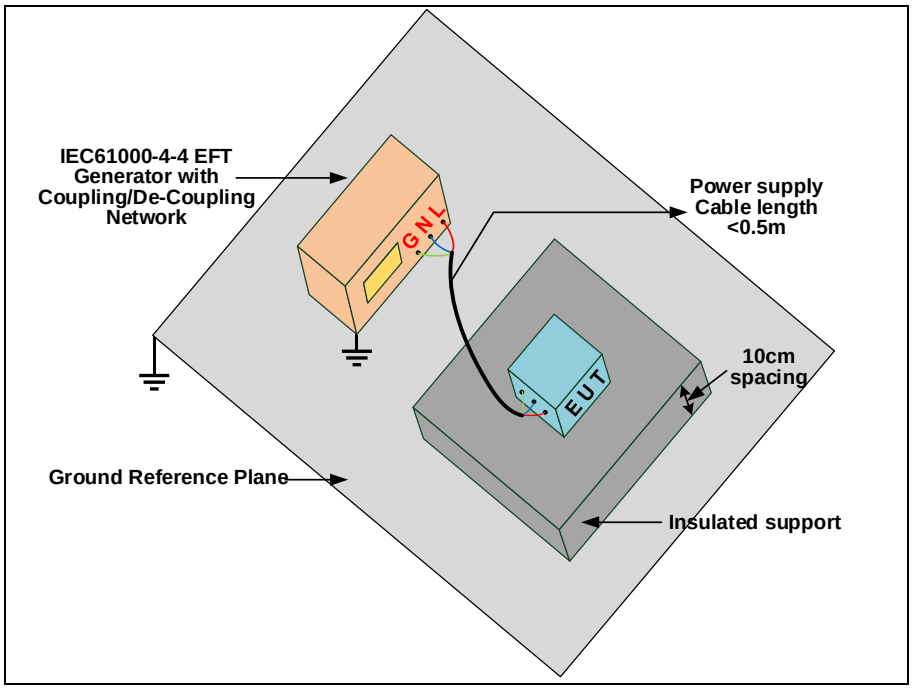
Manufacturers use EFT waveforms as defined by the IEC 61000-4-4 standard in order to test device performance after fast transients. This test primarily involves EFT pulses being injected into the equipment's power supply lines, signal lines, control lines, and ground connections in order to simulate the coupling of transient noise on these lines. The pulse waveform has the characteristics of high amplitude (0.5 ~ 4 kV), short rise time, high repetition rate and low energy.

Several international standards exist that specify requirements for the transient immunity performance of specific types of equipment. For example, the European Union's EN 55024 describes testing requirements and performance standards for information technology equipment. IEC 61547 specifies testing requirements and performance standards for lighting equipment. The requirements and test methods for all of these standards are derived from

IEC 61000-4-4.

3.3.1. Equipment of EFT

Figure 3-7. IEC 61000-4-2 Operator Station and Layout Environment



The EFT test of GD32MCU adopts the same test board as ESD. The DC current source is connected to the EFT generator coupling front end, and the power line is applied to the MCU after passing through the coupling network. 5kHz and 100kHz repetition frequency/positive and negative voltage/synchronous injection and L1/N/L1+N coupling methods of asynchronous injection are all tested for interference, from low to high. Each level is tested, and each level is tested for at least 60s.

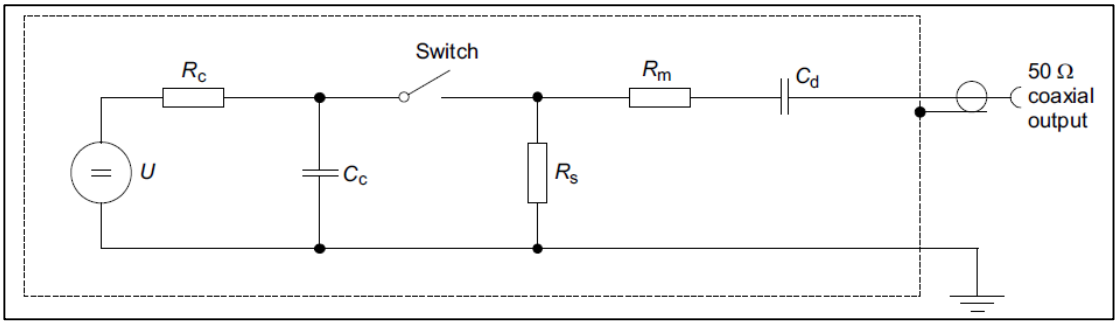
3.3.2. Target level of EFT

Table 3-2. EFT test levels

Open circuit output test voltage and repetition frequency of the impulses				
Level	Power ports, earth port (PE)		Signal and control ports	
	Voltage peak kV	Repetition frequency kHz	Voltage peak kV	Repetition frequency kHz
1	0,5	5 or 100	0,25	5 or 100
2	1	5 or 100	0,5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X [a]	Special	Special	Special	Special
The use of 5 kHz repetition frequency is traditional, however, 100 kHz is closer to reality. Product committees should determine which frequencies are relevant for specific products or product types. With some products, there may be no clear distinction between power ports and signal ports, in which case it is up to product committees to make this determination for test purposes.				
[a] "X" can be any level, above, below or in between the others. The level shall be specified in the dedicated equipment specification.				

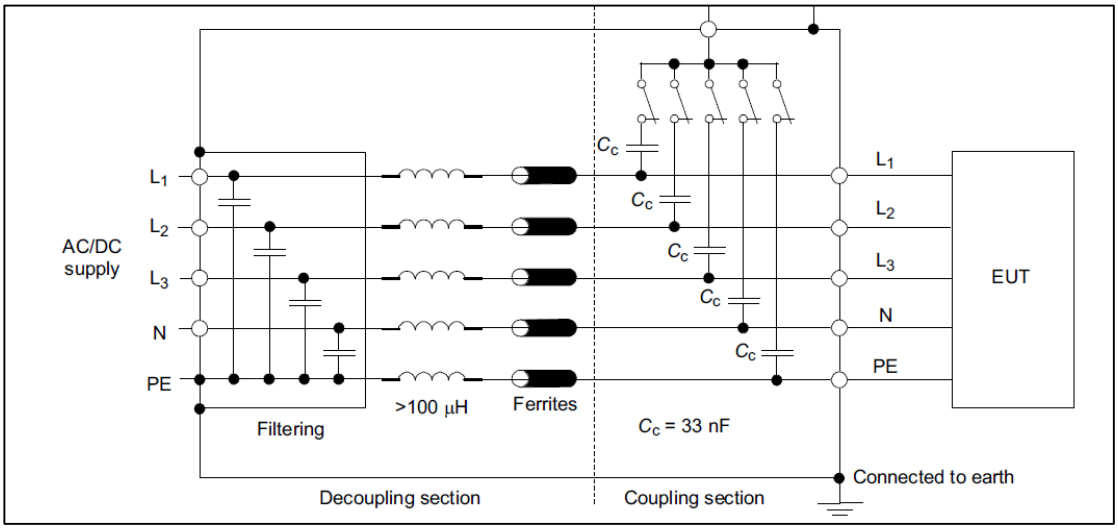
3.3.3. Waveform of EFT

Figure 3-8. Ideal discharge model for EFT generator



U high-voltage source
Rc charging resistor
Cc energy storage capacitor
Rs impulse duration shaping resistor
Rm impedance matching resistor
Cd DC blocking capacitor
Switch high-voltage switch

Figure 3-9. EFT Generator Decoupling Network Model



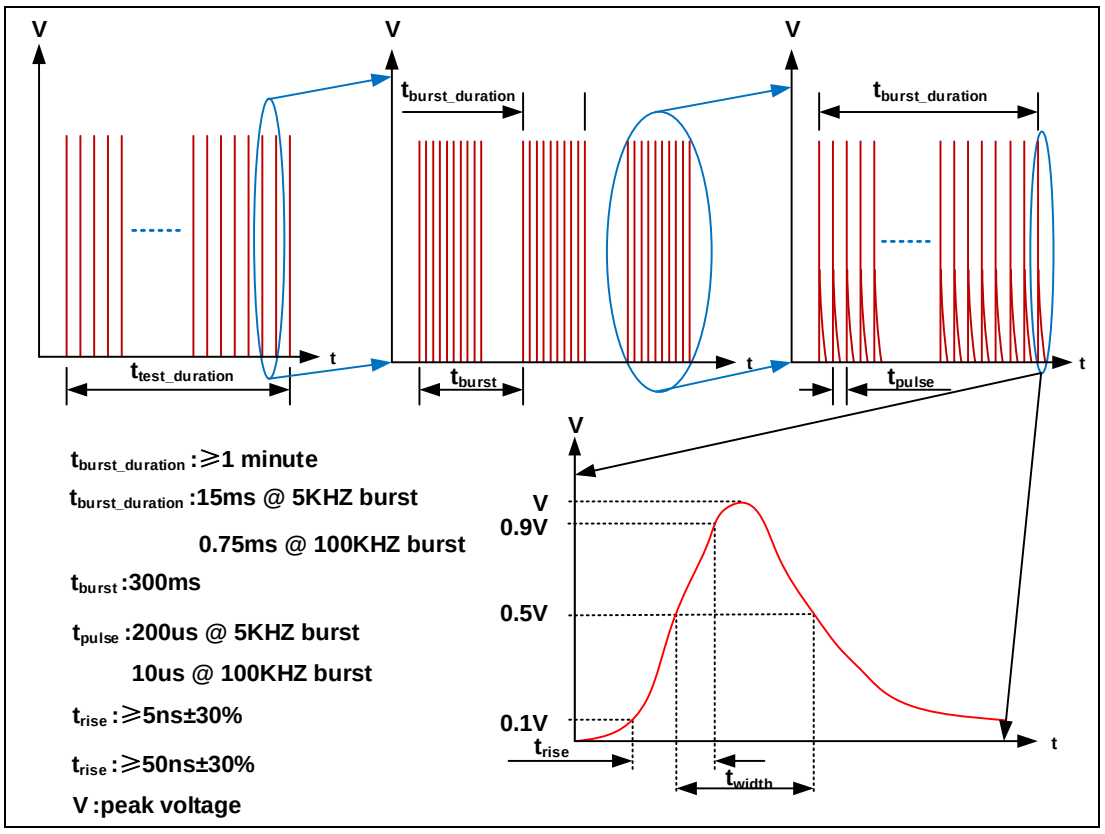
L1, L2, L3, phases

N neutral

PE protective earth

Cc coupling capacitors

Figure 3-10. EFT Burst Waveform Parameters



4. Electrical sensitivity

Discharges generated during manual operation can cause irreversible damage to integrated circuits, while discharges during automatic mechanical operation can destroy more integrated circuits. There are differences in how component-level ESD discharges integrated circuits or system equipment, and the reasons for this are also different. According to the different discharge conditions, the ESD discharge models are mainly divided into three types, the human body model ESD (ESD-HBM), the charge device model ESD(ESD-CDM), and the machine model ESD (ESD-MM).

The fault characteristics we are usually interested in are junction leakage, short circuit, gate oxide breakdown, thermal damage, etc. At present, all the test instruments have complete protective measures for MM model, so the risk of MM model occurrence has been relatively small. MCU GD32 Each series of products will test HBM and CDM, and are marked on Datasheet.

The purpose of the component-level ESD test is to test the antistatic performance of the chip in the process of cutting, packaging, pre-delivery testing, transportation, and PCB assembly and placement of the chip. Component-level ESD occurs in the ESD protection area (EPA) is not powered on. The system-level ESD test is to measure the complex electrostatic environment that the chip faces in actual use, not the ESD-controlled area, and most of the MCU power-on systems are in the running process.

The absolute electrical sensitivity test results in GD32MCU datasheet such as in***Figure 4-1. The way absolute electrical parameters are represented in the datasheet***

Figure 4-1. The way absolute electrical parameters are represented in the datasheet

Table 4-12. ESD characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; ESDA/JEDEC JS-001-2017	—	—	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; ESDA/JEDEC JS-002-2018	—	—	500	V

(1) Based on characterization, not tested in production.
(2) There is space for adjustment, it will be tested soon.

Table 4-13. Static latch-up characteristics (1)

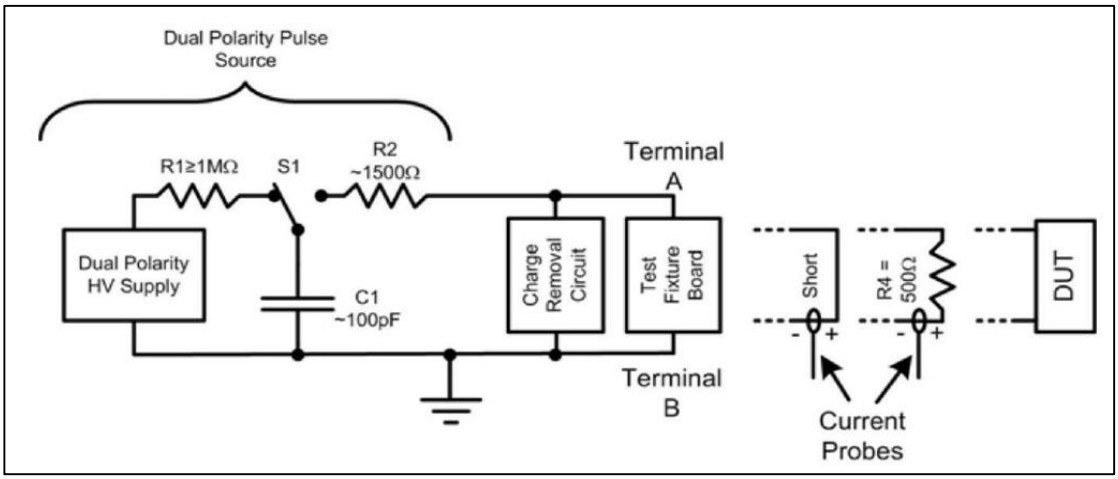
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A = 25 °C; JESD78E	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

(1) Based on characterization, not tested in production.
(2) There is space for adjustment, it will be tested soon.

4.1. Component level ESD HBM Human Body Mode

The HBM ESD pulse simulates the direct transfer of static electricity from the human body to the device under test. The 100pF capacitor is discharged through the switching element and the 1.5kΩ series resistor. This is by far the most used industry model for classifying devices for ESD susceptibility. This test meets the ESDA/JEDEC JS-001-2017 standard.

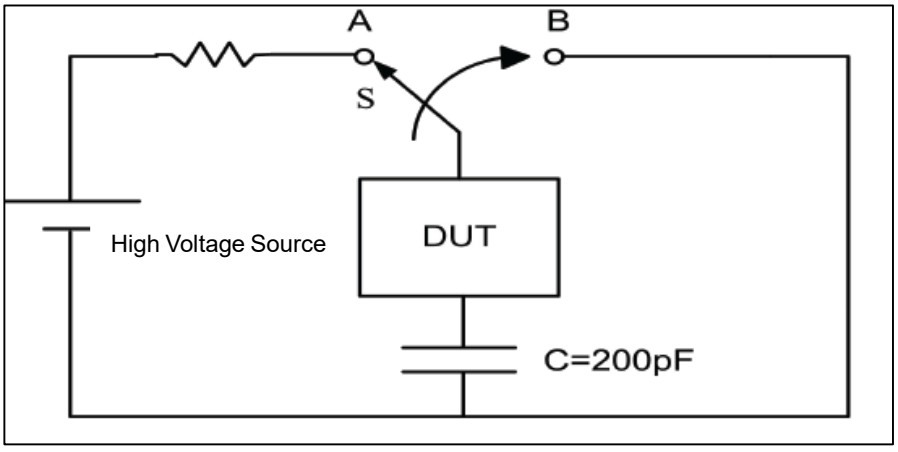
Figure 4-2. Ideal discharge model of component-level ESD HBM generator



4.2. Component level ESD CDM Charge Device Mode

The charged device model is the charged discharge of the IC itself. This way the charge is initially stored inside the IC, and if one of its pins touches a grounded object, it will self-discharge. Due to the difference in the angle of placement of the integrated circuit chip, the placement position, the type of package, the electrostatic charge accumulated inside the chip, etc; the equivalent capacitance will be different. This test meets the ESDA/JEDEC JS-002-2018 standard.

Figure 4-3. Ideal discharge model of component-level ESD CDM generator



4.3. Static Latch-up test

The Latch-up refers to a low-impedance path between the power supply power VDD and ground GND(VSS) in CMOS due to the interaction of parasitic PNP and NPN bipolar BJT. This phenomenon will lead to high current overload. In this case, the power supply needs to be disconnected to restore the initial state. Overload can be a voltage or current surge, excessive current or voltage change rate, or any other abnormal condition that causes the parasitic BJT to begin to self-hold. The Latch-up does not damage the device if the amplitude or duration of the current through the low-impedance path is sufficiently limited. This test meets the JESD78E standard.

To evaluate Latch-up performance, two complementary Latch-up tests are performed:

- Power supply overvoltage (applied to each power supply pin) simulates a user-applied transient overvoltage situation on the power supply.
- Current injection (applied to each input, output, and configurable I/O pin) simulates situations where an application causes a voltage to be applied to the pin to be higher than the maximum rating, such as a severe voltage on an input due to overshoot/ringing above VDD or below ground.

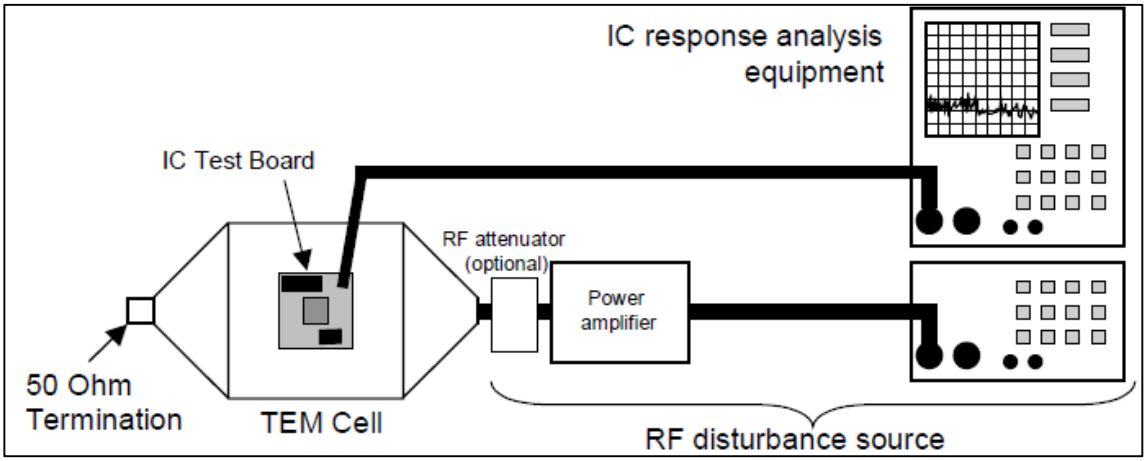
5. EMI characterization of MCU

EMI (electromagnetic interference) refers to the level of electromagnetic waves emitted by the device as the source of interference to the surrounding environment. The emitted electromagnetic waves are divided into conducted emissions and radiated emissions. Conducted emissions propagate along cables or interconnecting lines, while radiated emissions propagate through free space. This type of EMI coupling is typically encountered when the distance between the interferer and victim is typically greater than one wavelength λ.

5.1. Equipment of EMI test

The test complies with the SAE J1752-3:2017 (IEC61967-2) standard by testing in the TEM cell method, by rotating the test board by 0/90/180/270 degrees, testing the radiation noise in four directions. This method provides a good estimate of the level of radiated noise emitted by the MCU in the application environment. The MCU chip and package affect the radiated noise generated by the device, and the crystal and MCU system clock and its multiplied harmonics are generally EMI peaks.
Running firmware based on a simple application that toggles 2 LEDs via the I/O port.

Figure 5-1. Experiment layout of EMI test TEM method



5.2. The hardware and test standard of EMI test

The main indications related to test hardware in the IEC61967-1 standard are as follows:

Figure 5-1. IEC61967-1 standard PCB design reference

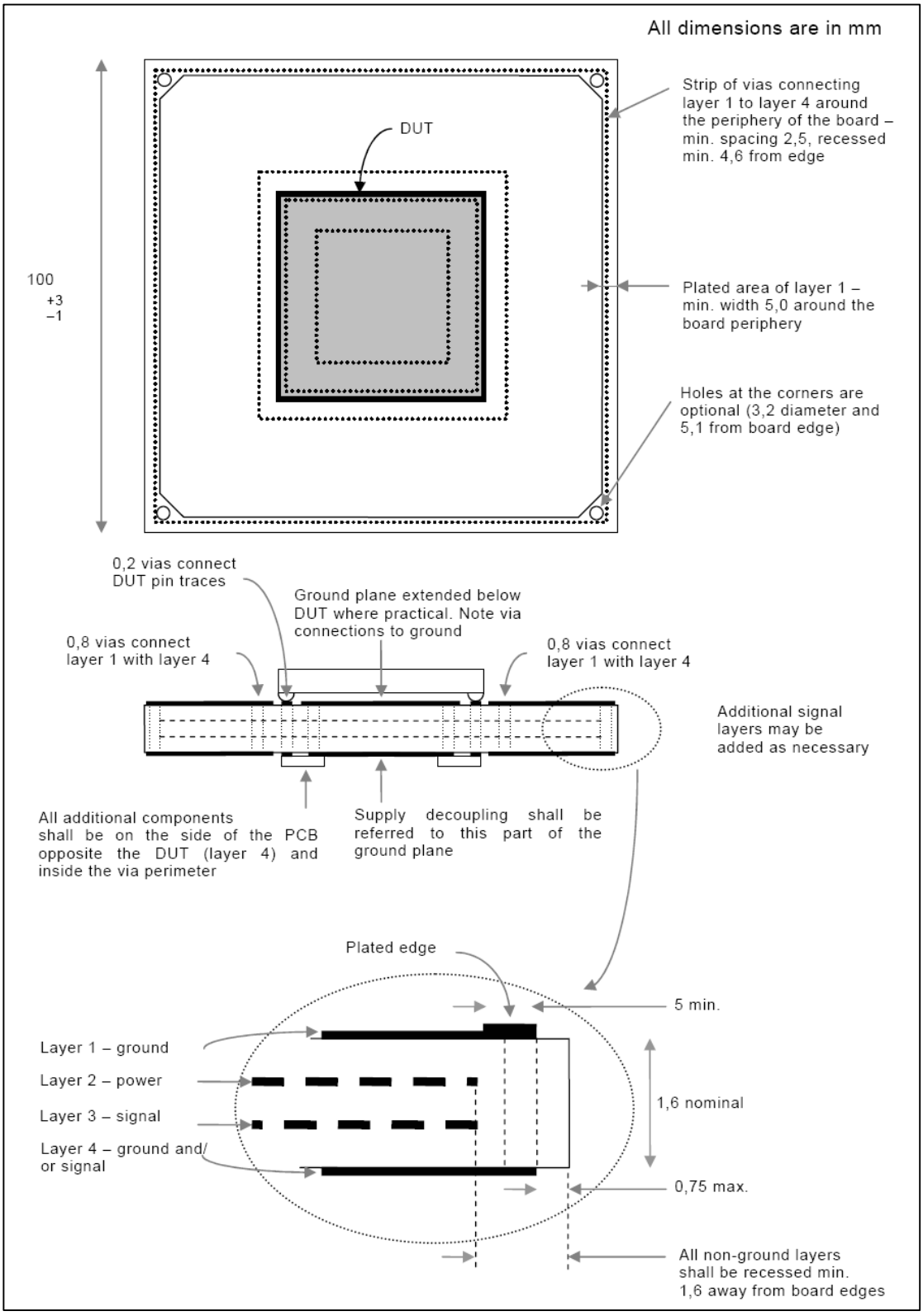


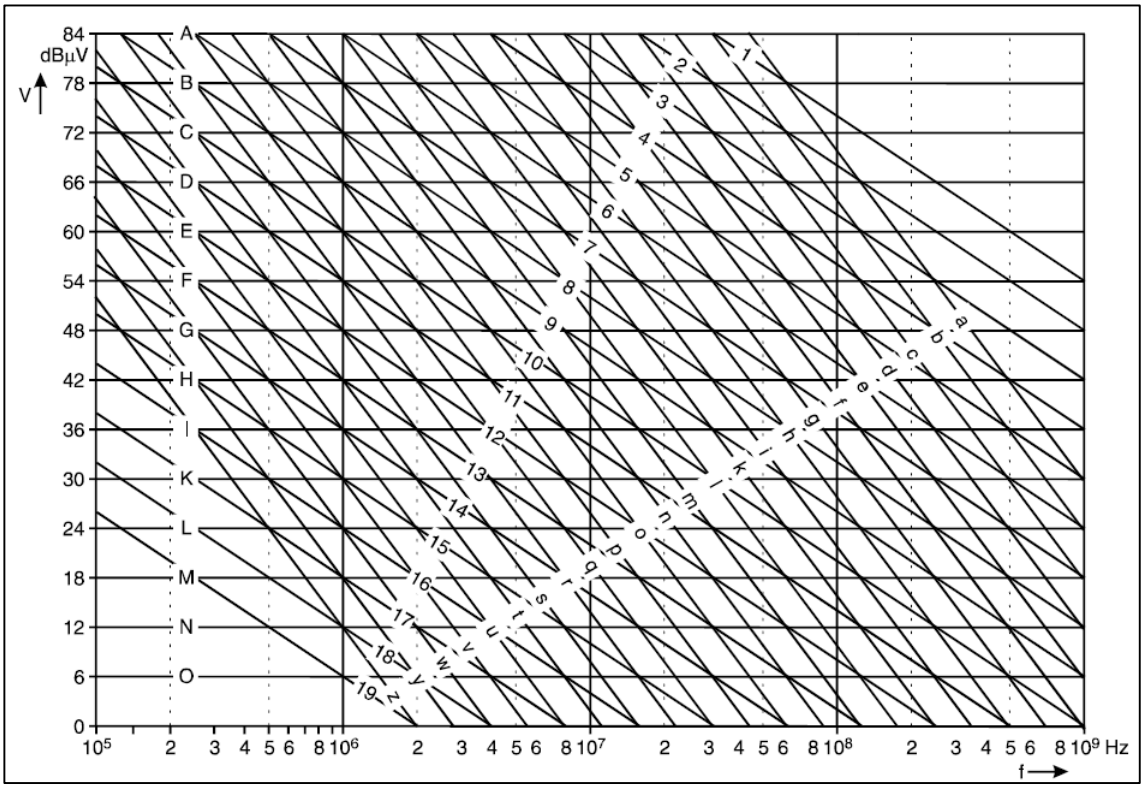
Figure 5-2. IC pin loading recommendations

IC PIN TYPE	PIN LOADING
Analog	
—Supply	As stated by the manufacturer (or as required)(1)
—Input	10 kΩ to ground (Vss) unless the IC is internally terminated
—Output Signal	10 kΩ to ground (Vss) unless the IC is internally terminated
—Output Power	Nominal loading as stated by the manufacturer
Digital	
—Supply	As stated by the manufacturer (or as required)[a]
—Input	Ground (Vss) or 10 kΩ to supply (Vdd) if cannot ground, unless the IC is internally terminated
—Output	47 pF to ground (Vss)
Control	
—Input	Ground (Vss) or 10 kΩ to supply (Vdd) if cannot ground, unless the IC is internally terminated
—Output	As stated by the manufacturer
—Bi-directional	47 pF to ground (Vss)
—Analogue	As stated by the manufacturer (or as required)[a]
(1). The actual load on the pin should be stated in the report.	

5.3. Target level of EMI test

EMI level classification is based on IEC61967-2 international standard

Figure 5-3. Emission characterization levels



The data in the Datasheet is presented as***Figure 5-4. IEC61967-2 radiation levels***:

Figure 5-4. IEC61967-2 radiation levels

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-10. EMI characteristics***(1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-10. EMI characteristics(1)

Symbol	Parameter	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}] 8/168 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +23 °C, LQFP144, f_{HCLK} = 168 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	3.49	dBµV
			30 MHz to 130 MHz	8.04	
			130 MHz to 1 GHz	16.70	

(1) Based on characterization, not tested in production.

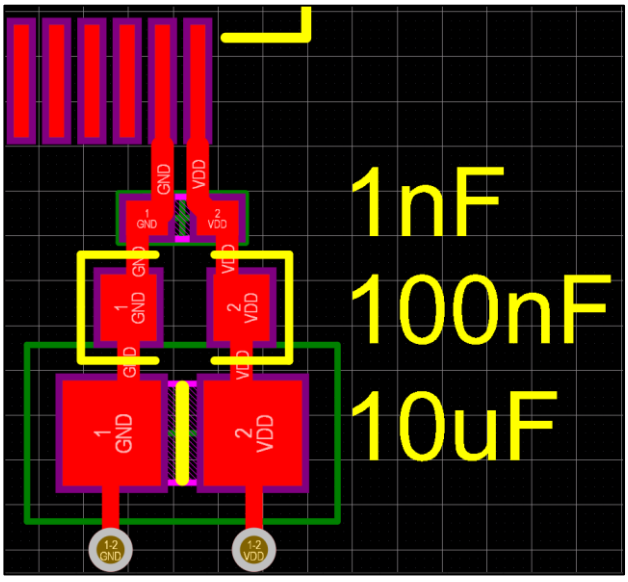
6. Hardware Strategy of GD32MCU EMC

6.1. Decoupling capacitor

At least one decoupling capacitor should be placed on each power pin of the MCU. The decoupling capacitor is required to provide the transient current required by the CMOS switching device MCU to offset the effect of the output inductance and the interconnect inductance of the power IC. In order to make the decoupling capacitor effective, the design and layout should be based on the following principles:

- A combination of decoupling capacitors is recommended. It is recommended to connect 10uF+100nF+1nF on each pin of MCU's VDD/VBAT power domain, and 1uF+10nF for each pin of VDDA power domain.
- The decoupling capacitors should be placed as close to the MCU as possible. When there are multiple decoupling capacitors, the smaller the capacitance is, the closer the capacitor is to the MCU. Usually, 1nF is the closest to the MCU pin, followed by 100nF, and 10uF is the outermost.
- Make sure that the supply current flows to the capacitor first and then to the MCU. If the power pin and the GND pin are far from each other, it is recommended to place the capacitor close to the GND pin, because the signal is generally based on GND.
- Each capacitor should have its own via, and it is strictly forbidden for multiple capacitors to share a via. The traces between the decoupling capacitors and the MCU pins should be as wide and short as possible to reduce the impedance between the decoupling capacitors and the MCU power pins. The traces between the power network and the decoupling capacitors should be as narrow and long as possible, or separated by VIA to provide high impedance for potential power supply noise and ripple.

Figure 6-1. Recommended Decoupling Capacitor Combinations



6.2. PCB stack design

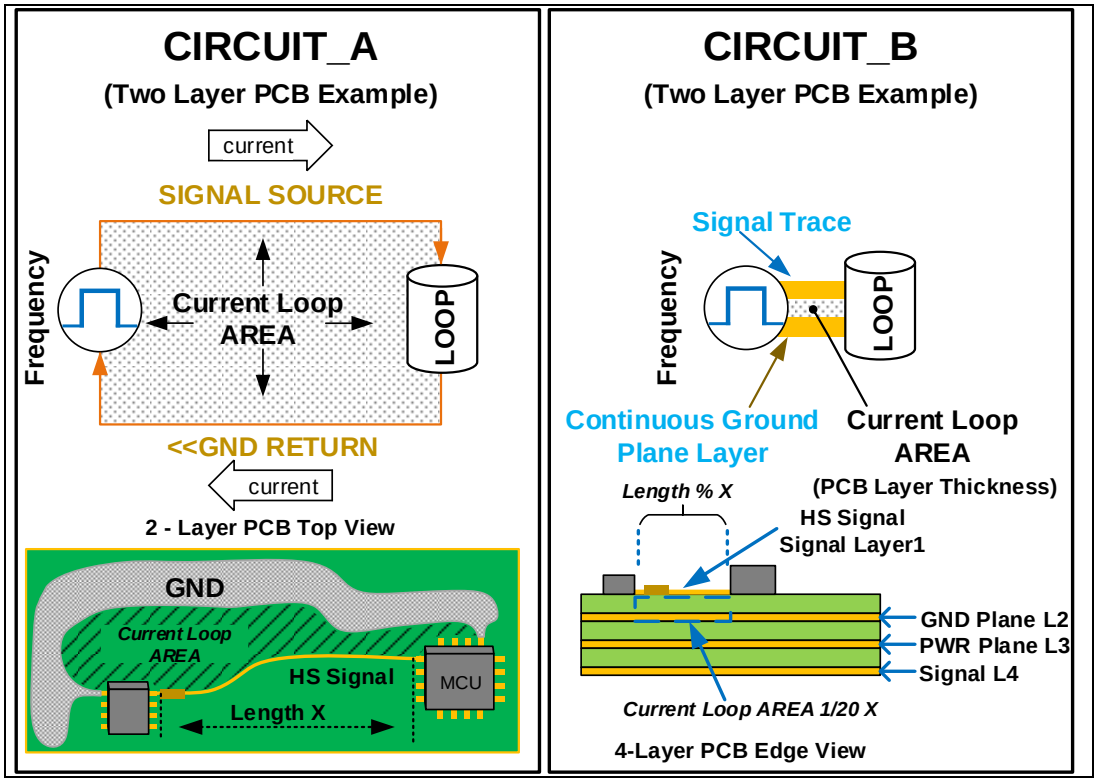
Before designing a four-layer board, you need to know the total thickness of the laminate required for the product, what the selected dielectric material is, and the type of impedance on the board. The four-layer stack is generally two signal layers and two reference layers. When designing, it is necessary to ensure that Layer 2 is a complete GND, and minimize the power supply and sensitive signal traces of the Bottom Layer. The recommended stack-up for a four-layer PCB is as follows:

Table 6-1.Recommended 4-layer PCB stackup

PCB Layer	Traces
Layer1	Signal1
PP	PP
Layer2	GND
Core	Core
Layer3	Power
PP	PP
Layer4	Signal2

The *Figure 6-2. Reflow area between two-layer and four-layer PCB* below shows the comparison of the reflow area of the two-layer board and the four-layer board. The reflow area of the four-layer PCB is 1/20 of that of the two-layer board, and the radiated EMI is less, and it is more conducive to the discharge of noise.

Figure 6-2. Reflow area between two-layer and four-layer PCB



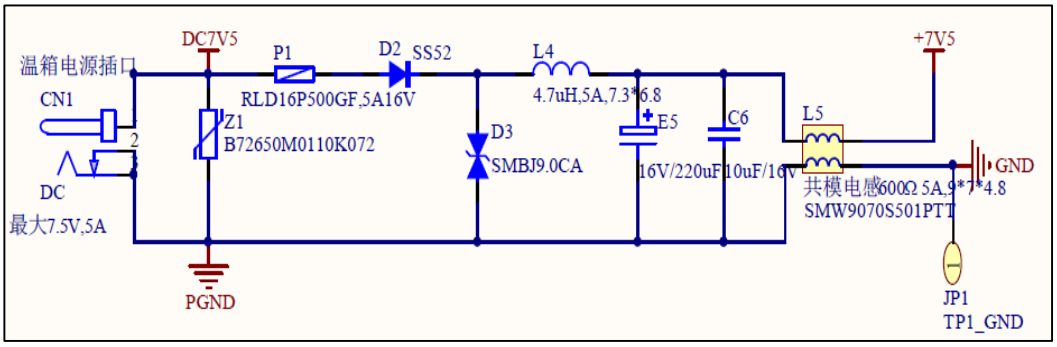
6.3. Power intergrity

6.3.1. Power filter

Each power supply must have a filter, which must be close to the regulator if it is on the board, or close to the PCB entry point if it is an external regulator. The filter should be designed according to the ripple characteristics of the regulator and the power supply requirements of the integrated circuit, and should include at least two capacitors: a large capacitor (μF) for low frequency filtering; a small capacitor for high frequency filtering (nF). ICs that require clean power should be equipped with an additional LC filter to avoid coupling of noise to other blocks of the circuit.

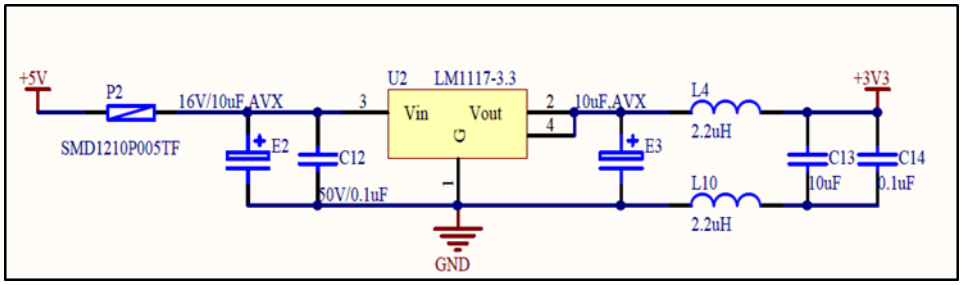
Power design example:

Figure 6-3. Recommended power protection design



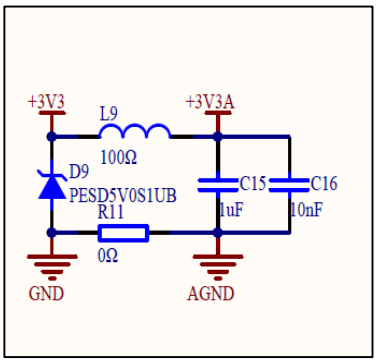
Design example of LDO:

Figure 6-4. Recommended LDO Design



The processing method between the power supply domain VDD and VDDA of the MCU is as follows:

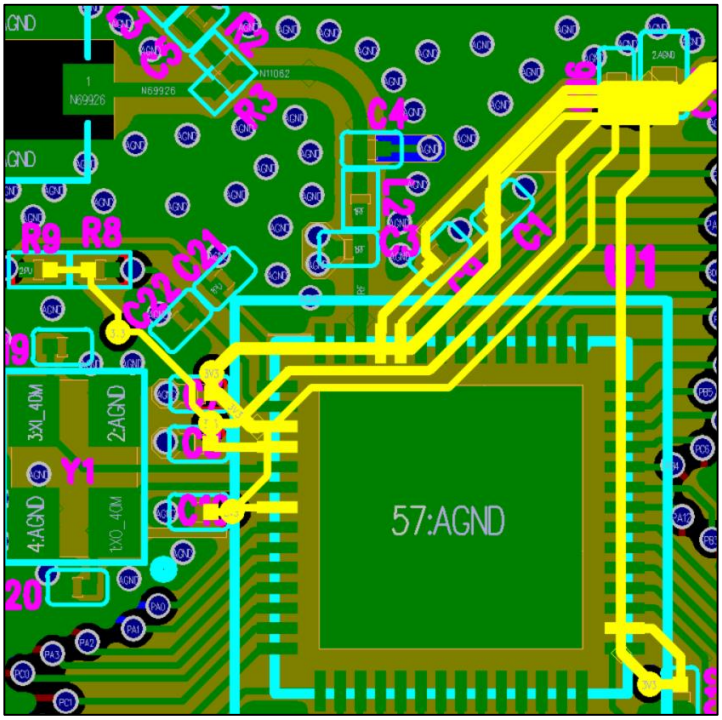
Figure 6-5. Recommended VDD&VDDA Design



6.3.2. Power network

It is recommended to use the "star" power supply mode for the 3.3V power supply wiring of the MCU. The traces of each power pin (Pin) are individually pulled from the 3.3V source to the chip Pin, and a large capacitor is placed at the 3.3V source.

Figure 6-6. Recommended MCU star power supply network

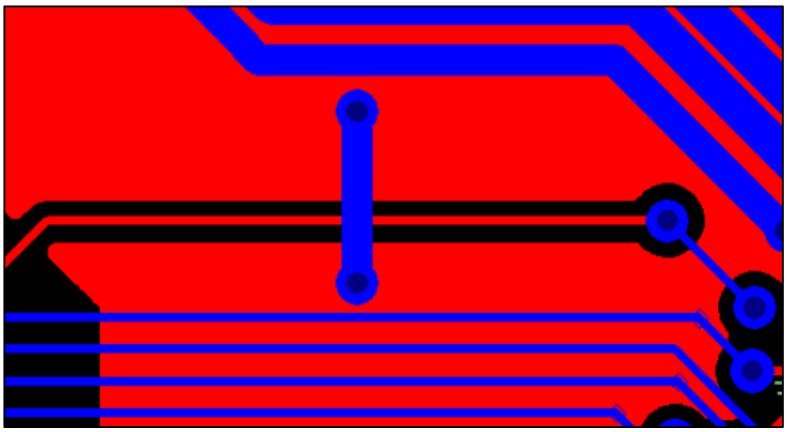


6.3.3. Intergrity of GND and Polygon

In addition to the reference layers of GND and Power, it is also recommended to lay copper as the GND network for the signal layer to avoid dead copper to ensure the integrity of the GND. The GND copper skin of the signal layer needs to be more VIA to the GND plane, which is beneficial to reduce the return area of high-frequency noise. In addition, it is recommended to use more VIA for the signal layer at the bottom of the MCU, which is conducive to heat dissipation and signal return. In addition, dead copper and islands can be bridged, as ***Figure***

6-7. Recommended bridging method:

Figure 6-7. Recommended bridging method

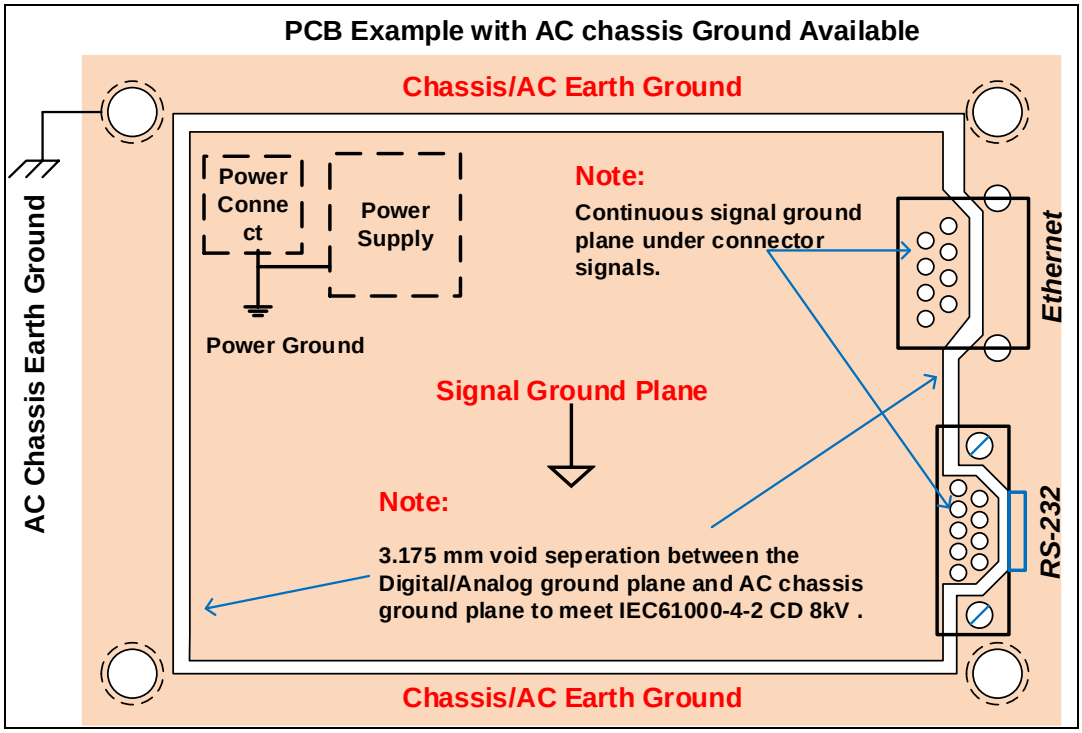


Grooving and borders. Separate the analog ground and the digital ground in the GND layer, and separate the digital ground and the analog ground on a ground plane by slotting, and the power ground does not need to be too separated. Since the noise and current generated by an analog circuit are several orders of magnitude smaller than those of a digital circuit, the analog ground is generally isolated from the digital ground in order not to introduce noise and current on the digital ground. The measure is generally through the isolation between the digital circuit and the analog circuit, as shown in the *Figure 6-7. Recommended bridging method*. High-frequency signals in the reference ground plane will automatically find the line with the smallest impedance (or least inductance, to be exact) and the shortest distance. However, when connecting vulgar digital circuits such as analog and digital domain logic, it is usually necessary to bridge a 1K-5K resistor in series at the slot. When it is necessary to connect high-speed signals in the analog domain and the digital domain, such as the audio decoding master clock, it should be connected directly instead of slotted, as shown in the *Figure 6-7. Recommended bridging method*, in practical applications, for terminal matching, generally 50 ohms at the clock source terminating resistor.

6.4. Layout design

The AC protective ground of the chassis, card holder, peripherals such as RS232 and CAN, and the connector box are electrically isolated from the signal ground. The enclosure should be connected to the ground (i.e. ground) of the AC rack as far as possible to harmlessly shun high voltage discharges to protective earth and not enter digital or analog ground circuits. Note that the ground plane is always continuous under all high-speed signal connections to the peripheral connector, but the connector housing is isolated from the external AC chassis plane.

Figure 6-8. Layout design of the recommended chassis protection ground



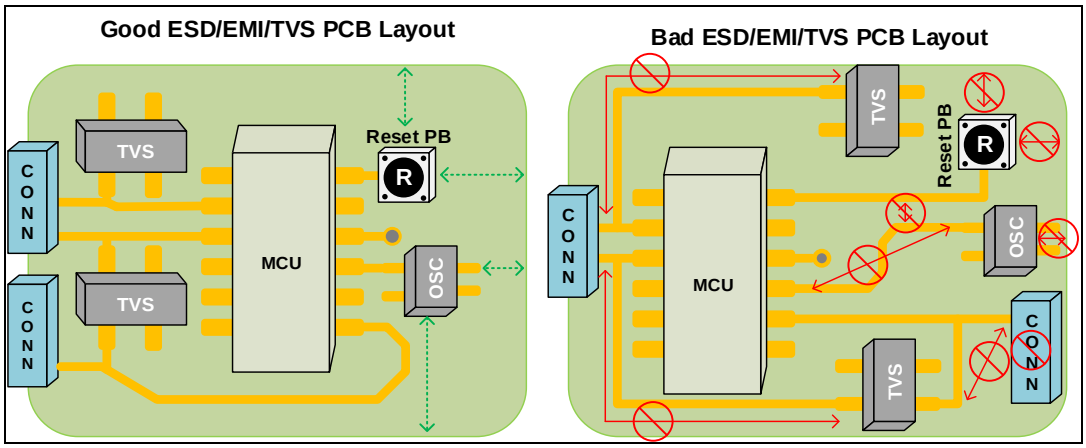
In the application of the chassis ground (protective earth/AC rack ground), it is strongly recommended not to ground the digital signal and the AC rack, and keep at least a certain distance between them > 3.175mm (0.125 inches), for 11-12 kV spark gap isolation to meet IEC61000-4-2 Level-4 8 kV contact discharge.

Place the TVS as close to the external signal connector as possible, connect the TVS ground directly to the ground plane, and avoid ground traces.

High-speed or sensitive analog/digital traces should be routed at least 2x times from the edge of the board, where "x" is the distance between the trace and its return current path. The electric and magnetic field lines associated with traces very close to the edge of the board are less accommodating. From these traces, the crosstalk and coupling to the antenna tends to be greater and makes them more susceptible to ESD, EMI and EFT events.

Sensitive components/circuits should be kept away from the edge of the PCB. It's best to place them in the center of the board. If this is not possible, try placing them more than 12 mm from the edge if not using external protective earth rings, as high frequency energy can concentrate on external edges during a high voltage discharge event, especially on right angle PCBs. The corners of the body (use rounded PCB corners).

Figure 6-9. Recommended protective device layout design



Components that interface with the outside world should be kept close to the edge of the PCB. The rest of the components should be kept away from the edge of the PCB to reduce environmental impact (eg, ESD).

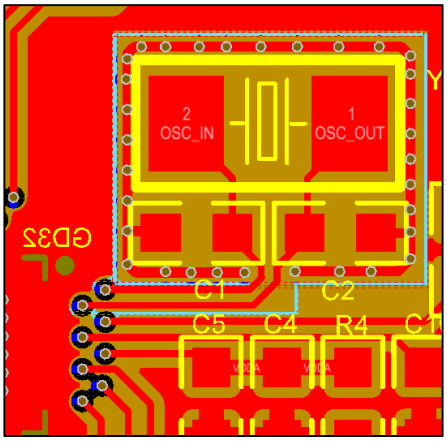
If a common mode choke or transient suppressor device (eg, TVS, MOV) is used for power filtering, it should be placed at the entrance of the PCB. In a circuit protected by a TVS circuit, the external signal from the connector should be routed first to the TVS, then to the ferrite or common mode choke, and then to the protected component.

6.5. Sensitive peripherals of MCU

6.5.1. Crystal oscillator design

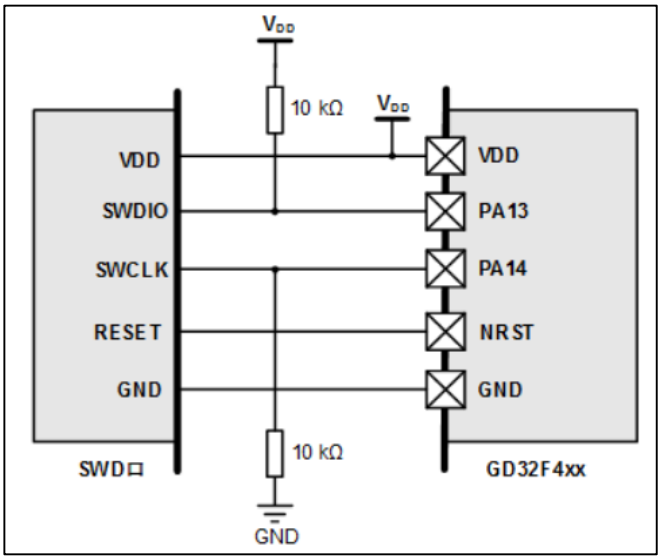
The crystal oscillator should be as close to the pin of the chip as possible, away from magnetic induction devices such as power inductors and radiating devices such as antennas, and isolated from other signal traces on the same layer by GND copper and VIA. The input and output traces of the crystal oscillators hould be as short as possible and less bent, and should not cross layers or cross traces. The load capacitors on both sides can be connected to the respective GND PAD of the crystal oscillator, and multiple GND VIAs can be placed to improve heat dissipation. Try not to take any transmission lines under the crystal oscillator, and keep the complete GND copper. The crystal oscillator circuit traces and matching capacitors should be measured in the same way as the crystal oscillator, and try not to penetrate the layers. The layout should make the crystal oscillator close to the MCU, and the crystal oscillator circuit traces should not be too long, not more than 12mm. The same layer and the next layer of the crystal oscillator are separated from other circuits, and the ground VIA is also used to form a guard ring around the crystal oscillator circuit.

Figure 6-10. Recommended Crystal Oscillator Lauout Design



Burning port SWD. The wiring of the SWD programming port of the MCU should be as short as possible, 12mm away from the edge of the board.

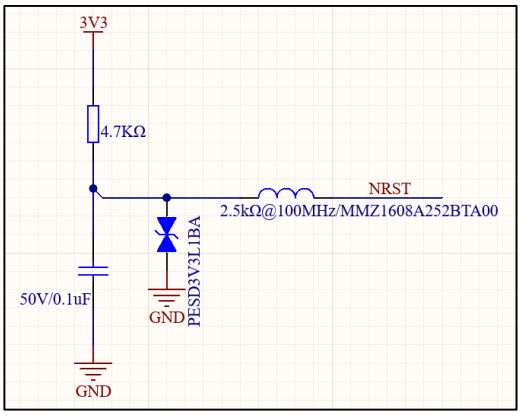
Figure 6-11. Recommended SWD programming port design



There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging. Shorten the length of the two SWD signal lines, preferably within 15cm; make a twist between the two SWD lines and the GND line, and wrap them together; connect the two signal lines of the SWD to ground with a small capacitor of tens of pf; the two signal lines of the SWD Any IO is connected in series with a 100Ω~1KΩ resistor.

6.5.2. Reset circuit NRST

Figure 6-12. Recommended reset circuit design



7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Aug.30. 2022

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