GigaDevice Semiconductor Inc.

Device limitations of GD32F3x0

Errata Sheet

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1. Introduction

This document applies to GD32F3x0 product series, as shown in ***Table 1-1. Applicable products***. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

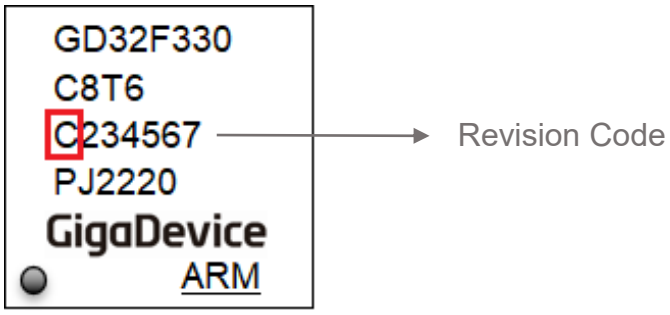
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32F310xx series
	GD32F330xx series
	GD32F350xx series

1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in ***Figure 1-1. Device revision code of GD32F3x0*** .

Figure 1-1. Device revision code of GD32F3x0



1.2. Summary of device limitations

The device limitations of GD32F3x0 are shown in ***Table 1-2. Device limitations***,please refer to section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code C
PMU	*MCU can not be waked up when an interrupt occurs before entering deep-sleep*	Y
	Standby mode can not be entered normally	Y
	Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode	N
TIMER	*TIMER comparator triggers BREAK failure*	Y

I2C	***Read one more data because the BTC flag was not cleared***	Y
Core	***VDIV or VSQRT instructions might not complete correctly when very short ISRs are used***	Y

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. PMU

2.1.1. MCU can not be waked up when an interrupt occurs before entering deep-sleep

Description & impact

When system application programme exists other interrupt code(such as systick / timer period interrupt) and needs to enter deep-sleep mode through WFE or WFI instruction, the system will exist the risk of not being wakedup after running for some time.

Workarounds

Application programme needs to mask all interrupts except EXTI for wakeup source before entering deep-sleep mode, then unmask the needed interrupts after wakeup.The latest firmware library of GD32F3x0 series has circumvented this problem.

2.1.2. Standby mode can not be entered normally

Description & impact

When system application programme exists other interrupt code(such as systick 1us period interrupt) and needs to enter standby mode through WFI instruction, the system can not enter the standby mode normally.

Workarounds

Application programme needs to mask all interrupts except wakeup source before entering standby mode, then unmask the needed interrupts after wakeup.

2.1.3. Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode

Description & impact

When reset the internal signal STBY_CTL to enter to standby mode, if the Tglitch is smaller than 100ns, which will cause the mcu cannot be waked up. The narrow glitch will result in incorrect Vcore voltage.

Note: The T_{glitch} is the time between STBY_CTL low level and the wakeup signal (PA0 high level)

Workarounds

Not available.

2.2. TIMER

2.2.1. TIMER comparator triggers BREAK failure

Description & impact

The break signal of the comparator output controlling the TIMER has no effect.

Workarounds

When the comparator triggers a break, it can only be triggered if the break polarity is configured to be active high.

2.3. I2C

2.3.1. Read one more data because the BTC flag was not cleared

Description & impact

If an interrupt occurs before reading I2C_DATA register when RBNE flag is set and BTC flag is reset, I2C will read an additional data if BTC flag is set during the interrupt processing because the read data operation can not clear the BTC flag.

Workarounds

1) Using interrupt method to read the I2C_DATA register.
2) Using DMA method to read the I2C_DATA register.

2.4. Core

2.4.1. VDIV or VSQRT instructions might not complete correctly when very short ISRs are used

This limitation refers to Arm ID number 776924 in “Cortex-M4 & Cortex-M4 with FPU Software Developers Errata Notice”.

Description & impact

The VDIV and VSQRT instructions take 14 cycles to execute. When an interrupt is taken a VDIV or VSQRT instruction is not terminated, and completes its execution while the interrupt stacking occurs. If lazy context save of floating point state is enabled then the automatic stacking of the floating point context does not occur until a floating point instruction is executed

inside the interrupt service routine.

Lazy context save is enabled by default. When it is enabled, the minimum time for the first instruction in the interrupt service routine to start executing is 12 cycles. In certain timing conditions, and if there is only one or two instructions inside the interrupt service routine, then the VDIV or VSQRT instruction might not write its result to the register bank or to the FPSCR.

The failure occurring conditions are as follows:

1) The floating point unit is enabled.
2) Lazy context saving is not disabled.
3) A VDIV or VSQRT is executed.
4) The destination register for the VDIV or VSQRT is one of s0 - s15.
5) An interrupt occurs and is taken.
6) The interrupt service routine being executed does not contain a floating point instruction.
7) Within 14 cycles after the VDIV or VSQRT is executed, an interrupt return is executed.

A minimum of 12 of these 14 cycles are utilized for the context state stacking, which leaves 2 cycles for instructions inside the interrupt service routine, or 2 wait states applied to the entire stacking sequence (which means that it is not a constant wait state for every access).

In general, this means that if the memory system inserts wait states for stack transactions then this erratum cannot be observed.

The implications of this limitation is that the VDIV or VQSRT instruction does not complete correctly and the register bank and FPSCR are not updated, which means that these registers hold incorrect, out of date, data.

Workarounds

A workaround is only required if the floating point unit is enabled. A workaround is not required if the stack is in external memory.

There are two possible workarounds:

1) Disable lazy context save of floating point state by clearing LSPEN to 0 (bit 30 of the FPCCR at address 0xE000EF34).
2) Ensure that every interrupt service routine contains more than 2 instructions in addition to the exception return instruction.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Aug.30 2022
1.1	Update note of chapter 1.2	Apr.4 2023
1.2	1. Add PMU limitation, referring to chapter 2.1.3 2. Add core limitation, referring to chapter 2.12.1	Nov.2 2023

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