GigaDevice Semiconductor Inc.

Device limitations of GD32L233

Errata Sheet

Revision 1.4

(Feb. 2025)

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1.   Introduction

This document applies to GD32L233 product series, as shown in **_Table 1-1. Applicable products_**. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.
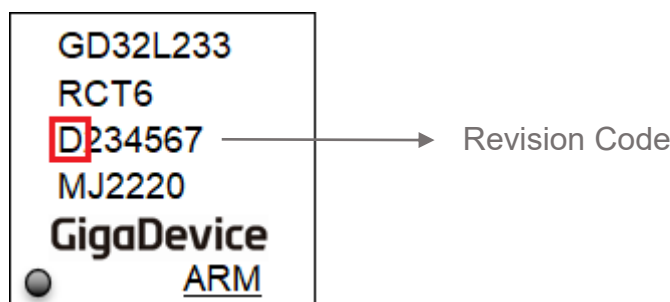
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32L233xx series

1.1.   Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in **_Figure 1-1. Device revision code of GD32L233_**.

Figure 1-1. Device revision code of GD32L233

1.2.   Summary of device limitations

The device limitations of GD32L233 are shown in **_Table 1-2. Device limitations_**, please refer to section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround			
		Rev. Code B	Rev. Code C	Rev. Code D	Rev. Code E
PMU	_FWDGTRSTF flag cannot be set in Deep-sleep mode_	Y	Y	Y	Y
RCU	_The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly_	Y	Y	Y	Y
I2C	_When SDA line interference causes garbled data on the I2C bus, it can lead to a stuck in the I2C slave device_	N	N	N	N

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Module	Limitations	Workaround			
		Rev. Code B	Rev. Code C	Rev. Code D	Rev. Code E
SLCD	*Do not support the use of internal voltage source*	Y	Y	--	--

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. PMU

2.1.1. FWDGTRSTF flag cannot be set in Deep-sleep mode

Description & impact

FWDGTRSTF bit cannot be set by hardware when mcu is in Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode and FWDGT reset is occurred.

Workarounds

The application programme can determine whether a FWDGT reset has occurred. For example, by marking whether the system has experienced a reset, and then excluding the cause of the reset, it can be determined if it was due to a FWDGT reset.

2.2. RCU

2.2.1. The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly

Description & impact

When LXTAL stops unexpectedly, the LXTALSTB bit cannot be cleared by disabling the LXTAL, which prevents the LXTAL from restarting.

Workarounds

Use one of the following solutions:

By repeatedly setting and resetting the LXTALBPS more than ten times to clear the LXTALSTB bit, and then reconfiguring the LXTAL. The reference code for clearing LXTALSTB bits is as follows:

```
void lxtal_stb_clear(void)
{
    volatile   uint32_t i = 0U;
    /* close LXTAL clock */
    rcu_osci_off(RCU_LXTAL);
    for(i = 0; i < 10; i++) {
        /* enable the LXTAL bypass mode */
        rcu_osci_bypass_mode_enable(RCU_LXTAL);
        /* disable the LXTAL bypass mode */
```

```
            rcu_osci_bypass_mode_disable(RCU_LXTAL);
        }
    }
}
```

2.3.   I2C

2.3.1.   When SDA line interference causes garbled data on the I2C bus, it can lead to a stuck in the I2C slave device

Description & impact

When I2C operates as a slave and is configured in 7-bit addressing mode, if the I2C slave device matches 10-bit address header during the I2C slave addressing phase and interference on the SCL / SDA line that causes the next RESTART signal to be sent early (the 9th SCL clock for sending the ACK was not sent), and then the slave matches the 7-bit address, which can result in the I2C slave pulling the SDA line low, ultimately leading to the I2C slave stuck.

When I2C operates as a slave and is configured in 10-bit addressing mode, and if there is a mismatch in the 10-bit address header or the lower 8 bits of the 10-bit address during the I2C slave addressing phase, interference on the SCL / SDA line that causes the next RESTART/STOP signal to be sent early can result in the I2C slave pulling the SDA line low, ultimately leading to the I2C slave stuck.

Workarounds

Not available.

2.4.   SLCD

2.4.1.   Do not support the use of internal voltage source

Description & impact

SLCD only supports the use of external voltage source but internal voltage source.

Workarounds

Use the external voltage source.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov.11 2022
1.1	Add limitations of Rev. Code D	Mar.28 2023
1.2	Update note of chapter 1.2	Apr.4 2023
1.3	1. Update the description of PMU limitation, refer to ***FWDGTRSTF flag cannot be set in Deep-sleep mode*** 2. Add the RCU limitation, refer to ***The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly*** 3. Add the I2C limitation, refer to ***When SDA line interference causes garbled data on the I2C bus, it can lead to a stuck in the I2C slave device*** 4. Add limitations of Rev. Code E	Sep.23 2024
1.4	1. Update the ***Summary of device limitations*** 2. Update the RCU limitation, refer to ***The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly***	Feb.21 2025

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