GigaDevice Semiconductor Inc.

GD32VF103 Hardware Development Guide

Application Note
AN091

Revision 1.3

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1. Introduction

The article is specially provided for developers of 32-bit general-purpose MCU GD32VF103 series based on RISC-V architecture. It provides an overall introduction to the hardware development of GD32VF103 series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32VF103 series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32VF103 series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32VF103 series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32VF103 series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32VF103 series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32VF103 series.
6. Reference circuit and PCB Layout design, mainly introduces GD32VF103 series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32VF103 series.

This document also satisfies the minimum system hardware resources used in application development based on GD32VF103 series products.

Table 1-1. Applicable products

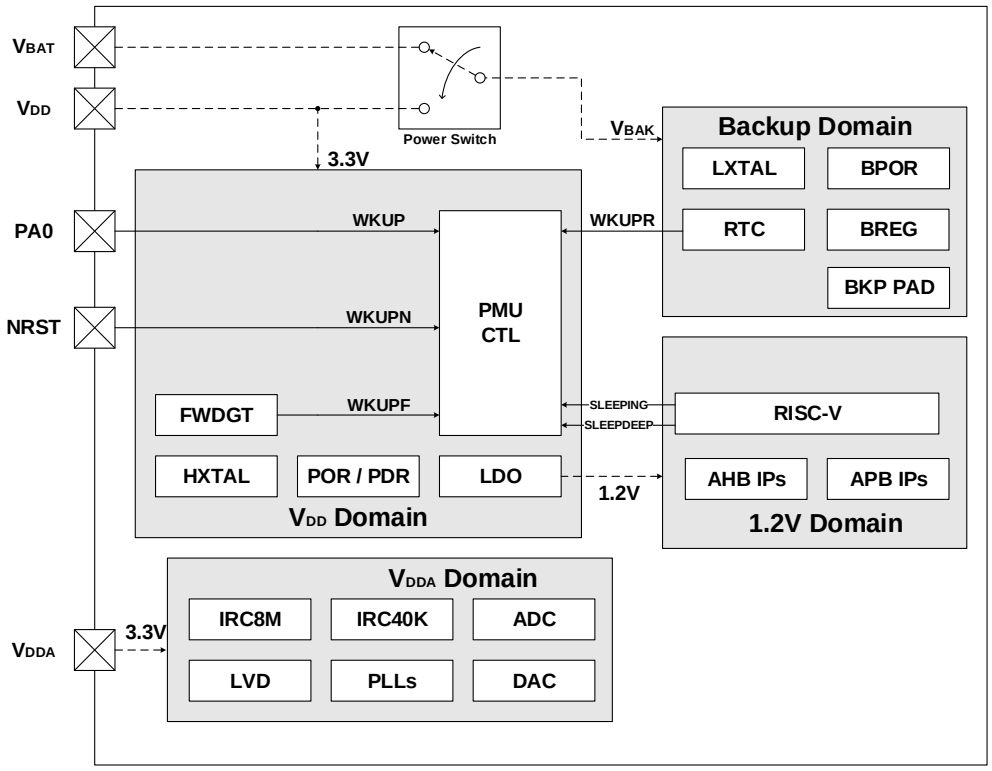
Type	Model
MCU	GD32VF103xx series

2. Hardware design

2.1. Power supply

The operating voltage range of GD32VF103x series V_{DD} / V_{DDA} is 2.6 V~3.6 V. As shown in ***Figure 2-1. GD32VF103 Series Power Domain Overview***, GD32VF103 series devices have three power domains, including V_{DD} / V_{DDA} domain, 1.2V domain and backup domain. The V_{DD} / V_{DDA} domain is directly powered by the power supply, and a LDO is embedded in the V_{DD} / V_{DDA} domain to power the 1.2V domain. The backup domain power supply V_{BAK} can be powered by V_{DD} or V_{BAT} through the power switch of the power switch. When the V_{DD} power is off, the power switch can switch the power supply of the backup domain to the V_{BAT} pin. At this time, the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. GD32VF103 Series Power Domain Overview



LVD: Low Voltage Detector
POR: Power On Reset
LDO: Voltage Regulator
PDR: Power Down Reset
BPOR: V_{BAK} Power On Reset
BREG: Backup registers

2.1.1. Backup domain

The backup domain power supply voltage range is 1.8 V~3.6 V. To ensure the normal operation of backup registers and RTC, when V_{DD} is closed, V_{BAT} pins can be connected to batteries or other backup power supplies. However, when V_{DD} is connected, V_{BAK} is powered by V_{DD} even though V_{BAT} pins is powered by external batteries.

If there is no external battery powered application, it is recommended to connect the V_{BAT} pin

to the V_{DD} pin after grounding through a 100nF capacitor.

Note: If the V_{BAT} pin is suspended, the power switch will switch the V_{BAK} to the V_{DD} after the MCU is powered on, and the internal V_{DD} will directly supply power to the Backup domain.

2.1.2. V_{DD} / V_{DDA} power domain

The V_{DD} / V_{DDA} power domain supplies power to all regions except the backup domain. If V_{DDA} is not equal to V_{DD}, the pressure difference between the two should not exceed 300mV (V_{DDA} and V_{DD} inside the chip are connected through back-to-back diodes). To avoid noise, V_{DDA} can be connected to V_{DD} through external filter circuit, and corresponding V_{SSA} can be connected to V_{SS} through specific circuit (single point grounding, through 0 Ω resistance or magnetic bead, etc.).

In order to improve the conversion accuracy of ADC, independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. The large package contains V_{REF} pins for independent power supply of ADC(2.4 V ≤ V_{REFP}≤ V_{DDA}, V_{REFN} = V_{SSA}).

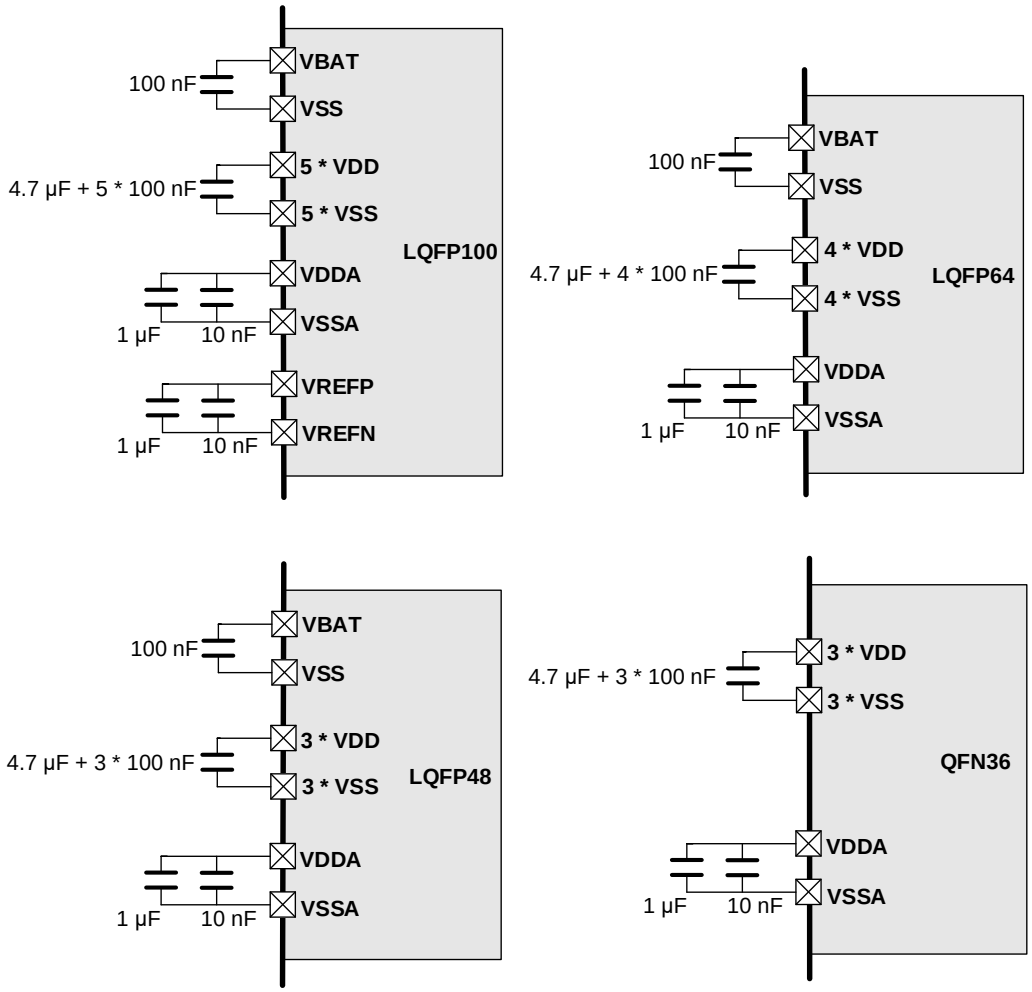
- The 100 pin package chip contains V_{REFP} and V_{REFN}, V_{REFP} can use an external reference power supply or be directly connected to V_{DDA}. V_{REFN} must be connected to V_{SSA}.
- 64 pin and smaller package chips have no V_{REFP} and V_{REFN}, which are directly connected to V_{DDA} and V_{SSA} internally. All analog modules are powered by V_{DDA} (including ADC / DAC).

2.1.3. Power supply design

The system needs a stable power supply. Some important matters need to be noted during development and use:

- VDD pin must be connected with external capacitance (N * 100nF ceramic capacitance+tantalum capacitance not less than 4.7uF, at least one VDD must be connected with capacitance not less than 4.7uF to GND, and other VDD pins must be connected with 100nF).
- VDDA pin must be connected with external capacitor (10nF+1uF ceramic capacitor is recommended).
- The VBAT pin must be connected to the external battery (1.8 V~3.6 V). If there is no external battery, it is recommended to connect the VBAT pin to the VDD pin after grounding through a 100nF capacitor.
- VREFP pin can be directly connected to VDDA. If a separate external reference voltage is used on VREF (2.4V ≤ VREFP≤ VDDA, VREFN = VSSA), 10nF+1uF ceramic capacitor must also be connected to the ground on VREFP pin.

Figure 2-2. GD32VF103 series recommended power supply design



Note:

1. All decoupling capacitors must be placed close to the corresponding V_{DD}, V_{DDA}, V_{REFP} and V_{BAT} pins of the chip.
2. V_{BAT} can be directly connected to V_{DD} or external battery according to actual application.
3. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
4. LQFP64、LQFP48、QFN36: VDDA、VREFP are connected internally, VSSA、VREFN are connected internally.

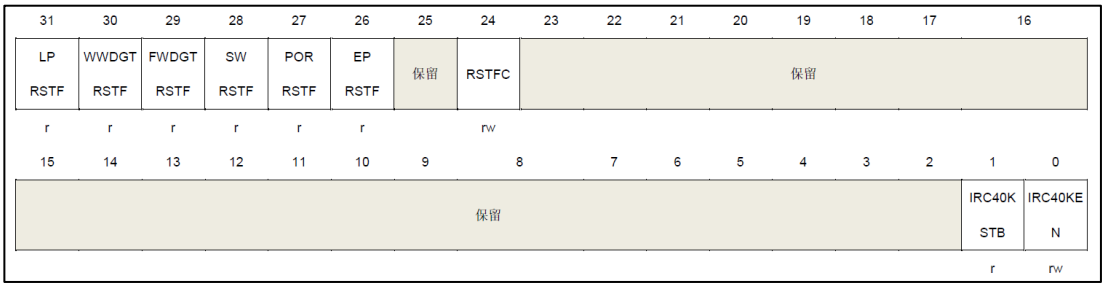
2.2. Power Detection and Reset

In this section, it is assumed by default that the VDD and VDDA pins remain connected and are powered by the same power source.

The reset control for the GD32VF103 series includes three types of resets: power reset, system reset, and backup domain reset. Power reset is a cold reset, which resets all systems except for the backup domain at power-up. During power and system resets, NRST will remain low until the reset ends.

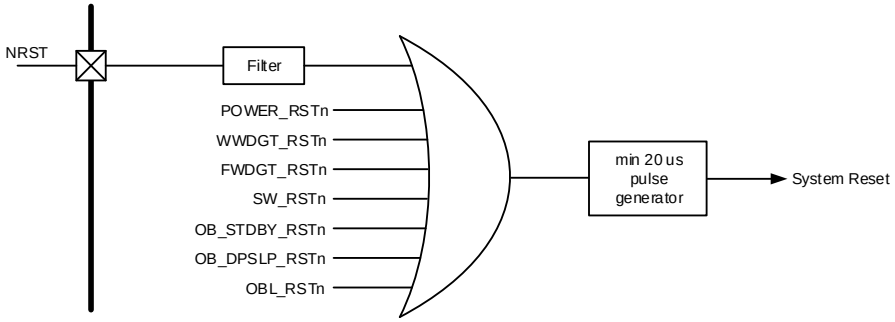
The MCU reset source can be determined by querying the register RCU_RSTSCK (0x40021024). This register can only clear flag bits through a power-on reset. Therefore, in use, after obtaining the reset source, the reset flags can be cleared through the RSTFC control bit. This allows more accurate reflection of watchdog resets or other reset events in the RCU_RSTSCK register.

Figure 2-3. RCU_RSTSCK register



During the power and system reset process, NRST will remain at a low level until the reset finishes. If the MCU cannot start executing, an oscilloscope can be used to monitor the waveform of the NRST pin to determine whether the chip is continuously experiencing reset events. The MCU is internally integrated with power-on/power-off reset circuitry. When a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) delivers at least a 20μs low-level pulse delay.

Figure 2-4. System reset circuit



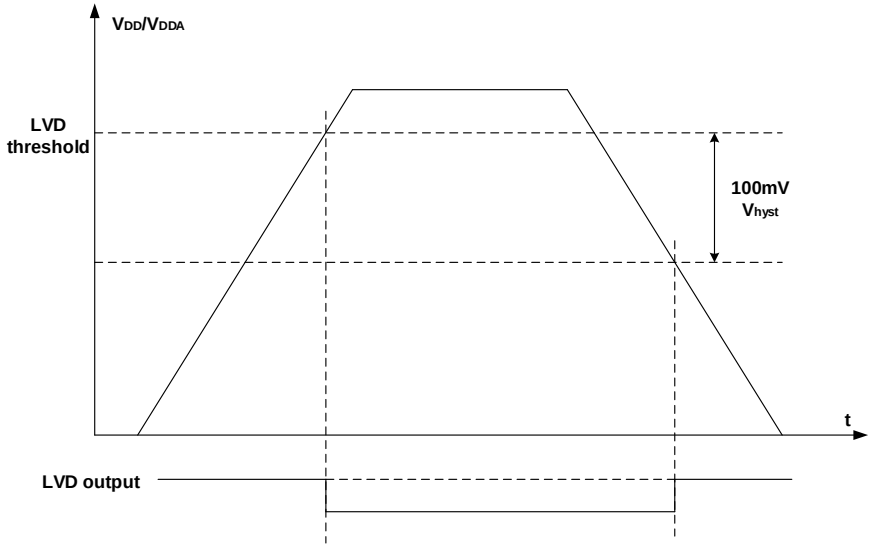
2.2.1. LVD

The function of the Low Voltage Detector (LVD) is to detect whether the VDD/VDDA supply voltage falls below the low voltage detection threshold (2.2 V to 2.9 V), which is configured by the LVDT[2:0] bits in the Power Management Unit Control Register (PMU_CTL). LVD is enabled by setting the LVDEN bit, and the LVDF bit located in the Power Management Unit Status Register (PMU_CS) indicates whether a low voltage event has occurred. This event is connected to line 16 of the EXTI, and users can configure line 16 of the EXTI to generate the corresponding interrupt. (The LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16). The hysteresis voltage Vhyst is 100mV. It is recommended to disable the LVD function before entering deep sleep mode or standby mode to avoid additional power consumption.

LVD application scenarios: When the MCU power supply is subjected to external interference,

such as a voltage drop, the LVD can be set to a low voltage detection threshold (which is higher than the Power-Down Reset (PDR) value). Once the voltage drops to this threshold, the LVD interrupt is triggered. Operations such as a soft reset can be executed within the interrupt function to prevent the MCU from encountering other anomalies.

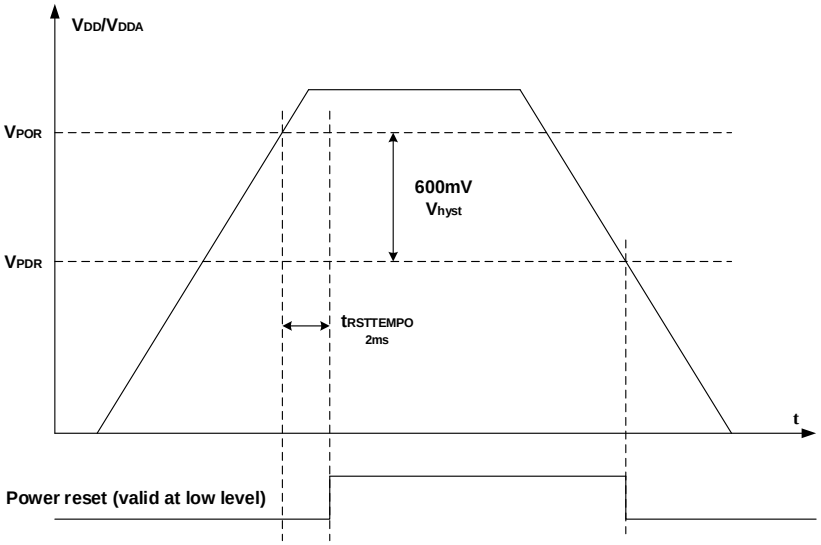
Figure 2-5. LVD threshold waveform



2.2.2. POR/PDR

The chip internally integrates a Power-On Reset (POR) / Power-Down Reset (PDR) circuit to monitor VDD/VDDA and generate a power reset signal when the voltage falls below a specific threshold, resetting the entire chip except for the backup domain. VPOR represents the power-on reset threshold voltage, with a typical value of about 2.4V, and VPDR represents the power-down reset threshold voltage, with a typical value of about 1.8V. The hysteresis voltage Vhyst is approximately 600mV.

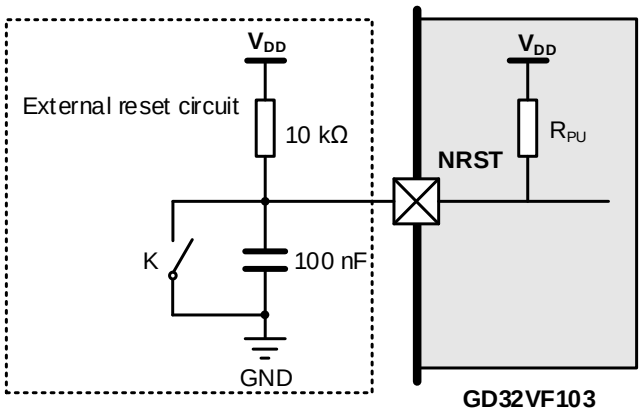
Figure 2-6**. Power on / power off reset waveform**



2.2.3. NRST Pin

For the MCU's NRST pin, it is recommended to place a capacitor (typically 100 nF) to prevent accidental reset triggering.

Figure 2-7. Recommended external reset circuit

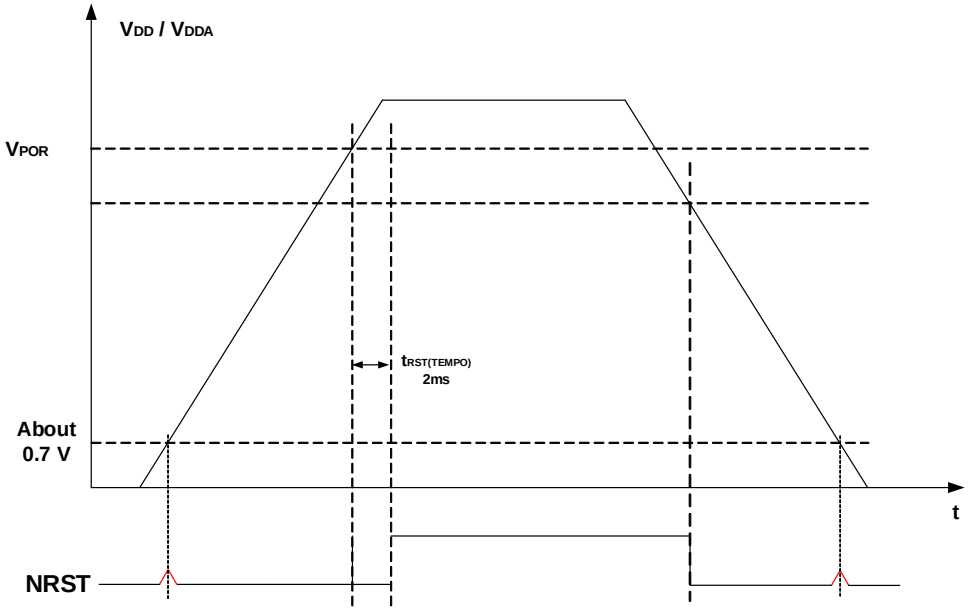


Note:

1. The internal pull-up resistance (RPU) is 40 kΩ. You are advised to connect the external pull-up resistance (RPU) to 10 KΩ so that voltage interference does not cause chip abnormalities.
2. ESD protection diode can be placed at the NRST pin if static electricity and other influences are considered.
3. Although there is a hardware POR circuit inside MCU, it is recommended to add NRST reset resistor capacitor circuit externally.
4. If the MCU starts abnormally (due to voltage fluctuation, etc.), the NRST capacitance to ground can be increased appropriately to lengthen the MCU reset completion time and avoid the abnormal power on timing zone.

Due to the threshold voltage characteristics of MOS transistors, during the power-up and power-down process of the chip, when V_{DD} / V_{DDA} is less than 0.7V, the internal pull-down MOS transistor of the chip will not pull the NRST pin low. In other words, during the power-up and power-down process, when V_{DD} / V_{DDA} is approximately 0.7V, a small pulse may occur, which does not affect the normal operation of the chip. This is illustrated by the red pulse shown in ***Figure 2-8. NRST Pin Power-On/Power-Down MOSFET Pulse Diagram***.

Figure 2-8. NRST Pin Power-On/Power-Down MOSFET Pulse Diagram



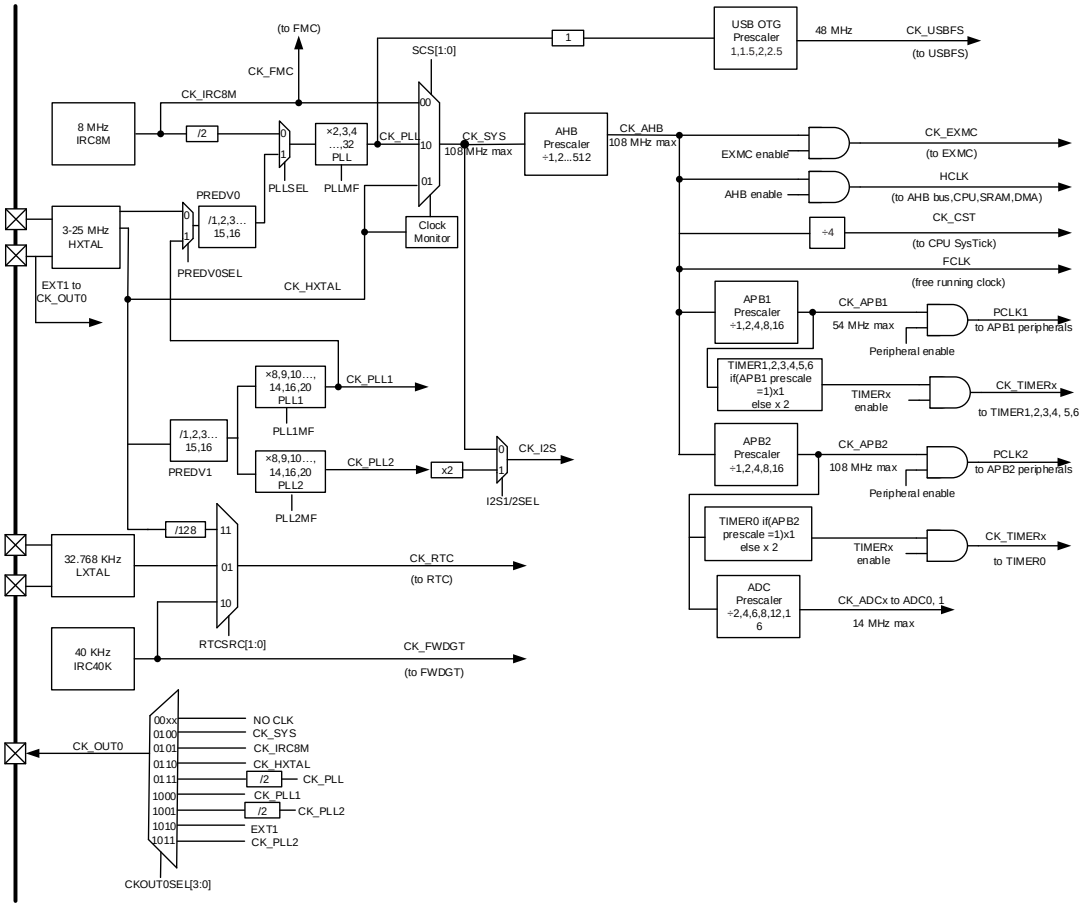
Due to the difference in charging and discharging speeds, the duration of the pulse on the falling edge is slightly longer than on the rising edge, with both durations being in the millisecond range.

2.3. Clock

GD32VF103 series has a complete clock system inside, which can select the appropriate clock source according to different applications. The main characteristics of the clock are as follows:

- 3-25 MHz external high-speed crystal oscillator (HXTAL).
- 8 MHz internal high-speed RC oscillator (IRC8M).
- 32.768 kHz external low-speed crystal oscillator (LXTAL).
- 40 kHz internal low speed RC oscillator (IRC40K).
- PLL clock source can be HXTAL or IRC8M.
- HXTAL clock can be monitored.

Figure 2-9. Clock tree



2.3.1. External high-speed crystal oscillator clock(HXTAL)

3-25MHz external high-speed crystal oscillator (passive crystal) can provide accurate master clock for the system. The crystal of this specific frequency must be placed close to the HXTAL pin, and the external resistance and matching capacitance connected to the crystal must be adjusted according to the selected oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). During bypass input, the signal is connected to OSC_ IN, The OSC_OUT remains suspended. The software needs to turn on the Bypass function of HXTAL (enable the HXTALBPS bit in RCU_CTL).

Figure 2-10. HXTAL external crystal circuit

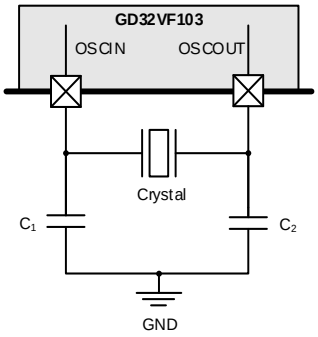
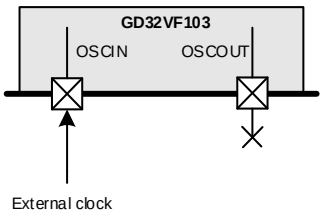


Figure 2-11. HXTAL external clock circuit



Note:

1. When bypass input is used, the signal is transferred from OSC_IN input, OSC_OUT remains suspended.
2. For the size of external matching capacitance, please refer to the formula:C_1=C_2=2*(C_{LOAD}-C_S), where C_S is the stray capacitance of PCB and MCU pins, and the typical value is 10pF. When it is recommended to select external high-speed crystals, try to select those with crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 have capacitance values of 20pF, and PCB layout should be as close to the crystal oscillator pin as possible.
3. C_S is the parasitic capacitance on PCB wiring and IC pin. When the crystal is closer to MCU, C_S is smaller, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, resulting in abnormal crystal operation, the external matching capacitance can be appropriately reduced.
4. When using external high-speed crystal, it is recommended to connect 1M Ω resistors in parallel at both ends of the crystal to make it easier for the crystal to vibrate.
5. Precision: external active crystal>external passive crystal>internal IRC8M.
6. If the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7V_{DD}, and the low level is required to be no more than 0.3V_{DD}.
7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSC_OUT and OSC_IN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768KHz low-speed external crystal (passive crystal), which can provide RTC with a low-power and high-precision clock source (LXTAL pin is not available for package models below 48 pins). The RTU module of MCU is equivalent to a counter, and the accuracy will be affected by crystal performance, matching capacitance, PCB material, etc. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design, calibrate LXTAL through TIMER, and set the frequency division register of RTC according to the calibration. LXTAL can also support bypass clock input (active crystal

oscillator, etc.) by configuring the LXTALBPS bit in RCU_BDCTL is enabled.

Figure 2-12. LXTAL external crystal circuit

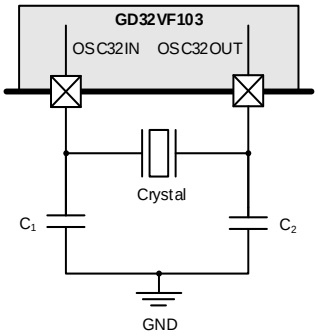
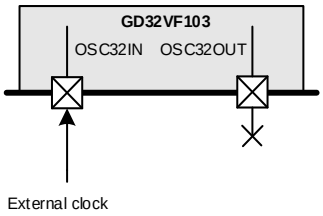


Figure 2-13. LXTAL external clock circuit



Note:

1. When bypass input is used, the signal is transferred from OSC32_ IN input, OSC32_ OUT remains suspended.
2. For the size of external matching capacitance, please refer to the formula: $C_1=C_2=2*(C_{LOAD}-C_S)$, where C_S is the stray capacitance of PCB and MCU pins, and the empirical value is between 2pF-7pF. It is recommended that 5pF be taken as the reference value for calculation. When it is recommended to select external crystals, try to select those with a crystal load capacitance of about 10pF, so that the external matching capacitors C_1 and C_2 have a capacitance value of 10pF, and PCB layout should be as close to the crystal oscillator pin as possible.
3. When IRC40K is selected as the clock source by RTC and VBAT is used for external independent power supply, if MCU is powered off at this time, RTC will stop counting. After power on again, RTC will continue to accumulate the time based on the previous count value. If the application needs to use VBAT to supply power to the RTC, the RTC can still time normally, and the RTC must select LXTAL as the clock source.

2.3.3. Clock output capacity (CKOUT)

GD32VF103 series MCU can be configured with the CKOUT0SEL[3:0] bit of clock register RCU_CFG0 selects different clock signal outputs, and the corresponding GPIO pin PA8 needs to be configured as a multiplexing function to output the selected signal.

Table 2-1. CKOUT0SEL[3:0] control bit

CKOUT0SEL[3:0]	Clock source
00xx	No clock output
0100	CK_SYS
0101	CK_IRC8M
0110	CK_HXTAL
0111	CK_PLL / 2
1000	CK_PLL1
1001	CK_PLL2 / 2
1010	EXT1
1011	CK_PLL2

2.3.4. HXTAL clock monitor (CKM)

The HXTAL clock monitor function is enabled by the HXTAL clock monitor enable bit, CKMEN, in the control register, RCU_CTL. This function should be enabled after the HXTAL start-up delay and disabled when the HXTAL is stopped. Once the HXTAL failure is detected, the HXTAL will be automatically disabled. The HXTAL Clock Stuck Flag, CKMIF, in the interrupt register, RCU_INT, will be set and the HXTAL failure event will be generated. This failure interrupt is connected to the Non-Maskable Interrupt, NMI, of the RISC-V.

Note: If HXTAL is selected as the system clock, PLL or RTC clock source, HXTAL failure will cause IRC8M to be selected as the system clock source, PLL will be automatically disabled, and RTC clock source needs to be reconfigured.

2.4. Startup configuration

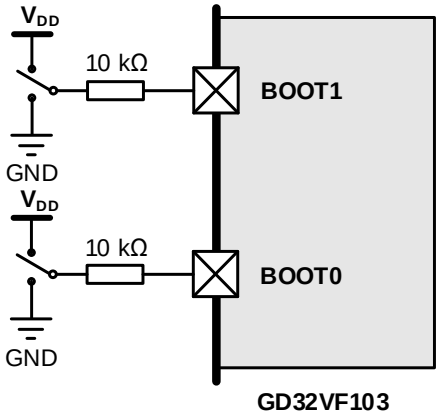
GD32VF103 series provides three startup modes, which can be configured through BOOT0 and BOOT1. The user can configure BOOT0 and BOOT1 for power on reset or system reset to determine the startup options. When designing the circuit, run the user program, BOOT0 cannot be suspended in the air, and it is recommended to use a 10kΩ resistor to GND; Run System Memory to update the program. You need to connect BOOT0 to high and BOOT1 to low. After the update is completed, connect BOOT0 to low and power on to run the user program; SRAM execution program is mostly used in debugging state.

The embedded Bootloader is stored in the system storage space for reprogramming the FLASH memory. In the GD32VF103 device, the Bootloader can interact with the outside world through USART0 (PA9 and PA10), USART1 (PD5 and PD6), and USBFS (PA9, PA11 and PA12).

Table 2-2. BOOT mode

BOOT mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-14. Recommended BOOT circuit design



Note:

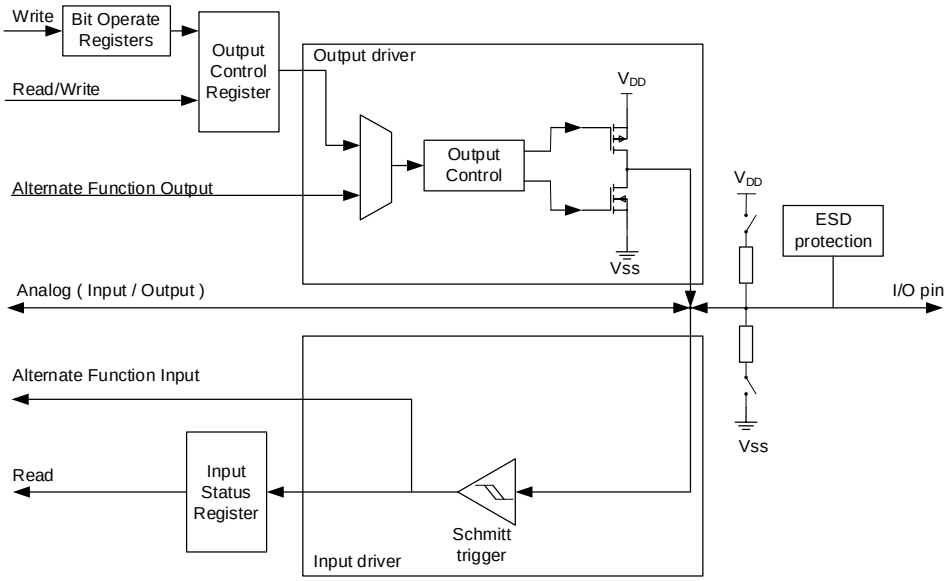
1. After the MCU is running, if the BOOT status is changed, it can take effect only after the system is reset.
2. Once the BOOT1 pin status is sampled, it can be released for other purposes.

2.5. Typical peripheral modules

2.5.1. GPIO circuit

The GPIO interface includes five groups of general-purpose input / output ports. Each group of ports provides up to 16 general-purpose input / output pins, namely PA0~PA15, PB0~PB15, PC0~PC15, PD0~PD15 and PE0~PE15. Each pin can be independently configured through a register. See the following figure for the basic structure of the GPIO interface:

Figure 2-15. Basic structure of standard IO



Note:

1. IO port is divided into 5V withstand and non 5V withstand. When using, pay attention to distinguish the withstand voltage of IO port. See Datasheet for details.
2. When the 5V tolerant IO port is 5V directly, it is recommended that the IO port be configured as open drain mode for external pull-up operation.
3. After the power on reset of the IO port, the default mode is floating input, and the level characteristics are uncertain. In order to obtain a more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to the application requirements (ports that are not led out in the chip also need to be configured).
4. To improve the EMC performance, it is recommended to pull up or down the unused IO port pins.
5. The drive capacity of the three IO ports PC13, PC14 and PC15 is weak, and the output current capacity is limited (about 3mA). When the output mode is configured, the operating speed cannot exceed 2MHz (the maximum load is 30pF).
6. In multiple groups, only one IO port with the same label PIN can be configured as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate an external interrupt, and do not support the three same external interrupt modes.
7. Non-5V tolerance of IO, when the external voltage exceeds VDD, may generate the irrigation current.

2.5.2. ADC circuit

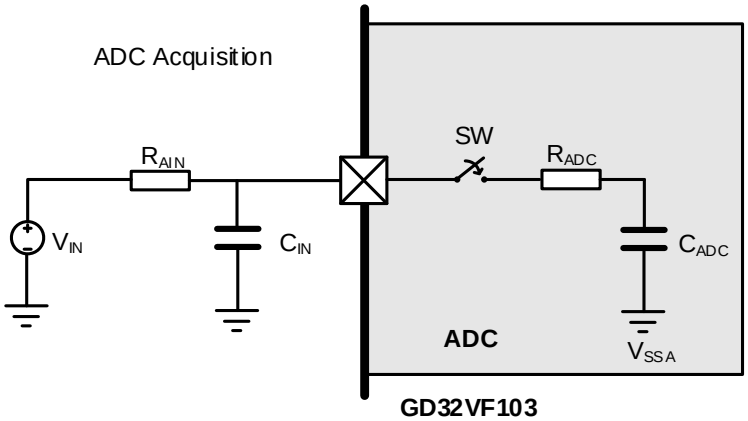
GD32VF103 is internally integrated with a 12 bit SAR ADC, which has up to 18 channels and can measure 16 external and 2 internal signal sources. The internal signal is the temperature sensor channel (ADC0_CH16) and the internal reference voltage input channel

(ADC0_CH17). The temperature sensor reflects the change of temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a stable voltage output (1.2V) to ADC and is internally connected to ADC0_ IN17.

If ADC collects external input voltage during use, if the sampling data fluctuates greatly, it may be due to interference caused by power supply fluctuation. It can be calibrated by sampling internal V_{REFINT} to deduce external sampling voltage.

When designing ADC circuit, it is recommended to place a small capacitor at the input pin of ADC, and it is recommended to place a small capacitor of 500pF.

Figure 2-16. ADC Acquisition Circuit Design



When f_{ADC}=14MHz, the relationship between the input impedance and the sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during the use process, select a larger value for the sampling period as much as possible, and reduce the input impedance as much as possible during the design of external circuits. If necessary, use the op amp follower to reduce the input impedance.

Table 2-3. Relationship between f_{ADC}=14MHz sampling period and external input impedance

T_s(cycles)	t_s(us)	R_{AINmax} (kΩ)
1.5	0.11	1.46
7.5	0.54	9.49
13.5	0.96	17.5
28.5	2.04	37.6
41.5	2.96	55
55.5	3.96	73.7
71.5	5.11	95
239.5	17.11	320

2.5.3. USB circuit

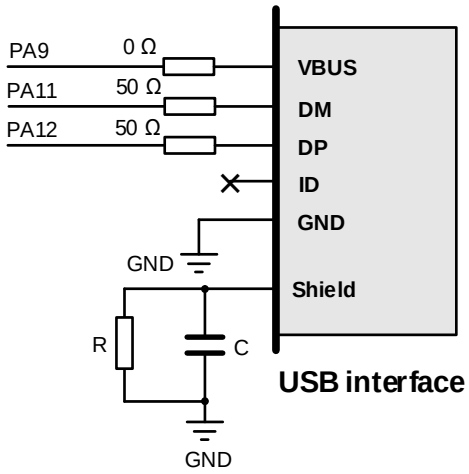
GD32VF103 series MCU has embedded USB interface, which is a USBFS module. The USB

protocol requires that the clock accuracy be no less than 500ppm, and the IRC8M may not be able to achieve such accuracy. Therefore, it is recommended to use an external crystal or an active crystal oscillator as the clock source of the USB module when using the USB function.

GD32VF103 series USB can be designed as both USB device and USB host. When the device is designed, if PA9 is connected to VBUS, the DP line does not need to be connected with an external 1.5K pull-up resistor; If PA9 is not connected to VBUS, and VBUSIG control bit in USBFS_GCCFG register is configured, then USB_DP data cable can not be externally connected with 1.5K pull-up resistor. If this register is not configured, then the USB_DP data line needs to be externally connected with 1.5K pull-up resistor.

When designing the circuit, in order to improve the ESD performance of USB, it is recommended to design a resistance capacitance discharge isolation circuit for USB shell.

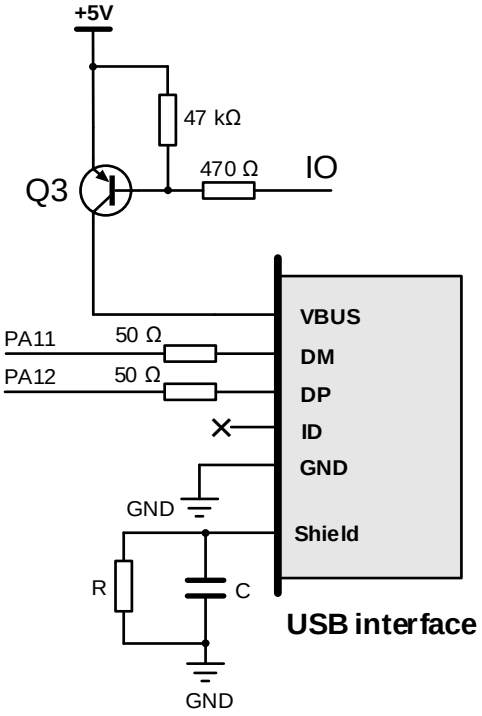
Figure 2-17. Recommended USB Device reference circuit



Recommend: R = 1MΩ, C = 4700pF.

Note: By configuring VBUSIG control bit in USBFS_GCCFG register, VBUS can not be connected to PA9, PA9 can be released for other functions. If VBUSIG control bit is not configured, PA9 needs to be connected to external VBUS.

Figure 2-18. Recommended USB Host reference circuit

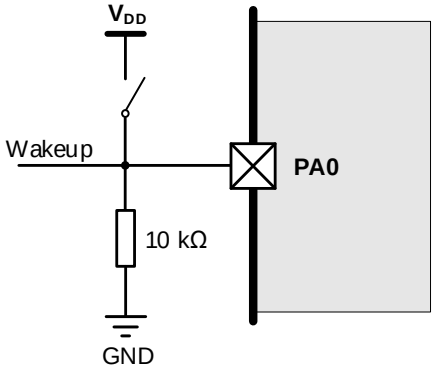


Recommend: R = 1MΩ，C = 4700pF。

2.5.4. Standby mode wake-up circuit

The GD32VF103 series supports three low power consumption modes: sleep mode, deep sleep mode, and standby mode. Standby mode has the lowest power consumption and requires the longest wake-up time. Wake up from Standby mode can be realized through the rising edge of WKUP pin. At this time, it is not necessary to configure the corresponding GPIO, just configure the WUPEN bit in the PMU_ CS register is sufficient. The reference circuit of WKUP wake-up pin is designed as follows.

Figure 2-19. Recommended Standby external wake-up pin circuit design



Note: In the circuit design of this mode, it should be noted that if there is a series resistance between PA0 and V_{DD}, additional power consumption may be increased.

2.6. Download debugging circuit

The GD32VF103 series kernel only supports the JTAG debug interface, not the SWD interface. JTAG interface standard is 20 pin interface, including 5 signal interfaces.

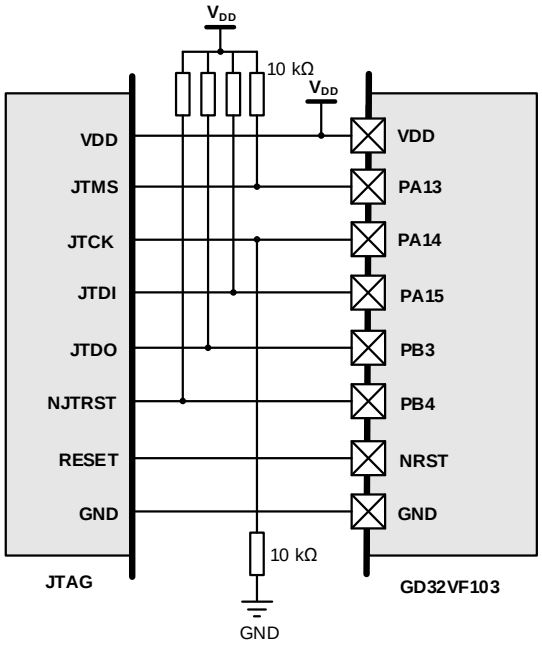
Note: After reset, the debugging related port is in the input PU / PD mode, where:

PA15: JTDI is pull-up mode;
PA14: JTCK is a pull-down mode;
PA13: JTMS is pull-up mode;
PB4: NJTRST is pull-up mode;
PB3: JTDO is floating mode.

Table 2-4. Download debugging interface assignment

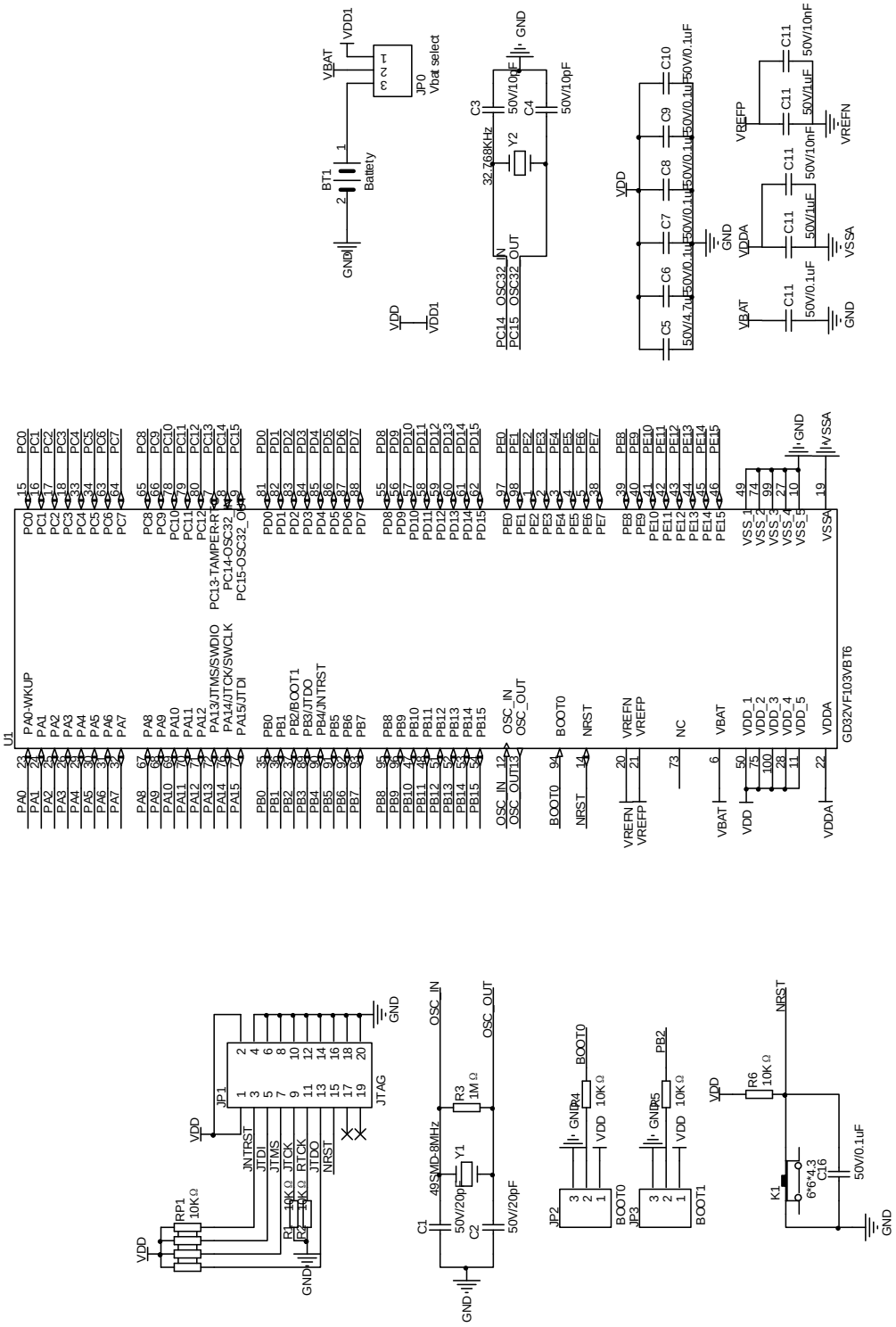
Standby function	GPIO port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-20. Recommended JTAG wiring reference design



2.7. Reference schematic design

Figure 2-21. GD32VF103 recommend reference schematic design



3. PCB Layout design

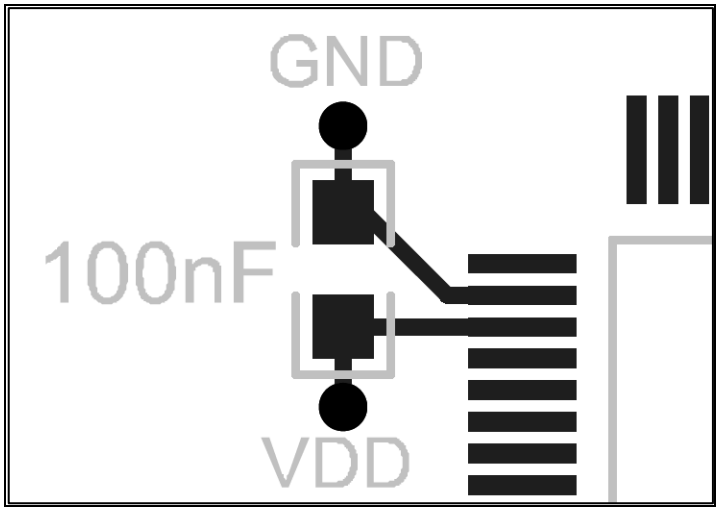
In order to enhance the functional stability and EMC performance of MCU, it is not only necessary to consider the performance of supporting peripheral components, but also important in PCB Layout. In addition, if conditions permit, PCB design scheme with independent GND layer and independent power supply layer shall be selected as far as possible to provide better EMC performance. If conditions do not permit, independent GND layer and power supply layer cannot be provided, it is also necessary to ensure a good power supply and grounding design, such as making the integrity of GND plane below MCU as much as possible.For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping MCU away from these strong interference sources.

3.1. Power decoupling capacitor

The GD32VF103 series power supply has four power supply pins: V_{DD}, V_{DDA}, V_{REFP} and V_{BAT}. The 100nF decoupling capacitor can be made of ceramics, and the position should be as close to the power supply pin as possible. The power supply wiring shall be routed to MCU power supply pin after passing through the capacitor as far as possible. It is recommended to lay out via near the capacitor PAD.

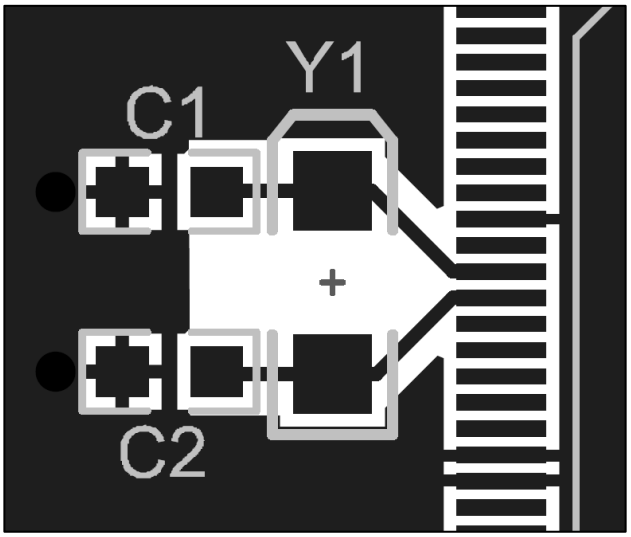
Figure 3-1. Recommended power supply pin decoupling Layout design



3.2. Clock circuit

GD32VF103 series clocks include HXTAL and LXTAL. Clock circuits (including crystals or crystal oscillators and capacitors) are required to be placed close to MCU clock pins, and clock wiring should be wrapped by GND as much as possible.

Figure 3-2. Recommended clock pin layout design (passive crystal)



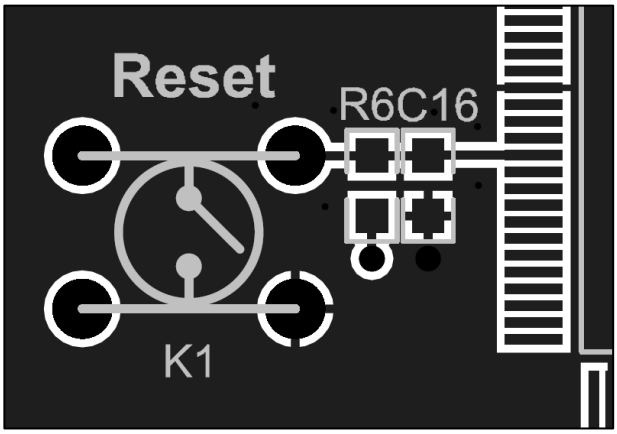
Note:

1. The crystal shall be as close as possible to the MCU clock pin, and the matching capacitor shall be as close as possible to the crystal.
2. The whole circuit shall be on the same layer with MCU as far as possible, and the wiring shall not cross the layer as far as possible.
3. The PCB area of the clock circuit shall not be empty as far as possible, and no wiring irrelevant to the clock shall be used.
4. High power, strong interference risk components and high-speed wiring shall be far away from clock crystal circuit as far as possible.
5. The clock cable shall be wrapped to ground for shielding.

3.3. Reset circuit

NRST wiring PCB layout reference is as follows:

Figure 3-3. Recommend NRST routing layout design



Note: The reset circuit resistance and capacitance shall be as close to the MCU NRST pin as possible, and the NRST wiring shall be as far away from the strong interference risk components and high-speed wiring as possible. If conditions permit, it is better to package

the NRST wiring to achieve better shielding effect.

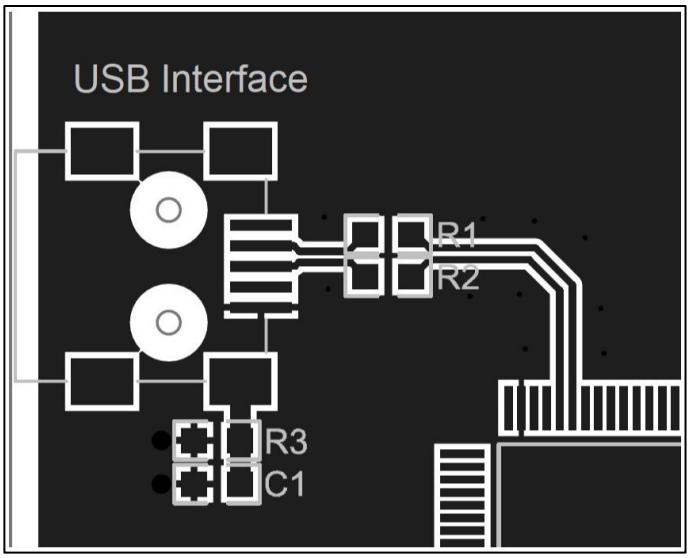
3.4. USB circuit

The USB module has two differential signal lines, DM and DP. It is recommended that the PCB wiring should have a characteristic impedance of 90 ohm. The differential wiring should strictly follow the rules of equal length and equal distance, and try to keep the wiring as short as possible. If the two differential lines are not equal in length, a serpentine wire can be used at the terminal to compensate for the short line.

Considering impedance matching, it is recommended that the series matching resistance should be about 50 Ω. When the USB terminal interface is far from the MCU, the series resistance should be increased appropriately.

USB differential wiring reference is as follows:

Figure 3-4. Recommend USB differential routing layout design



Recommend: R1 = R2 = 50Ω, R3 = 1MΩ, C = 4700pF.

Note:

1. The layout shall be reasonable to shorten the differential routing distance.
2. Give priority to drawing difference lines, and try not to exceed two pairs of vias on one pair of difference lines, which should be placed symmetrically.
3. Symmetrical parallel wiring, ensure that the two lines are closely coupled, and avoid 90 °, arc or 45 ° wiring.
4. The resistance capacitance, EMC and other devices connected to the differential wiring, or test points, shall also be symmetrical.

4. Package instruction

GD32VF103 series has four packaging forms, namely LQFP100, LQFP64, LQFP48 and QFN36.

Table 4-1. Description of package model

Ordering code	Package
GD32VF103TxU6	QFN36(6x6, 0.5 pitch)
GD32VF103CxT6	LQFP48(7x7, 0.5 pitch)
GD32VF103RxT6	LQFP64(10x10, 0.5 pitch)
GD32VF103VxT6	LQFP100(14x14, 0.5 pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Dec.16, 2022
1.1	1. Update section 2.1.2 to provide all package power supply design drawings, indicating the connection of relevant pins inside the chip 2. Update Figure 2-21 in section 2.7	Jun.21, 2023
1.2	1. Modified the description of adding capacitors externally to NRST in Section 2.2.3. 2. Delete ” If Bypass is not turned on, the requirements for the amplitude of the active crystal oscillator will be greatly reduced” in Section 2.3.1.	Sep.3, 2024
1.3	1. Refine the content related to power supply detection and reset, and add Section 2.2.	Dec.15, 2024

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