GigaDevice Semiconductor Inc.

GD32 MCU GPIO structure and precautions

Application Note
AN092

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1. Introduction

This article is specially provided for engineers who develop GPIO based on GD32 MCU. It mainly introduces the functional configuration, internal structure and the matters for attention when using GPIO in different scenarios. The purpose of this application notes is to help GD32 MCU users optimize the use of general-purpose input / output ports (GPIO), and correctly and quickly use GD32 MCU for product development.

GPIO, short for general-purpose input / output ports, can be configured with its output or input by software. The GPIO pin of GD32 can be connected with external devices to realize the functions of external communication, control and signal input. It is a common and most widely used module in GD32 MCU.

Each GPIO pin can be configured by software for output (push-pull or open drain), input, peripheral standby, or analog mode. Each GPIO pin can be configured in pull-up, pull-down or non pull-up/non pull-down mode.

GD32 MCU GPIO features:

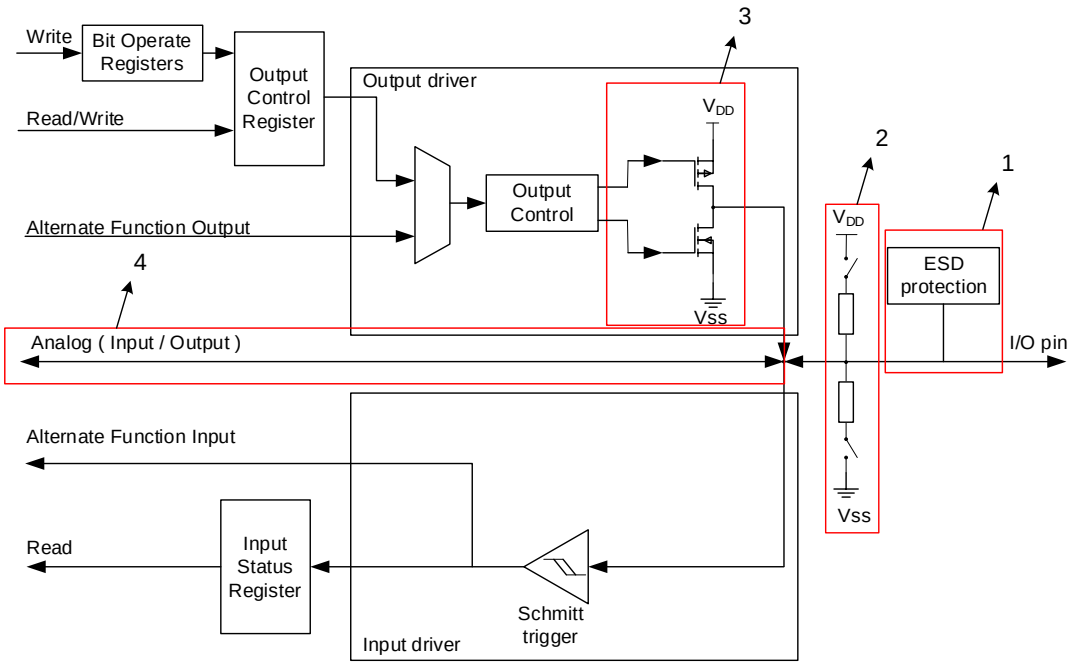
- Input / output direction control.
- Schmidt trigger input function
- Each pin has a weak pull-up/pull-down function.
- Push-pull/open drain output enable control.
- Set/reset output enable.
- External interrupts for programmable trigger edges - use EXTI to configure registers.
- Analog input/output configuration.
- Standby function input/output configuration.
- Port lock configuration.

For GD32, GPIO of some series MCU may have more functions, such as clock, I2C, SPI, CAN, USART, USB, ADC, DAC, etc. Before designing the circuit board, check th e data manual and user manual of the series to compare whether the GPIO used m eets the requirements.

2. GPIO structure

In GD32 MCU, there are usually two types of GPIO, non-5V tolerant IO and 5V tolerant IO(Some MCUs do not have 5VT pins, such as GD32A503xx series). The two types of GPIO are slightly different in structure. *Figure 2-1. Standard IO basic structure diagram*.

Figure 2-1. Standard IO basic structure diagram



I/O pin represents the I/O pad of the chip, which is connected to the external circuit, and other parts of the circuit are the internal circuit of the chip.

The upper part of the block diagram represents the output part of the IO circuit. When the IO uses its standby function to connect other internal peripherals, the relevant power output part of the circuit will also be shared. The bottom half of the block diagram shows the input circuit of the IO, which is also shared with other internal peripherals, such as the Schmidt flip-flop, as a backup function. The middle part of the block diagram, such as the circuit in red box 4, represents the analog input-output channel. The output of the analog channel (such as the DAC output) does not pass through the power output circuit, and the input does not pass through the Schmidt input circuit. The external circuit is directly connected to the internal analog peripheral through the IO pin.

Red box 3 represents the main power circuit of I/O output. Relevant control registers can be configured to control the conduction of the upper and lower MOS tubes to realize push-pull output or open-drain output.

Red box 2 represents the internal pull-up or pull-down circuit of the IO port. The internal pull-up or pull-down circuit of the input port can be realized through the configuration of relevant registers. The resistance value of the pull-up/pull-down resistor can be referred to the data manual, and the typical value is 40kΩ. If the PA10 pin pull-down resistance of GD32F425xx

is 10 kΩ, see the section GPIO characteristic in the data book for detailed data.

Red box 2 represents ESD protection circuit.

The ESD protection circuit of non-5VT IO is shown in ***Figure 2-2. Basic structure diagram of non-5VT IO pins*** shows that the ESD protection circuit forms two diodes respectively in V_{DD} and V_{SS} of IO. Obviously, if the voltage ratio of IO to V_{DD} is greater than the positive guide voltage drop of diode, or the voltage on IO is lower than the potential of V_{SS}, And the voltage difference is greater than the diode positive guide voltage, will generate a current from IO to V_{DD}, or from V_{SS} to IO.

The ESD protection circuit of 5VT IO is shown in ***Figure 2-3. Basic structure diagram of 5VT IO pin***. The 5VT IO pin is not connected to the internal protection diode of the power supply (V_{DD}).

Therefore, in actual use, if the pin is powered on first and the MCU is powered on later, the pin of 5VT is preferred to be used as the pin of external connection to power on first, to avoid the IO pin pulling down due to pin leakage. If standard IO pins must be selected, isolation measures such as triode should be used to prevent pin leakage.

Figure 2-2. Basic structure diagram of non-5VT IO pins

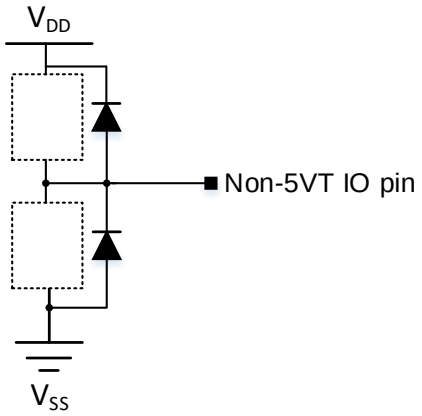
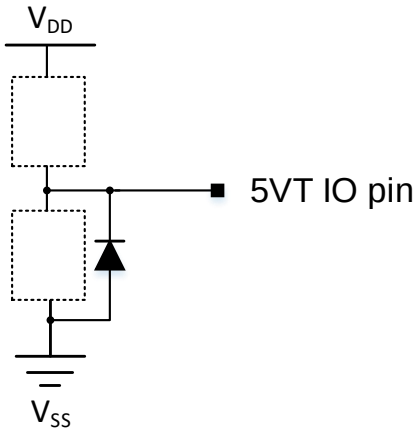


Figure 2-3. Basic structure diagram of 5VT IO pin



Note: The internal structure of 5VT IO is partially different from that of non-5VT IO.

3. Typical application scenarios and precautions

There are some precautions for using different types of IO. The following describes the typical application scenarios, features and precautions of different types of IO from the perspectives of input and output.

3.1. IO input

The first is the input voltage range of the IO port. The input voltage tolerance value represents the input voltage range that can be tolerated by the IO port, some GD32 MCU contain 5VT IO and non-5VT IO , as shown in ***Table 3-1. Absolute maximum ratings*** in the data manual, 5VT IO has different characteristics than non-5VT IO.

Table 3-1. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input voltage on 5V tolerant pin(1)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V

(1) V_{IN} maximum value cannot exceed 5.5 V.

For the IO port input scenario, note the following:

1. For 5VT IO, when V_{DD} = 0 (when the MCU is not powered on), the pin input voltage cannot exceed 3.6V.
2. We need to carefully choose 5VT IO or non-5VT IO according to the voltage range of the external input signal of the IO port. If the input signal is greater than 5.5V, the signal should be adjusted into a suitable range and then sent to the IO port of the MCU.
3. The low level of GPIO input is ≤ $0.3V_{DD}$, and the high level of GPIO input is ≥$0.7V_{DD}$.
4. According to the typical structure of IO ports of different types described above, if the voltage on non-5VT IO is more than 0.3V larger than the voltage of V_{DD}, it may cause leakage of IO in ESD protection circuit to the diode conduction of V_{DD}, especially in the case that the MCU is not powered on and the IO port has already been charged. If 5VT IO is selected, the leakage from IO to V_{DD} will be avoided. Typically, if the IO is connected to the I2C bus, we need to select the 5VT pin.
5. When all I/Os of the MCU are powered on and no other configuration is performed, they work in the floating input mode by default, and the debug port is pull-up or pull-down mode. For details about pull-up or pull-down, see the user manual. Therefore, in some scenarios where a fixed level needs to be generated, if the MCU is reset from standby mode, the default input pull-down state of these I/O ports needs to be considered, and the default state will not change until the program reconfigures the state of these I/Os.
6. In order to achieve lower power consumption, especially in sleep mode and deep sleep mode, the unused IO needs to be configured as analog input, or configured as floating input state with external drop-down, or set as internal drop-down or drop-down. Note that when internal pull-down is used, external hardware pull-down is not required to avoid extra power consumption. External hardware cannot be pulled up (the IO not used here

also includes the IO not elicited on this wrapper). For GD32 low-power MCU products, the best power performance will also be achieved in run mode with Settings as described previously.

7. 5VT IO can input up to 5.5V only in input mode. When output mode is enabled, 5VT IO can no longer withstand 5.5V voltage. For details on the I/O input voltage, refer to the V_{IN} parameter in the Datasheet Common Operating Conditions Table.
8. Only when the analog function is not enabled on the pin, 5VT IO can input the maximum voltage of 5.5V. If some analog input functions (ADC input active, COMP input, OPAMP input) are enabled on the 5VT IO, then the maximum operating voltage on the pin cannot exceed min(V_{DDA}, V_{REFP}) + 0.3V.

3.2. IO output

There are also some important points to note in the IO output scenario:

1. There is a very significant relationship between the open-drain output voltage and the output on-load current. Generally, when the output of IO is high, the higher the load is, the lower the output high level will be. Similarly, when the output of IO is low, the greater the current flowing into IO is, the higher the output low level will be.
2. For the model with backup domain in MCU, some IO works in the power supply of the backup domain, and the carrying capacity of these IO is limited. It is recommended to set the IO speed parameter of these IO to the lowest speed (generally 2MHz). For example, the four pins PC13, PC14, PC15 and PI8 in GD32F4xx series are different for different series with weak driving ability. Detailed information can be queried in the data manual of this series.
3. The passable current of GPIO is related to the IO configuration speed. At present, the maximum passable current of IO of all GD32 MCU is 25 mA (excluding pins working in the backup domain), and the source current and sink current of GPIO shall not exceed 25 mA. When GPIO speed configuration is low, its source current and sink current capacity may not reach 25 mA.
4. Some GD32 MCU contain I/O compensation units, such as E50x series. By default, the I/O compensation unit is not used. When the output speed of the I/O port is greater than 50MHz, you are advised to use the I/O compensation unit to control the slope of the I/O port to reduce the impact of I/O port noise on the working power supply.
5. The overshoot of IO will increase with the increase of the speed of IO port during the high and low level conversion. The overshoot can be reduced by reducing the speed of IO port.
6. The high and low level of GPIO output is not absolute zero or V_{DD}, but varies with the speed of IO configuration, V_{DD} voltage and output current. As shown in ***Table 3-2. GD32F425xx GPIO DC characteristics***, the data table of GD32F425xx GPIO output high and low levels varies with these variables.

Table 3-2. GD32F425xx GPIO DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IO_Speed:level 3						
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	—	—	0.11	V
		V_{DD} = 3.3 V	—	—	0.10	
		V_{DD} = 3.6 V	—	—	0.10	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	—	—	0.29	
		V_{DD} = 3.3 V	—	—	0.27	
		V_{DD} = 3.6 V	—	—	0.26	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	2.46	—	—	
		V_{DD} = 3.3 V	3.18	—	—	
		V_{DD} = 3.6 V	3.48	—	—	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	2.22	—	—	
		V_{DD} = 3.3 V	2.98	—	—	
		V_{DD} = 3.6 V	3.29	—	—	
IO_Speed:level 2						
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	—	—	0.16	V
		V_{DD} = 3.3 V	—	—	0.14	
		V_{DD} = 3.6 V	—	—	0.14	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	—	—	0.43	
		V_{DD} = 3.3 V	—	—	0.37	
		V_{DD} = 3.6 V	—	—	0.36	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	2.40	—	—	
		V_{DD} = 3.3 V	3.12	—	—	
		V_{DD} = 3.6 V	3.44	—	—	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	2.05	—	—	
		V_{DD} = 3.3 V	2.84	—	—	
		V_{DD} = 3.6 V	3.17	—	—	
IO_Speed:level 1						
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	—	—	0.28	V
		V_{DD} = 3.3 V	—	—	0.28	
		V_{DD} = 3.6 V	—	—	0.24	
	(I_{IO} = +15 mA)	V_{DD} = 2.6 V	—	—	0.57	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 3.3 V	—	—	0.66	
		V_{DD} = 3.6 V	—	—	0.64	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	2.23	—	—	
		V_{DD} = 3.3 V	3.00	—	—	
		V_{DD} = 3.6 V	3.31	—	—	
	(I_{IO} = +15 mA)	V_{DD} = 2.6 V	1.83	—	—	
	High level output voltage for an IO Pin	V_{DD} = 3.3 V	2.45	—	—	
		V_{DD} = 3.6 V	2.81	—	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	(I_{IO} = +20 mA)					
IO_Speed:level 0						
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.6 V	—	—	0.17	V
		V_{DD} = 3.3 V	—	—	0.15	
		V_{DD} = 3.6 V	—	—	0.15	
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.6 V	—	—	0.80	
		V_{DD} = 3.3 V	—	—	0.63	
		V_{DD} = 3.6 V	—	—	0.60	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.6 V	2.38	—	—	
		V_{DD} = 3.3 V	3.12	—	—	
		V_{DD} = 3.6 V	3.42	—	—	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.6 V	1.45	—	—	
		V_{DD} = 3.3 V	2.48	—	—	
		V_{DD} = 3.6 V	2.83	—	—	

3.3. Other considerations

To better improve the performance of GD32 MCU in some typical application scenarios, note the following when using GPIO of GD32 MCU:

1. The ADC input pins of some series GD32 MCU are standard IO pins. Attention should be paid to avoid the ADC input voltage exceeding VDD+0.3V, otherwise the ADC sampling may be abnormal due to leakage; When using the ADC module, all ADC pins shall not introduce negative voltage, otherwise the ADC sampling will be inaccurate.
2. The V_{BAT} pin allows the GD32 backup domain to be powered from an external voltage source (battery or capacitor). When the GD32 microcontroller is powered only by the V_{BAT} pin, only GPIO in the backup domain will work. The GPIO driver of the backup domain is weak and varies according to the backup domain. For applications without external batteries, it is recommended to connect the V_{BAT} pin to the V_{DD} pin after grounding through the 100nF's external ceramic decoupling capacitor.
3. To improve EMC performance and to avoid the risk of leakage current from floating input I/O pins, it is recommended to use hardware pull-up or pull-down for unused I/O pins.
   The input circuit of the I/O can be simplified as shown in ***Figure 3-1. Simplified diagram of I/O input circuit***, where Pxx represents a specific pin of the MCU.
   Ip represents the leakage from V_{DD} to Pxx, and In represents the leakage from Pxx to V_{SS}. Both Ip and In include not only the internal device leakage of the chip but also the leakage that may be introduced on the PCB, as well as the leakage that may be introduced during testing. The relative magnitude of Ip and In determines the voltage value of Pxx. If Ip is much greater than In, then Pxx is approximately equal to V_{DD}; if Ip is much less than In, then Pxx is approximately equal to V_{SS}; if the difference between Ip and In is not very large, then the voltage of Pxx is some intermediate value between V_{SS} and V_{DD}.
   When the I/O is configured in floating input mode, switches SW1 and SW2 are closed. If

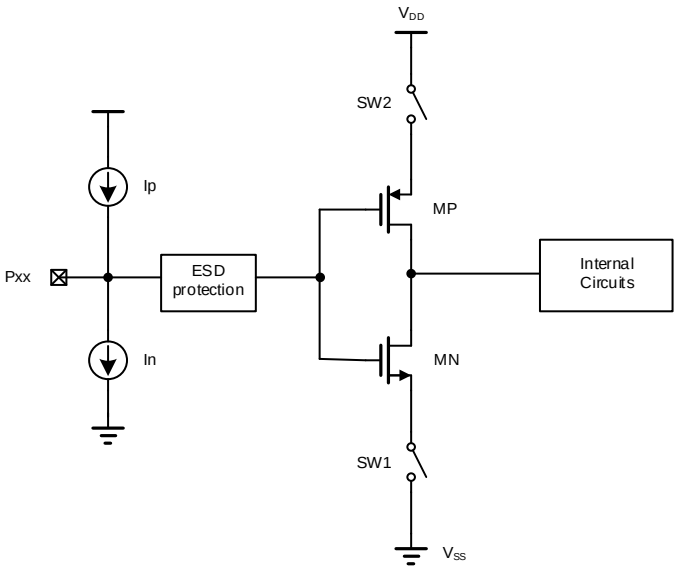
Pxx is not driven by an external voltage, the voltage of Pxx can be any value between V_{SS} and V_{DD}. Assuming in ***Figure 3-1. Simplified diagram of I/O input circuit*** that the threshold voltage of MN is V_{THN} and the threshold voltage of MP is V_{THP}, when the voltage of Pxx is between V_{THN} and (V_{DD} - V_{THP}), both MN and MP are turned on simultaneously, which may result in a significant leakage current between V_{DD} and V_{SS}.

When the I/O is configured in pull-up mode, pull-down mode, or analog mode, MP and MN will not conduct at the same time, preventing any leakage current between V_{DD} and V_{SS}.

Additionally, another possible leakage scenario is that when the IO is configured in a floating input mode, if P_{XX} is subjected to noise interference, it may cause the inverter composed of MP and MN in the diagram and the subsequent logic gates to continuously toggle, resulting in dynamic power consumption by the chip.

It should be noted that due to factors such as process variations, temperature, the magnitude of V_{DD}, and differences in the number and type of components connected to each pin, the specific magnitudes of Ip and In can vary greatly between different pins, different chips, and different batches. This is also the reason why different chips, even when their pins are configured as floating inputs, have varying levels of power consumption, with some being lower and others being higher.

Figure 3-1. Simplified diagram of I/O input circuit



4. In multiple groups, only one I/O port of the same label PIN can be configured as external interrupt. For example, only one of the three I/O ports in PA0, PB0, and PC0 can be configured as external interrupt.

4. Revision history

Table 4-1. Revision history

Revison No.	Description	Date
1.0	Initial Release	Dec.16, 2022
1.1	Updated charts and descriptions	Mar.29, 2023
1.2	Remove Figure 2-1 Analog channel switch	Jun.21, 2023
1.3	Add I/O floating input leakage risk warning and principle introduction	July.15, 2024
1.4	Supplemental Introduction to the Principle of Leakage Current in Floating Input IO	Sept.20, 2024
1.5	In Figure 2-1, change Vdd to VDD and remove the pull-up and pull-down resistors in the input drive box.	Dec.15, 2024

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