# GigaDevice Semiconductor Inc.

# Device limitations of GD32E50x

# Errata Sheet

Revision 1.6

(Jun. 2025)

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# 1. Introduction

This document applies to GD32E50x product series, as shown in ***Table 1-1. Applicable products***. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

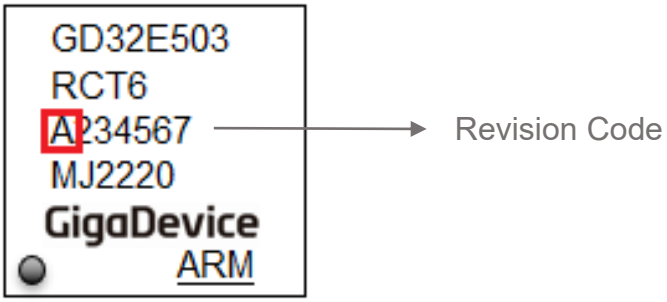
**Table 1-1. Applicable products**

| Type | Part Numbers |
|---|---|
| MCU | GD32E503xx series |
| | GD32E505xx series |
| | GD32E507xx series |
| | GD32E508xx series |
| | GD32EPRTxx series |

## 1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in ***Figure 1-1. Device revision code of GD32E50x***.

**Figure 1-1. Device revision code of GD32E50x**




## 1.2. Summary of device limitations

The device limitations of GD32E50x are shown in ***Table 1-2. Device limitations***, please refer to section 2 for more details.

**Table 1-2. Device limitations**

| Module | Limitations | Workaround | |
|---|---|---|---|
| | | Rev. Code A | Rev. Code B |
| PMU | ***Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode*** | N | N |
| | ***Power consumption will increase when using LVD detection*** | Y | Y |

| Module | Limitations | Workaround | |
|---|---|---|---|
| | | Rev. Code A | Rev. Code B |
| | *in standby mode* | | |
| RCU | *MCU cannot be waked up from Deepsleep mode when DSLP_HOLD bit is set* | Y | Y |
| GPIO | *When the OSCIN and OSCOUT pins are remapped to PD0 / PD1 pins, PD0 / PD1 can be used as a normal GPIO function but cannot be used as an EXTI function* | Y | -- |
| | *The square wave or negative voltage on PD5 will affect the stability of core voltage* | Y | Y |
| DAC | *There is leakage between the DAC output pin and the VREFP pin* | Y | -- |
| TIMER | *Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function* | Y | Y |
| SHRTIMER | *In certain cases, DLL calibration will lose SET / RESET* | N | -- |
| | *Unable to enter fault interrupt* | N | -- |
| | *SHRTIMER works abnormally when the update source is configured* | N | -- |
| | *Wave loss occurs when using DLL to multiply frequency of SHRTIMER* | N | N |
| | *When using the update event function, there are wave loss, counter abnormal reset, and counter overperiod counting problems* | N | -- |
| I2C | *Read one more data because the BTC flag was not cleared* | Y | Y |
| | *When I2C2 works in 7/10 address slave mode, receiving an abnormal timing will cause the SDA line to stuck* | N | N |
| SQPI | *The power consumption in Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode is high when using external PSRAM* | Y | Y |
| | *The power consumption in standby mode is high when using external PSRAM* | Y | Y |
| SDIO | *In SDIO multi-line mode (4-bit or 8-bit data width), after completing data reception, if the FIFO is not cleared in time and subsequent data arrives on the data line, it will cause the STBITE error to remain set state* | Y | Y |
| EXMC | *NE timing can not satisfy the requirement when using NAND pre-waiting function* | Y | Y |
| CAN | *RS bit is 1 in default* | N | N |
| ENET | *The TBU interrupt fails to set the NI state* | Y | -- |
| USB | *When the LPM slave machine is connected to the PC host, if the previous control transaction of the LPM transaction is STALL, the LPM transaction will also be STALL* | Y | Y |

| Module | Limitations | Workaround | |
|---|---|---|---|
| | | Rev. Code A | Rev. Code B |
| | ***Failure of data transfer in high speed synchronous pressure test*** | Y | Y |

**Note:**

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

# 2. Descriptions of device limitations

## 2.1. PMU

### 2.1.1. Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode

**Description & impact**

When reset the internal signal STBY_CTL to enter to standby mode, if the Tglitch is smaller than 100ns, which will cause the MCU cannot be waked up. The narrow glitch will result in incorrect Vcore voltage.

**Note:** The $T_{glitch}$ is the time between STBY_CTL low level and the wakeup signal (PA0 high level)

**Workarounds**

Not available.

### 2.1.2. Power consumption will increase when using LVD detection in standby mode

**Description & impact**

When the LVD detection function is enabled, the standby power consumption will increase due to LVD detection function cannot be automatically disabled in standby mode.

**Workarounds**

The application program needs to disable LVD detection before entering standby mode.

## 2.2. RCU

### 2.2.1. MCU cannot be waked up from Deepsleep mode when DSLP_HOLD bit is set

**Description & impact**

When the DSLP_HOLD bit in the DBG_CTL register is set, the MCU cannot be waked up after the MCU enters deepsleep mode.

**Workarounds**

When the DSLP_HOLD bit is set to enable low power debugging, the application program needs to switch the system clock to IRC8M before entering the deepsleep mode.

## 2.3. GPIO

### 2.3.1. When the OSCIN and OSCOUT pins are remapped to PD0 / PD1 pins, PD0 / PD1 can be used as a normal GPIO function but cannot be used as an EXTI function

**Description & impact**

When the external crystal function is not used and the OSCIN and OSCOUT pins are remapped to PD0 / PD1 pins, the remapped PD0 / PD1 can be used as a normal GPIO function but cannot be used as an EXTI function.

**Workarounds**

When the OSCIN and OSCOUT pins are remapped to PD0 / PD1 pins, the use of PD0 / PD1 for EXTI functionality is avoided in the application.

### 2.3.2. The square wave or negative voltage on PD5 will affect the stability of core voltage

**Description & impact**

Due to the sensitivity of the PD5 pin to interference signals, the square wave or negative voltage (exceeding $V_{SS}$-0.3V) on PD5 will affect the stability of core voltage (1.1V domain).

**Workarounds**

Avoid input square wave signal or negative voltage (exceeding $V_{SS}$-0.3V) signal on PD5 pin.

## 2.4. DAC

### 2.4.1. There is leakage between the DAC output pin and the VREFP pin

**Description & impact**

When the DAC is disabled and the $V_{DD}$ voltage is 0.7V higher than the $V_{REFP}$ voltage, the DAC output pin (PA4 / PA5) has leakage to VREFP pin.

**Workarounds**

Ensure that the voltage difference between $V_{DD}$ and $V_{REFP}$ does not exceed 0.7V.

## 2.5. TIMER

### 2.5.1. Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function

**Description & impact**

When using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function, DMA transfers data 0x00 to TIMERx_CHyCV register which will result in the second data lost after data 0x00.

**Workarounds**

Use one of the following solutions:

1) Do not use data 0x00 in DMA transfer buffer.
2) Transfer the second data after the 0x00 twice.
3) Use the timer update event to trigger DMA transfer.

## 2.6. SHRTIMER

### 2.6.1. In certain cases, DLL calibration will lose SET / RESET

**Description & impact**

If the SET / RESET event occurs during DLL calibration,the SET / RESET event may be lost and has no effect on the output.

**Workarounds**

Not available.

### 2.6.2. Unable to enter fault interrupt

**Description & impact**

When a fault event from system fault or fault channel occurs, the corresponding interrupt cannot be generated.

**Workarounds**

Not available.

### 2.6.3. SHRTIMER works abnormally when the update source is configured

**Description & impact**

When SHRTIMER shadow registers are enabled, SHRTIMER works abnormally.

**Workarounds**

Not available.

### 2.6.4. Wave loss occurs when using DLL to multiply frequency of SHRTIMER

**Description & impact**

When using DLL to multiply frequency of SHRTIMER, sampling deviation may occur in the internal frequency multiplier, which results in SHRTIMER wave loss.

**Workarounds**

Not available.

### 2.6.5. When using the update event function, there are wave loss, counter abnormal reset, and counter overperiod counting problems

**Description & impact**

When the SHRTIMER update event function is used, problems such as wave loss, counter abnormal reset, counter overperiod counting, etc. occur.

**Workarounds**

Not available.

## 2.7. I2C

### 2.7.1. Read one more data because the BTC flag was not cleared

**Description & impact**

If an interrupt occurs before reading I2C_DATA register when RBNE flag is set and BTC flag is reset, I2C will read an additional data if BTC flag is set during the interrupt processing because the read data operation can not clear the BTC flag.

**Note:** This limitation applies to I2C0 / I2C1.

**Workarounds**

Use one of the following solutions:

1) Using interrupt method to read the I2C_DATA register (need higher interrupt priority).
2) Using DMA method to read the I2C_DATA register (recommend).

### 2.7.2. When I2C2 works in 7/10 address slave mode, receiving an abnormal timing will cause the SDA line to stuck

**Description & impact**

When the I2C is operating as a slave device in 7-bit address mode and the I2C master simulates I2C communication via IO. If the master sends the following sequence, the I2C slave will enter an error state, causing it to malfunction and the SDA line to remain low:

Start + 10-bit Match Head Address + Start + 7-bit Address Read + Wait ACK + Start

When the I2C is operating as a slave device in 10-bit address mode and the I2C master simulates I2C communication via IO. If the master sends the following sequence, the I2C slave will enter an error state, causing it to malfunction and the SDA line to remain low:

Start + 10-bit Mismatch Head Address + Start
or
Start + 10-bit Match Head Address + Wait ACK + 10-bit Mismatch 8-bit Address + Start

**Note:** This limitation applies to I2C2.

**Workarounds**

Software periodically checks the status of the SDA line. If SDA is detected to be stuck low, reinitialize the I2C module.

## 2.8. SQPI

### 2.8.1. The power consumption in Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode is high when using external PSRAM

**Description & impact**

The power consumption in Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode is high when using external PSRAM.

**Workarounds**

Before entering Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode, configure the unused GPIO into analog mode and reinitialize the corresponding GPIO after waking up .

### 2.8.2. The power consumption in standby mode is high when using external PSRAM

**Description & impact**

After MCU entered the standby mode, PF6 connected to PSRAM chip selection signal CEN also loses power, resulting in PSRAM could not enter the standby mode.

**Workarounds**

Switch standby mode to Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode.

## 2.9. SDIO

### 2.9.1. In SDIO multi-line mode (4-bit or 8-bit data width), after completing data reception, if the FIFO is not cleared in time and subsequent data arrives on the data line, it will cause the STBITE error to remain set state

**Description & impact**

In SDIO multi-line mode (4-bit or 8-bit data width), after completing data reception, if the FIFO is not cleared in time and subsequent data arrives on the data line, it will cause the STBITE error to remain set state.

**Workarounds**

Use one of the following solutions:

1) When using polling mode, software should check both the STBITE flag and the DTEND flag at the same time. The STBITE flag is considered valid only when STBITE is set and DTEND is not set. The reference code is as follows:

```
if ((RESET != sdio_flag_get(SDIO_FLAG_STBITE)) && \\
   (RESET == sdio_flag_get(SDIO_FLAG_DTEND))){
    /* user code */
    ....
}
```

2) When using interrupt mode, the interrupt function should process the DTEND flag before the STBITE flag, and the interrupt enable bit STBITEIE should be cleared within the code of handling the DTEND flag. The reference code is as follows:

```
void SDIO_IRQHandler(void){
    if((RESET != sdio_flag_get(SDIO_FLAG_DTEND)) && \\
       (0U != (SDIO_INTEN & SDIO_INTEN_DTENDIE))){
          sdio_interrupt_disable(SDIO_INT_STBITE);
           /* user code */
           ....
    }
    if((RESET != sdio_flag_get(SDIO_FLAG_STBITE)) && \\
       (0U != (SDIO_INTEN & SDIO_INT_STBITE))){
           /* user code */
```

```
            ....
        }
}
```

3) Instead of using CMD12 to stop the open transmission of data, the multiblock read uses CMD23 to notify the slave device in advance of the number of data blocks to be transmitted. Then when DTEND is set, there will be no more extra data sent to the data line from the slave.

## 2.10. EXMC

### 2.10.1. NE timing can not satisfy the requirement when using NAND pre-waiting function

**Description & impact**

For some EXMC_NCE-sensitive NAND Flash, NE timing can not satisfy the requirement when using NAND pre-waiting function. NE signal keeps the low level when EXMC_INTx is active.

**Workarounds**

Using general I/O port to simulate the NE timing to finish the NAND reading and writing, NE signal keeps the low level after starting reading or writing.

## 2.11. CAN

### 2.11.1. RS bit is 1 in default

**Description & impact**

When in default or receiving state, RS bit in CAN_STAT register is 1; When in the sending state, the RS bit is cleared to 0.

**Workarounds**

When using, pay attention to the above logic processing.

## 2.12. ENET

### 2.12.1. The TBU interrupt fails to set the NI state

**Description & impact**

The NI bit in ENET_DMA_STAT register cannot be set by TBU interrupt, which results in no

NI interrupt occurrence.

**Workarounds**

Polling the TBU bit in ENET_DMA_STAT register to get TBU status.

## 2.13. USB

### 2.13.1. When the LPM slave machine is connected to the PC host, if the previous control transaction of the LPM transaction is STALL, the LPM transaction will also be STALL

**Description & impact**

In the software code, the STALL operation will STALL both the IN and OUT directions of the control endpoint. If the OUT directions of the control endpoint is STALL, the next OUT control transaction will not be properly responded and will directly return to the STALL. However, SETUP transactions can be received normally. LPM transactions do not belong to SETUP transactions. LPM transactions are a special transaction, equivalent to OUT transactions, resulting in that they cannot be ACK normally.

**Workarounds**

Modify the code according to the USB requirements of different PCs to solve the problem.

### 2.13.2. Failure of data transfer in high speed synchronous pressure test

**Description & impact**

During a high-speed synchronous pressure test, the device does not respond to the IN and OUT token packets of the host after a period of time. As a result, data transmission is interrupted.

**Note:** This limitation applies to USB product certification phase.

**Workarounds**

Configure external crystal oscillator for high speed synchronous pressure test.

# 3. Revision history

**Table 3-1. Revision history**

| Revision No. | Description | Date |
|---|---|---|
| 1.0 | Initial Release | Dec.12 2022 |
| 1.1 | Update note of chapter 1.2 | Apr.4 2023 |
| 1.2 | Add PMU limitation, referring to chapter 2.1.1 | Nov.2 2023 |
| 1.3 | 1. Add limitations of Rev. Code B<br>2. Add RCU / GPIO / DAC / TIMER / I2C / EXMC / CAN / ENET peripherals limitations | Apr.24 2024 |
| 1.4 | Update GPIO limitation description & impact, referring to chapter 2.3.2 | Jun.27 2024 |
| 1.5 | 1. Update the description of GPIO limitation, refer to ***The square wave or negative voltage on PD5 will affect the stability of core voltage***<br>2. Add I2C limitation, refer to ***When SDA line interference causes garbled data on the I2C bus, it can lead to a stuck in the I2C2 slave device***<br>3. Update the description of USB limitation, refer to ***Failure of data transfer in high speed synchronous pressure test***<br>4. Delete SQPI limitation, ***Misaligned access to PSRAM causes the program to run out of track*** | Sep.1 2024 |
| 1.6 | 1. Update SHRTIMER workaround of Rev. Code B, refer to ***Table 1-2. Device limitations***<br>2. Update the description of SHRTIMER limitation, refer to ***Wave loss occurs when using DLL to multiply frequency of SHRTIMER***<br>3. Add SDIO limitation, refer to ***In SDIO multi-line mode (4-bit or 8-bit data width), after completing data reception, if the FIFO is not cleared in time and subsequent data arrives on the data line, it will cause the STBITE error to remain set state***<br>4. Update I2C limitations, refer to ***When I2C2 works in 7/10 address slave mode, receiving an abnormal timing will cause the SDA line to stuck*** | Jun.25 2025 |

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