GigaDevice Semiconductor Inc.

Device limitations of GD32E50x

Errata Sheet

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1. Introduction

This document applies to GD32E50x product series, as shown in ***Table 1-1. Applicable products***. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

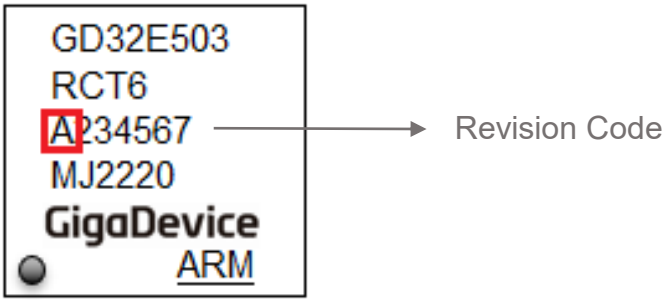
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32E503xx series
	GD32E505xx series
	GD32E507xx series
	GD32E508xx series
	GD32EPRTxx series

1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in ***Figure 1-1. Device revision code of GD32E50x***.

Figure 1-1. Device revision code of GD32E50x



1.2. Summary of device limitations

The device limitations of GD32E50x are shown in ***Table 1-2. Device limitations***, please refer to section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround	
		Rev. Code A	Rev. Code B
PMU	***Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode***	N	N
	Power consumption will increase when using LVD detection	Y	Y

Module	Limitations	Workaround	
		Rev. Code A	Rev. Code B
	in standby mode		
RCU	*MCU cannot be waked up from Deepsleep mode when DSLP_HOLD bit is set*	Y	Y
GPIO	*When PD0 / PD1 is shared with the OSCIN / OSCOUT pin, the external interrupt function cannot be used*	Y	--
	The square wave or negative voltage on PD5 will affect the stability of core voltage	N	N
DAC	*There is leakage between the DAC output pin and the VREFP pin*	Y	--
TIMER	*Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function*	Y	Y
SHRTIMER	*In certain cases, DLL calibration will lose SET / RESET*	N	N
	Unable to enter fault interrupt	N	N
	SHRTIMER works abnormally when the update source is configured	N	N
	Wave loss occurs when using DLL calibration	N	N
	When using the update event function, there are wave loss, counter abnormal reset, and counter overperiod counting problems	N	--
I2C	*Read one more data because the BTC flag was not cleared*	Y	Y
	When SDA line interference causes garbled data on the I2C bus, it can lead to a stuck in the I2C2 slave device	N	N
SQPI	*The power consumption in Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode is high when using external PSRAM*	Y	Y
	The power consumption in standby mode is high when using external PSRAM	Y	Y
EXMC	*NE timing can not satisfy the requirement when using NAND pre-waiting function*	Y	Y
CAN	*RS bit is 1 in default*	N	N
ENET	*The TBU interrupt fails to set the NI state*	Y	--
USB	*When the LPM slave machine is connected to the PC host, if the previous control transaction of the LPM transaction is STALL, the LPM transaction will also be STALL*	Y	Y
	Failure of data transfer in high speed synchronous pressure test	Y	Y

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. PMU

2.1.1. Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode

Description & impact

When reset the internal signal STBY_CTL to enter to standby mode, if the Tglitch is smaller than 100ns, which will cause the mcu cannot be waked up. The narrow glitch will result in incorrect Vcore voltage.

Note: The T_{glitch} is the time between STBY_CTL low level and the wakeup signal (PA0 high level)

Workarounds

Not available.

2.1.2. Power consumption will increase when using LVD detection in standby mode

Description & impact

When the LVD detection function is enabled, the standby power consumption will increase due to LVD detection function cannot be automatically disabled in standby mode.

Workarounds

The application programme need disable LVD detection before entering standby mode.

2.2. RCU

2.2.1. MCU cannot be waked up from Deepsleep mode when DSLP_HOLD bit is set

Description & impact

When the DSLP_HOLD bit in the DBG_CTL register is set, the MCU cannot be waked up after the MCU enters deepsleep mode.

Workarounds

When the DSLP_HOLD bit is set to enable low power debugging, the application programme need switch the system clock to IRC8M before entering the deepsleep mode.

2.3. GPIO

2.3.1. When PD0 / PD1 is shared with the OSCIN / OSCOUT pin, the external interrupt function cannot be used

Description & impact

When PD0 / PD1 is shared with the OSCIN / OSCOUT pins, the I/O port cannot use the external interrupt function when it is used as a common I/O port.

Workarounds

Not available.

2.3.2. The square wave or negative voltage on PD5 will affect the stability of core voltage

Description & impact

Due to the sensitivity of the PD5 pin to interference signals, the square wave or negative voltage (exceeding V_{SS}-0.3V) on PD5 will affect the stability of core voltage (1.1V domain).

Workarounds

Avoid input square wave signal or negative voltage (exceeding V_{SS}-0.3V) signal on PD5 pin.

2.4. DAC

2.4.1. There is leakage between the DAC output pin and the VREFP pin

Description & impact

When the DAC is disabled and the VDD voltage is 0.7V higher than the V_{REFP} voltage, the DAC output pin (PA4 / PA5) has leakage to VREFP pin.

Workarounds

The V_{REFP} voltage should be 0.7V less than the VDD voltage.

2.5. TIMER

2.5.1. Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function

Description & impact

When using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function, DMA transfers data 0x00 to TIMERx_CHyCV register which will result in the second data lost after data 0x00.

Workarounds

Use one of the following solutions:

1) Use timer update event to trigger DMA transfer.
2) The second data after data 0x00 is carried twice.

2.6. SHRTIMER

2.6.1. In certain cases, DLL calibration will lose SET / RESET

Description & impact

If the SET / RESET event occurs during DLL calibration,the SET / RESET event may be lost and has no effect on the output.

Workarounds

Not available.

2.6.2. Unable to enter fault interrupt

Description & impact

When a fault event from system fault or fault channel occurs, the corresponding interrupt cannot be generated.

Workarounds

Not available.

2.6.3. SHRTIMER works abnormally when the update source is configured

Description & impact

When SHRTIMER shadow registers are enabled, SHRTIMER works abnormally.

Workarounds

Not available.

2.6.4. Wave loss occurs when using DLL calibration

Description & impact

When using DLL to calibrate the SHRTIMER clock, sampling deviation may occur in the internal frequency multiplier, which results in SHRTIMER wave loss.

Workarounds

Not available.

2.6.5. When using the update event function, there are wave loss, counter abnormal reset, and counter overperiod counting problems

Description & impact

When the SHRTIMER update event function is used, problems such as wave loss, counter abnormal reset, counter overperiod counting, etc. occur.

Workarounds

Not available.

2.7. I2C

2.7.1. Read one more data because the BTC flag was not cleared

Description & impact

If an interrupt occurs before reading I2C_DATA register when RBNE flag is set and BTC flag is reset, I2C will read an additional data if BTC flag is set during the interrupt processing because the read data operation can not clear the BTC flag.

Note: This limitation applies to I2C0 / I2C1.

Workarounds

Use one of the following solutions:

1) Using interrupt method to read the I2C_DATA register (need higher interrupt priority).
2) Using DMA method to read the I2C_DATA register (recommend).

2.7.2. When SDA line interference causes garbled data on the I2C bus, it can lead to a stuck in the I2C2 slave device

Description & impact

When I2C2 operates as a slave and is configured in 7-bit addressing mode, if the I2C2 slave device matches 10-bit address header during the I2C2 slave addressing phase and interference on the SCL / SDA line that causes the next RESTART signal to be sent early (the 9th SCL clock for sending the ACK was not sent), and then the slave matches the 7-bit address, which can result in the I2C2 slave pulling the SDA line low, ultimately leading to the I2C2 slave stuck.

When I2C2 operates as a slave and is configured in 10-bit addressing mode, and if there is a mismatch in the 10-bit address header or the lower 8 bits of the 10-bit address during the I2C2 slave addressing phase, interference on the SCL / SDA line that causes the next RESTART / STOP signal to be sent early can result in the I2C2 slave pulling the SDA line low, ultimately leading to the I2C2 slave stuck.

Note: This limitation applies to I2C2.

Workarounds

Not available.

2.8. SQPI

2.8.1. The power consumption in Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode is high when using external PSRAM

Description & impact

In Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode, the MCU does not use the GPIO configuration to shut down early to reduce power consumption.

Workarounds

In Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode, the mcu reduces power consumption by configuring the GPIO to turn off early.

2.8.2. The power consumption in standby mode is high when using external PSRAM

Description & impact

After MCU entered the standby mode, PF6 connected to PSRAM chip selection signal CEN

also losts power, resulting in PSRAM could not enter the standby mode.

Workarounds

Switch standby mode to Deep-sleep / Deep-sleep 1 / Deep-sleep 2 mode.

2.9. EXMC

2.9.1. NE timing can not satisfy the requirement when using NAND pre-waiting function

Description & impact

For some EXMC_NCE-sensitive NAND Flash, NE timing can not satisfy the requirement when using NAND pre-waiting function. NE signal keeps the low level when EXMC_INTx is active.

Workarounds

Using general I/O port to simulate the NE timing to finish the NAND reading and writing, NE signal keeps the low level after starting reading or writing.

2.10. CAN

2.10.1. RS bit is 1 in default

Description & impact

When in default or receiving state, RS bit in CAN_STAT register is 1; When in the sending state, the RS bit is cleared to 0.

Workarounds

When using, pay attention to the above logic processing.

2.11. ENET

2.11.1. The TBU interrupt fails to set the NI state

Description & impact

The NI bit in ENET_DMA_STAT register cannot be set by TBU interrupt, which results in no NI interrupt occurrence.

Workarounds

Polling the TBU bit in ENET_DMA_STAT register to get TBU status.

2.12. USB

2.12.1. When the LPM slave machine is connected to the PC host, if the previous control transaction of the LPM transaction is STALL, the LPM transaction will also be STALL

Description & impact

In the software code, the STALL operation will STALL both the IN and OUT directions of the control endpoint. If the OUT directions of the control endpoint is STALL, the next OUT control transaction will not be properly responded and will directly return to the STALL.However, SETUP transactions can be received normally. LPM transactions do not belong to SETUP transactions. LPM transactions are a special transaction, equivalent to OUT transactions, resulting in that they cannot be ACK normally.

Workarounds

Modify the code according to the USB requirements of different PCs to solve the problem.

2.12.2. Failure of data transfer in high speed synchronous pressure test

Description & impact

During a high-speed synchronous pressure test, the device does not respond to the IN and OUT token packets of the host after a period of time. As a result, data transmission is interrupted.

Note: This limitation applies to USB product certification phase.

Workarounds

Configure external crystal oscillator for high speed synchronous pressure test.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Dec.12 2022
1.1	Update note of chapter 1.2	Apr.4 2023
1.2	Add PMU limitation, referring to chapter 2.1.1	Nov.2 2023
1.3	1. Add limitations of Rev. Code B 2. Add RCU / GPIO / DAC / TIMER / I2C / EXMC / CAN / ENET peripherals limitations	Apr.24 2024
1.4	Update GPIO limitation description & impact, referring to chapter 2.3.2	Jun.27 2024
1.5	1. Update the description of GPIO limitation, refer to ***The square wave or negative voltage on PD5 will affect the stability of core voltage*** 2. Add I2C limitation, refer to ***When SDA line interference causes garbled data on the I2C bus, it can lead to a stuck in the I2C2 slave device*** 3. Update the description of USB limitation, refer to ***Failure of data transfer in high speed synchronous pressure test*** 4. Delete SQPI limitation, ***Misaligned access to PSRAM causes the program to run out of track***	Sep.1 2024

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