GigaDevice Semiconductor Inc.

Methods to Reduce GD32L233 MCU Power Consumption

Application Note
AN106

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1. Introduction

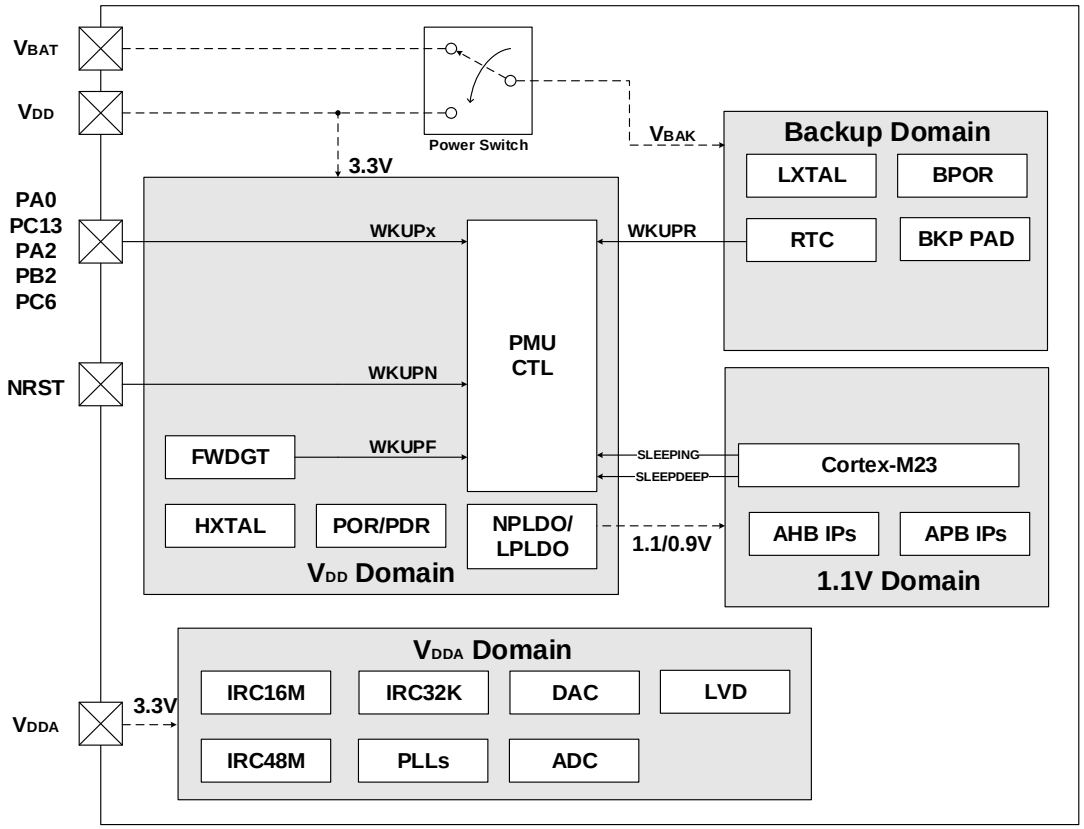
The GD32L233 family of devices is a 32-bit general-purpose microcontroller based on an Arm® Cortex®-M23 core with ultra-low power consumption. Its power module has a variety of power saving modes especially suitable for low power applications. This application note mainly provides a method to reduce power consumption for GD32L233 devices.

2. Reduce power consumption of GD32L233

2.1. Power supply architecture

Power consumption design is one of the most important issues of GD32L233 series products. The power management unit provides ten power saving modes that reduce power consumption and allow applications to strike the best compromise between CPU uptime requirements, speed, and power consumption. As shown in ***Figure 2-1. Power supply overview***. Power Domain overview, the GD32L233 series device has three power domains, including the V_{DD} / V_{DDA} domain, 1.1V domain, and backup domain. The V_{DD} / V_{DDA} domain is directly powered by the power supply. The LDO is embedded in the V_{DD} / V_{DDA} domain to power the 1.1V domain. There is a power switch in the backup domain, and when the V_{DD} power is off, the power switch can switch the power of the backup domain to the V_{BAT} pin, at which point the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. Power supply overview



LVD: Low Voltage Detector
NPLDO: Normal power Voltage Regulator
BPOR: V_{BAK} Power On Reset
POR: Power On Reset
LPLDO: Low power Voltage Regulator
PDR: Power Down Reset

2.2. Power-saving modes

After system reset or power reset, GD32L233 MCU is in full function state and all power domains are in power supply state. At this point, there are three ways to achieve lower power consumption: Slow down the system clock (HCLK, PCLK1 and PCLK2), turn off the clock of unused peripherals, in addition, ten power saving modes can achieve lower power consumption, they are Run mode, Run mode 1, Run mode 2, Sleep mode, Sleep mode 1, Sleep mode 2, Deep sleep mode, Deep sleep mode 1, Deep sleep Mode 2 and Standby mode. The wake up time of low power mode contributes a lot to power optimization and application flexibility, so the trade-off between low power mode consumption and the corresponding wake up time must be made.

Table 2-1. Power saving mode summary

Mode	Description	LDO	Entry	Wakeup	Wakeup status	Wakeup Latency
Run	no effect on all clocks, all power on	NPLDO on LPLDO on	system / power reset or wakeup from standby	-	-	-
Run1	system clock <= 16Mhz	NPLDO on LPLDO on	LDOVS set to 0.9V	clear LDVOS	-	-
Run2	system clock <= 2Mhz	NPLDO in low driver mode LPLDO on	LDOVS set to 0.9V and LDNP set to 1	clear LDVOS and LDNP	-	-
Sleep	Only CPU clock is off	NPLDO on LPLDO on	SLEEPDEEP = 0,WFI or WFE from Run	Any interrupt for WFI Any event (or interrupt when SEVONPEND is 1) for WFE	Run mode	-
Sleep1	Only CPU clock is off	NPLDO on LPLDO on	SLEEPDEEP = 0,WFI or WFE from Run1	Any interrupt for WFI Any event (or interrupt when SEVONPEND is 1) for WFE	Run1 mode	-
Sleep2	Only CPU clock is off	NPLDO in low driver mode LPLDO on	SLEEPDEEP = 0,WFI or WFE from Run2	Any interrupt for WFI Any event (or interrupt when SEVONPEND is 1) for WFE	Run2 mode	-
Deep-sleep	1. All clocks in the 1.1V domain are off 2. Disable IRC16M, IRC48M, HXTAL and PLLs	NPLDO in low driver mode or normal driver mode LPLDO on	SLEEPDEEP = 1, LPMOD = 00, WFI or WFE	Any interrupt from EXTI lines for WFI Any event(or interrupt when SEVONPEND is 1) from EXTI for WFE	Run / Run1 / Run2	IRC16M wakeup time, + Flash wakeup time
Deep-sleep 1	1. All clocks in the 1.1V domain are off	NPLDO off LPLDO on	SLEEPDEEP = 1, LPMOD = 01,	Any interrupt from EXTI lines for WFI	Run / Run1 / Run2	IRC16M wakeup time,

Mode	Description	LDO	Entry	Wakeup	Wakeup status	Wakeup Latency
	2. Disable IRC16M, IRC48M, HXTAL and PLLs 3. LPLDO instead of NPLDO		WFI or WFE	Any event(or interrupt when SEVONPEND is 1) from EXTI for WFE		+ NPLDO wakeup time+Flash wakeup time
Deep-sleep 2	1. All clocks in the 1.1V domain are off 2. Disable IRC16M, IRC48M, HXTAL and PLLs 3. LPLDO instead of NPLDO 4. COREOFF0 / SRAM1 / COREOFF1 power-off.	NPLDO off LPLDO on	SLEEPDEEP = 1, LPMOD = 10, WFI or WFE	Any interrupt from EXTI lines for WFI Any event(or interrupt when SEVONPEND is 1) from EXTI for WFE	Run / Run1 / Run2	IRC16M wakeup time, + NPLDO wakeup time+Flash wakeup time
Standby	1. The 1.1V domain is power off 2. Disable IRC16M, IRC48M, HXTAL and PLLs	NPLDO off LPLDO off	SLEEPDEEP = 1, LPMOD = 11, WFI or WFE	1. NRST pin 2. WKUP pins 3. FWDGT reset 4. RTC	Run	IRC16M wakeup time, + NPLDO wakeup time+Flash wakeup time
BKP_ONLY	All V_{DD} / 1.1V core domain power off	NPLDO off LPLDO off	V_{DD} off	V_{DD} on	Run	V_{DD} power on sequence

2.3. Methods to reduce power consumption

System clock configuration

Clock prescaler can be configured with clock frequencies in the AHB and APBx domains. In Run mode, the system clock value is reduced by a clock pre-divider to provide the required clock for the peripherals and to avoid power loss due to overclocking. When peripherals are not in use, power consumption is further reduced through APBx and AHB gated clock disabling.

Peripheral clock gating

The more peripherals are activated, the more power is consumed. By controlling the clock that does not use peripherals, energy saving is achieved.

I/O configuration

All unused pins should be configured as analog inputs, in which case the Schmidt trigger is disabled and each I / O consumes zero, avoiding the creation of additional current. For output,

the lowest I / O speed is recommended. Do not activate the pull-up or pull-down configuration, if it is not necessary. Users also need to disable clock output pins when they are not needed.

Using Direct Memory Access (DMA)

Peripherals can access data through DMA, which not only improves performance but also reduces power consumption. Before the DMA transfer ends, the CPU can enter sleep mode to achieve lower power consumption for the application.

Use low power mode

Entering low power mode reduces average application power consumption. In the management of power mode switching, the requirements of application power consumption, wake up source, wake up time and peripheral operation are considered. In low power mode, if the GPIO has external component input / output, you are advised to set the input to pull-up / pull-down and output push-pull to ensure that the GPIO stays stationary when it is idle.

Use low-power functional peripherals

Some of the GD32L233 peripherals feature low power consumption, such as LPTIMER and LPUART, which can achieve the required functions and performance while minimizing the power consumption. LPTIMER is a 32-bit timer that can operate in all power modes except Standby mode. Low power universal synchronous asynchronous receiver transmitter (LPUART) provides a low power flexible and convenient serial data exchange interface.

Set a low core voltage

The LDO (voltage regulator) powers the internal digital power. Setting a low core voltage is a simple and straightforward method to reduce power consumption. LDO that power the 1.1V domain and remain enabled after reset can be configured to work in different states: It includes Sleep mode (1.1V fully powered state, 0.9V fully powered state and low power state), Deep sleep mode / Deep sleep mode 1 / Deep sleep mode 2 (fully powered state or low power state) and standby mode (off state). In standby mode, the 1.1V domain is directly closed to greatly reduce power consumption, but the register content in the domain is lost, including internal RAM.

Execute code from the SRAM

When the MCU is operating at normal or low power, code is executed from the SRAM and the flash memory can go into sleep / power down mode, further reducing power consumption.

Shut down SRAM1

SRAM1 (0x20004000~0x20007FFF) can be powered off independently. SRAM1 is powered on by default after the system is reset. In order to reduce the power consumption of Run mode / Run mode 1 / Run mode 2, SRAM1 can be powered off. To further reduce the power consumption of low power modes (Sleep mode / Sleep Mode 1 / Sleep mode 2 / Deep sleep mode / Deep sleep mode 1 / Deep sleep mode 2), SRAM1 can be powered off before entering low power mode.

COREOFF1 Power domain is powered off

COREOFF1 domain can be powered off separately. COREOFF1 domain is powered off by default after the system is reset. The COREOFF1 domain needs to be powered on when the COREOFF1 domain module is used. To reduce the power consumption of Run mode / Run Mode 1 / Run Mode 2, power off the COREOFF1 domain. To further reduce the power consumption of low power modes (Sleep mode / Sleep Mode 1 / Sleep mode 2 / Deep sleep mode / Deep sleep mode 1 / Deep sleep mode 2), the COREOFF1 domain can be turned off before entering low power mode. COREOFF1 power domain contains the CAU module.

3. Summary

Embedded programs need to reduce power consumption when executing programs for complex real-time applications. For a given manufacturing process and wafer area, power consumption is largely determined by two dynamically controlled factors: voltage and frequency. In GD32L233 devices, LDO provides a fixed voltage for most logic circuits to minimize power consumption, while clock sources, cascaded clock prescaler, gating techniques, and peripheral clock management allow only necessary logic gates to activate. All these methods can reduce power consumption in operating mode. At the same time, the performance and power consumption of various power saving modes are considered to provide users with flexible choices.

4. Revision history

Table 4-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.7, 2023

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