GigaDevice Semiconductor Inc.

GD32F20x Hardware Development Guide

Application Note
AN107

Revision 1.2

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1.   Introduction

The article is specially provided for developers of 32-bit general-purpose MCU GD32F20x series based on Arm® Cortex®-M3 architecture. It provides an overall introduction to the hardware development of GD32F20x series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32F20x series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32F20x series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32F20x series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32F20x series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32F20x series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32F20x series.
6. Reference circuit and PCB Layout design, mainly introduces GD32F20x series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32F20x series.

This document also satisfies the minimum system hardware resources used in application development based on GD32F20x series products.

Table 1-1. Applicable Products

Type	Part Numbers
MCU	GD32F205xx series
	GD32F207xx series

2.   Hardware design

2.1.   Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32F20x series products is 2.6 V ~ 3.6 V. For GD32F20x series, there are three power domains, including V_{DD} / V_{DDA} domain, 1.2 V domain, and Backup domain, as is shown in ***Figure 2-1. GD32F20x Power supply overview***. The V_{DD}/V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.2 V domain. The backup domain power supply V_{BAK} can be powered by V_{DD} or V_{BAT} through the power switch Power Switch. When the V_{DD} power supply is turned off, the power switch can switch the power supply of the backup domain to the V_{BAT} pin. At this time, the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. GD32F20x Power supply overview

LVD: Low Voltage Detector   LDO: Voltage Regulator   BPOR: V$_{BAK}$ Power On Reset
POR: Power On Reset   PDR: Power Down Reset   BREG: Backup registers
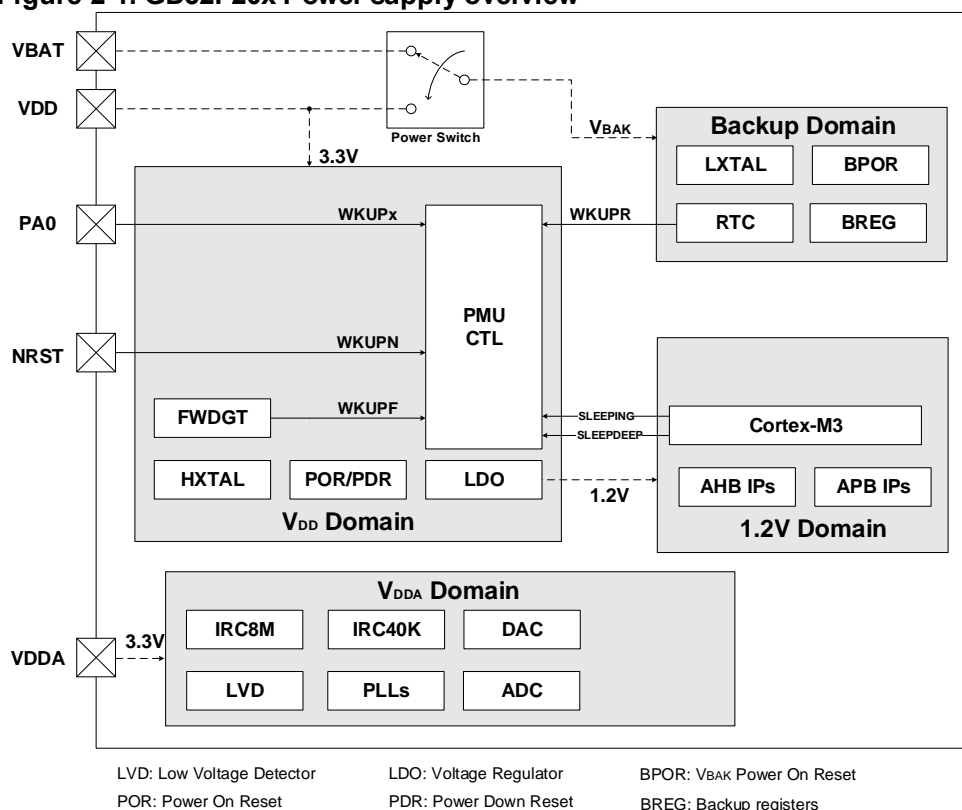
2.1.1.   Backup domain

The backup domain supply voltage range is 1.8V ~ 3.6V. In order to ensure the content of the Backup domain registers and the RTC supply, when V_{DD} supply is shut down, V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or by another source. The power switch is controlled by the Power Down Reset circuit in the V_{DD} / V_{DDA} domain. If there is no external battery-powered application, it is recommended to connect the V_{BAT} pin to the ground through a 100nF capacitor and then connect it to the V_{DD} pin.

Note: If the V_{BAT} pin is left floating, the Power Switch will switch V_{BAK} to V_{DD} after the MCU is powered on, and the internal V_{DD} will directly supply power to the Backup domain.

2.1.2. V_{DD}/V_{DDA} domain

The V_{DD} / V_{DDA} power domain supplies power to all areas except the backup domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two is required to be less than 300mV (the internal VDDA and VDD are connected by back-to-back diodes). To avoid noise, VDDA can be connected to VDD through an external filter circuit, and the corresponding VSSA can be connected to VSS through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. There is a VREFP and VREFN pin (2.4 V ≤ V_{REFP} ≤ V_{DDA}, V_{REFN} = V_{SSA}) for ADC independent power supply on the large package.

- The package chips with 100 pins and more contain VREFP and VREFN. VREFP can use an external reference power supply, or can be directly connected to VDDA, and VREFN must be connected to VSSA.
- The 64-pin package chip has no VREFP and VREFN, it is directly connected to VDDA and VSSA internally, and all analog modules are powered by VDDA (including ADC/DAC)

2.1.3. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one VDD pin needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF).
- The VDDA pin must be connected with an external capacitor (10nF+1uF ceramic capacitor is recommended).
- The VBAT pin must be connected to an external battery (1.8 V ~ 3.6 V). If there is no external battery, it is recommended to connect the VBAT pin to the ground through a 100nF capacitor and then connect it to the VDD pin.
- VREFP pin can be directly connected to VDDA. If a separate external reference voltage is used on VREFP (2.4V ≤ V_{REFP} ≤ V_{DDA}, V_{REFN} = V_{SSA}), a 10nF+1uF ceramic capacitor must also be connected to ground on the VREFP pin.

Figure 2-2. GD32 F20x Recommended Power Supply Design
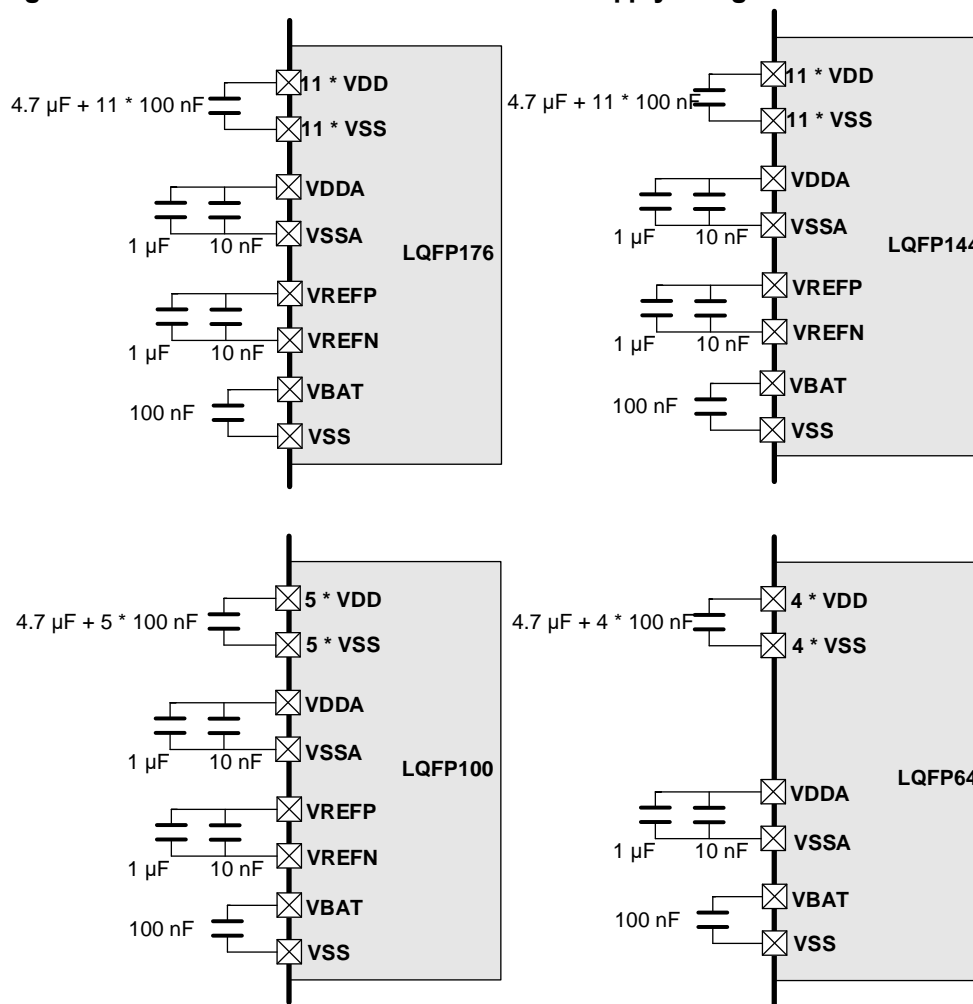
Note:

1、 All decoupling capacitors must be placed close to the corresponding VDD, VDDA, VREFP, VBAT pins of the chip.

2、 When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.

3、 LQFP64: VREFN and VSSA are connected internally, VREFP and VSS are connected internally.

4、 VBAT can be directly connected to VDD, or it can be connected to an external battery according to the actual application.

2.2.   Power Detection and Reset

In this section, the default VDD and VDDA pins remain connected and are powered by the same power supply.

GD32F20x series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain when the power is turned on.

The MCU reset source can be searched by the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register:

Figure 2-3. RCU_RSTSCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
LP RSTF	WWDGT RSTF	FWDGT RSTF	SW RSTF	POR RSTF	EP RSTF	OBL RSTF	RSTFC	V12 RSTF				Reserved				
r	r	r	r	r	r	r	rw	r								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
					Reserved									IRC40K STB	IRC40K EN	
														r	rw	

MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20μs.

Figure 2-4. System Reset Circuit
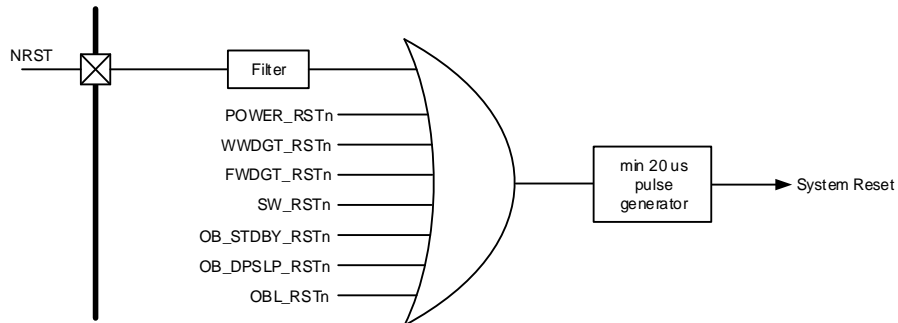
2.2.1. LVD

The function of LVD is to detect whether the V_{DD}/V_{DDA} supply voltage is lower than the low voltage detection threshold (2.2 V ~ 2.9 V), which is configured by the LVDT[2:0] bit in the power control register (PMU_CTL). LVD is enabled by LVDEN setting. The LVDF bit in the power supply status register (PMU_CS) indicates whether a low voltage event occurs. This event is connected to the 16th line of EXTI. The user can generate a corresponding interrupt by configuring the 16th line of EXTI. (LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16). The hysteresis voltage Vhyst value is 100 mV.

LVD application: When the MCU power supply is subject to external interference, such as a voltage drop, we can set the low voltage detection threshold (the threshold is greater than the PDR value) through LVD. Once it falls to the threshold, the LVD interrupt is turned on, which can be used in the interrupt function. Set operations such as soft reset to avoid other exceptions from the MCU.

Figure 2-5. LVD Threshold Waveform
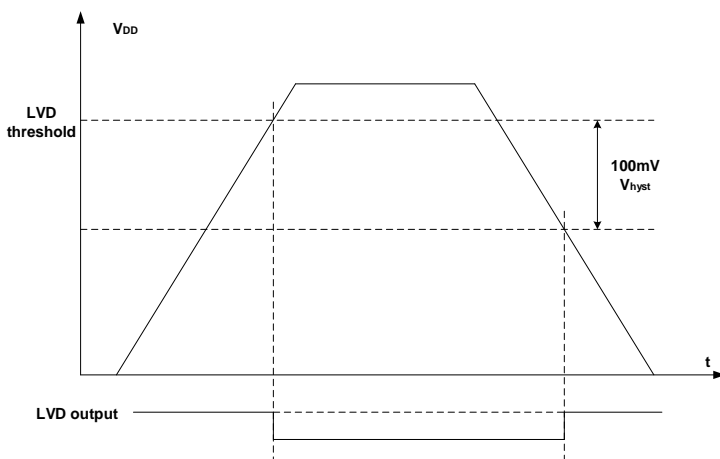
2.2.2. POR / PDR

The chip integrates a POR / PDR (power-on / power-down reset) circuit to detect V_{DD} / V_{DDA} and generate a power reset signal to reset the entire chip except the backup domain when the voltage is lower than a certain threshold. V_{POR} is the threshold voltage of power-on reset, and the typical value is about 2.4 V, and V_{PDR} is the threshold voltage of power-down reset, and the typical value is about 1.8 V. The value of the hysteresis voltage V_{hyst} is about 600 mV. It should be noted that the GD32F20x series reset pin only has the input function, and the low level generated by the system reset cannot be seen from the reset pin.

Figure 2-6. Power-on/power-down reset waveforms
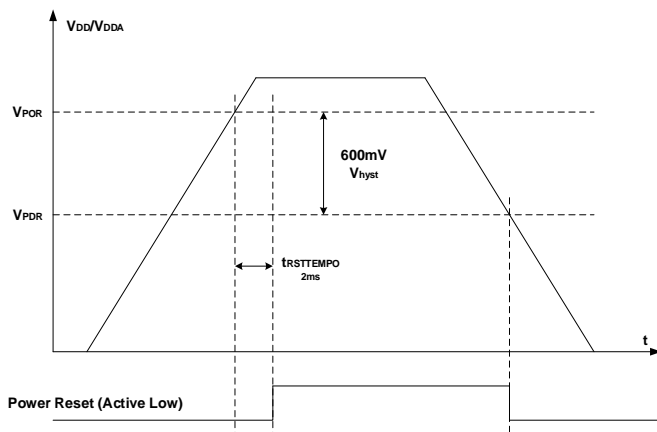
2.2.3. NRST Pin

For the MCU's NRST pin, to prevent accidental reset triggering, it is recommended to place a capacitor (typically 100 nF) on the NRST pin.

Figure 2-7. Recommend External Reset Circuit

GD32F20x

Note:

1. Internal pull-up resistance R_{PU} = 40 kΩ. You are advised to use an external pull-up resistance of 10 kΩ to ensure that voltage interference does not cause chip abnormalities

2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.

3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.

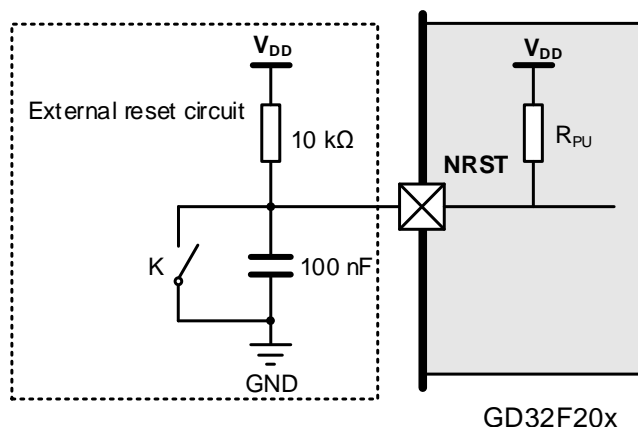4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

Due to the threshold voltage characteristics of the MOS transistor, during the power-up and power-down process of the chip, when VDD / VDDA < 0.7 V, the internal pull-down MOS transistor of the chip will not pull down the NRST pin. Therefore, during the power-up and power-down process, when VDD / VDDA ≈ 0.7 V, a small pulse occurs, which does not affect the normal operation of the chip, as shown by the red pulse in *__Figure 2-8. The illustration of the pulse of the NRST pin power-up/down MOS transistor__*.

Figure 2-8. The illustration of the pulse of the NRST pin power-up/down MOS transistor
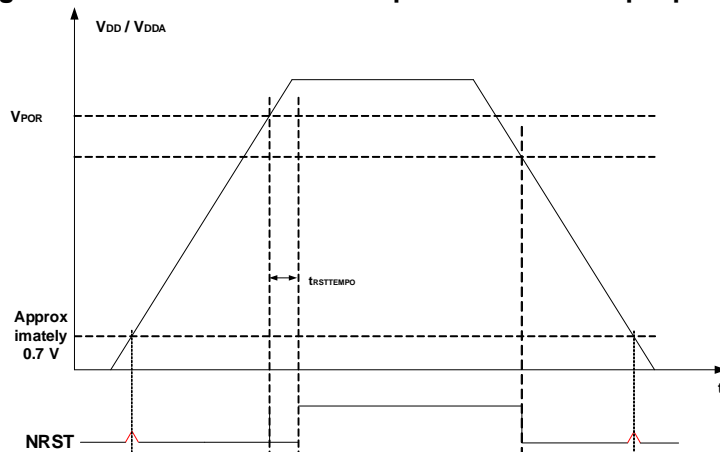
Due to the difference in charge and discharge speeds, the duration of the pulse on the falling edge is slightly longer than that on the rising edge, both of which are at the

millisecond level.

2.3.   Clock

GD32F20x series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

■   4-32 MHz external high-speed crystal oscillator (HXTAL).

■   Internal 8 MHz RC oscillator (IRC8M).

■   32.768 kHz external low-speed crystal oscillator (LXTAL).

■   Internal 40 kHz RC oscillator (IRC40K).

■   PLL clock source can be selected from HXTAL or IRC8M.

■   HXTAL clock monitor.

Figure 2-9. GD32F205xx Clock Tree
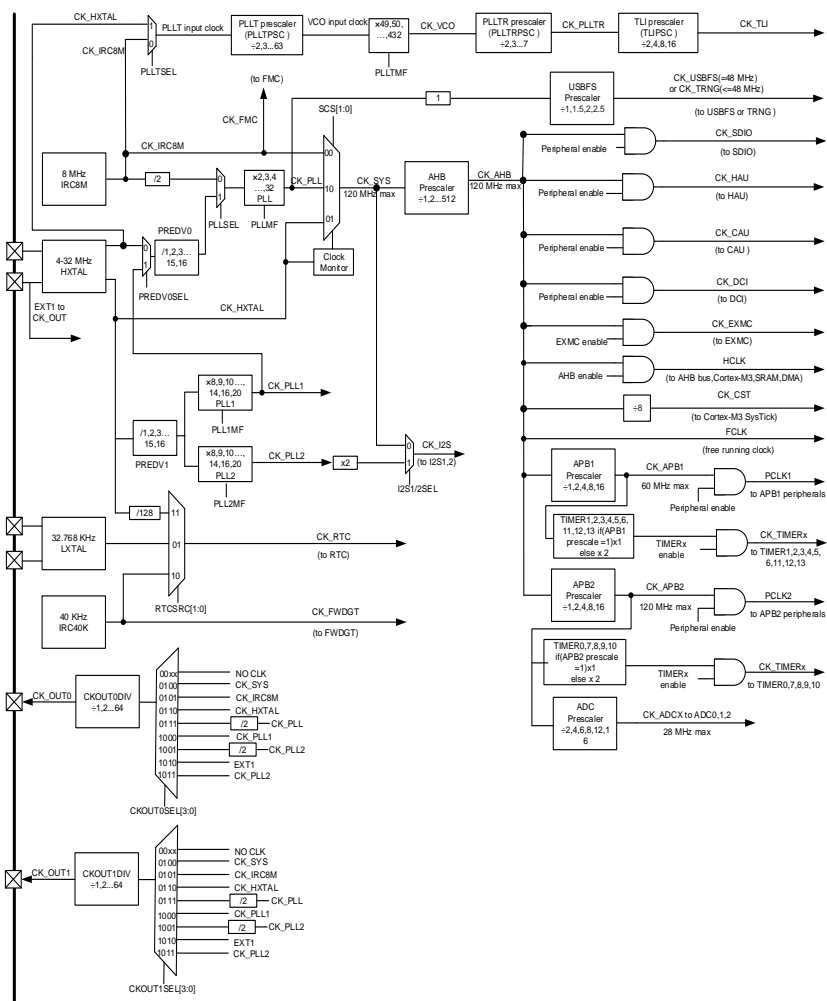
Figure 2-10. GD32F207xx Clock Tree
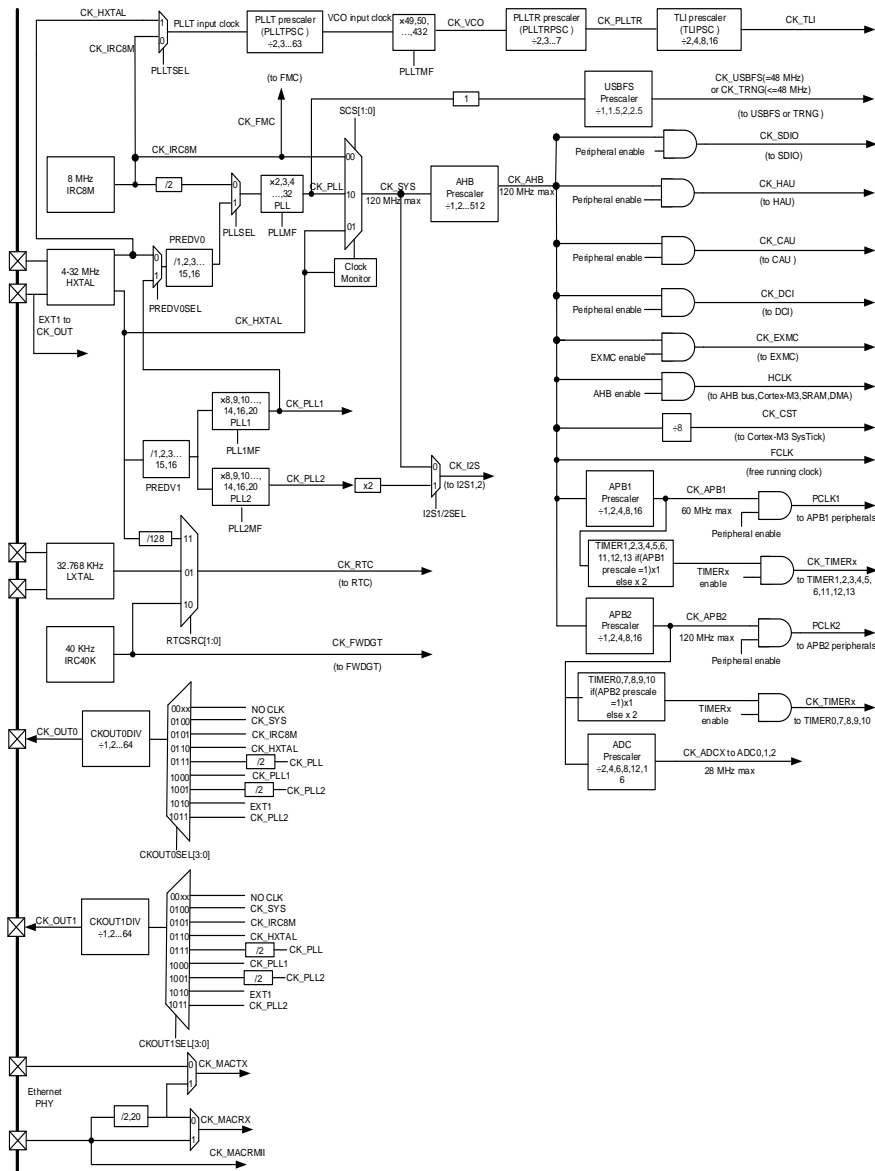
2.3.1. External high-speed crystal oscillator clock (HXTAL)

4-32MHz external high-speed crystal oscillator (passive crystal) can provide accurate main clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSC_IN, and OSC_OUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-11. HXTAL External Crystal Circuit
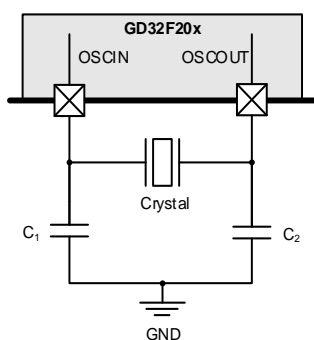
Figure 2-12. HXTAL External Clock Circuit
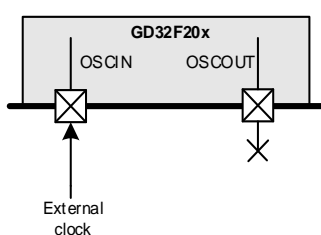
Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.

2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.

3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.

4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.

5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC8M.

6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}. If Bypass is not turned on, the amplitude requirements of the active crystal oscillator will be greatly reduced.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768KHz low-speed external crystal (passive crystal), which can provide

a low-power and high-precision clock source for RTC. The RTC module of the MCU is equivalent to a counter. The accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-13. LXTAL External Crystal Circuit
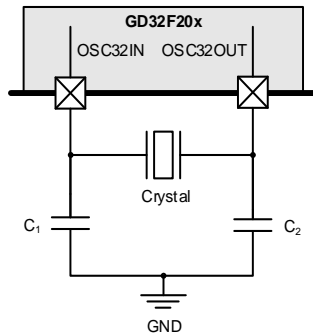
Figure 2-14. LXTAL External Clock Circuit
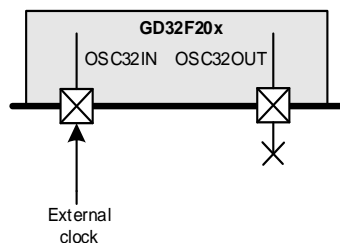
Note:

1. When using the bypass input, the signal is input from OSC32_IN, and OSC32_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. When the RTC selects IRC40K as the clock source and uses V_{BAT} for external independent power supply, if the MCU is powered off at this time, the RTC will stop counting. After re-powering, the RTC will continue to count up with the previous count value. If the application needs to use V_{BAT} to power the RTC, the RTC can still time normally, and the RTC must select LXTAL as the clock source.

2.3.3. Clock Output Capability (CKOUT)

For GD32F20x series MCU, you can select two clock signal outputs by configuring the CKOUT0SEL[3:0] bits of the clock register RCU_CFG0 and CKOUT1SEL[3:0] bits of the clock register RCU_CFG2, the corresponding GPIO pin PA8/PA9 needs to be configured as a multiplexing function to output the selected signal, as shown in the following:

Table 2-1. CKOUT0SEL[3:0] Control Bits

CKOUT0SEL[3:0]	Clock Source
00xx	NO CLK
0100	CK_SYS
0101	CK_IRC8M
0110	CK_HXTAL
0111	CK_PLL/2
1000	CK_PLL1
1001	CK_PLL2/2
1010	EXT1
1011	CK_PLL2

Table 2-2. CKOUT1SEL[3:0] Control Bits

CKOUT1SEL[3:0]	Clock Source
00xx	NO CLK
0100	CK_SYS
0101	CK_IRC8M
0110	CK_HXTAL
0111	CK_PLL/2
1000	CK_PLL1
1001	CK_PLL2/2
1010	EXT1
1011	CK_PLL2

2.3.4. HXTAL Clock Monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the control register RCU_CTL, HXTAL can enable the clock monitoring function. This function must be enabled after the HXTAL start-up delay has elapsed and disabled after the HXTAL has been stopped. Once the HXTAL fault is detected, the HXTAL will be automatically disabled, and the HXTAL clock blocking interrupt flag bit CKMIF in the interrupt register RCU_INT will be set to '1' to generate an HXTAL fault event. The interrupt caused by this fault is connected to the non-maskable interrupt NMI of the Cortex-M3.

Note: If HXTAL is selected as the system clock, PLL clock source or RTC clock source, HXTAL failure will cause the IRC8M to be selected as the system clock source and the PLL will be automatically disabled. The clock source of the RTC needs to be reconfigured.

2.4. Startup Configuration

The GD32F20x series provides three boot modes, which can be selected by the BOOT0 bit and the BOOT1 pin to determine the boot option. When designing the circuit, run the user program, the BOOT0 pin cannot be left floating, it is recommended to connect a 10kΩ resistor to GND. When running the System Memory to update the program, you need to connect the BOOT0 pin to high and the BOOT1 pin to low. After the update is completed, the user program can be run after the BOOT0 is connected to a low level; the SRAM execution program is mostly used in the debugging status.

The embedded Bootloader is stored in the system storage space for reprogramming the FLASH memory. In the GD32F20x device, Bootloader can interact with the outside world through USART0(PA9 and PA10), USART1 (PD5 and PD6) or USBFS(PA9, PA10, PA11 and PA12).

Table 2-3. BOOT mode

BOOT mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-15. Recommend BOOT Circuit Design
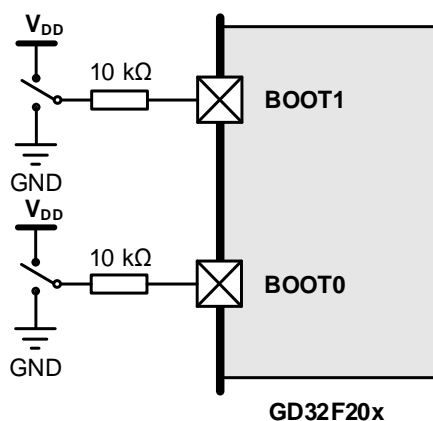
Note:
1. After the MCU is running, if the BOOT state is changed, it will take effect after the system is reset MCU.
2. Once the BOOT1 pin state is sampled, it can be released for other purposes.

2.5.   Typical Peripheral Modules

2.5.1.   GPIO Circuit

The largest package GPIO interface includes 9 groups of general-purpose input/output ports, each group of ports provides up to 16 general-purpose input/output pins, which are PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0~PH1 and PI0 ~ PI11(unique to LQFP176 package of GD32F207), each pin can be independently configured through registers, the basic structure of GPIO port is shown in *Figure 2-16. Basic structure of standard IO*.

Figure 2-16. Basic structure of standard IO
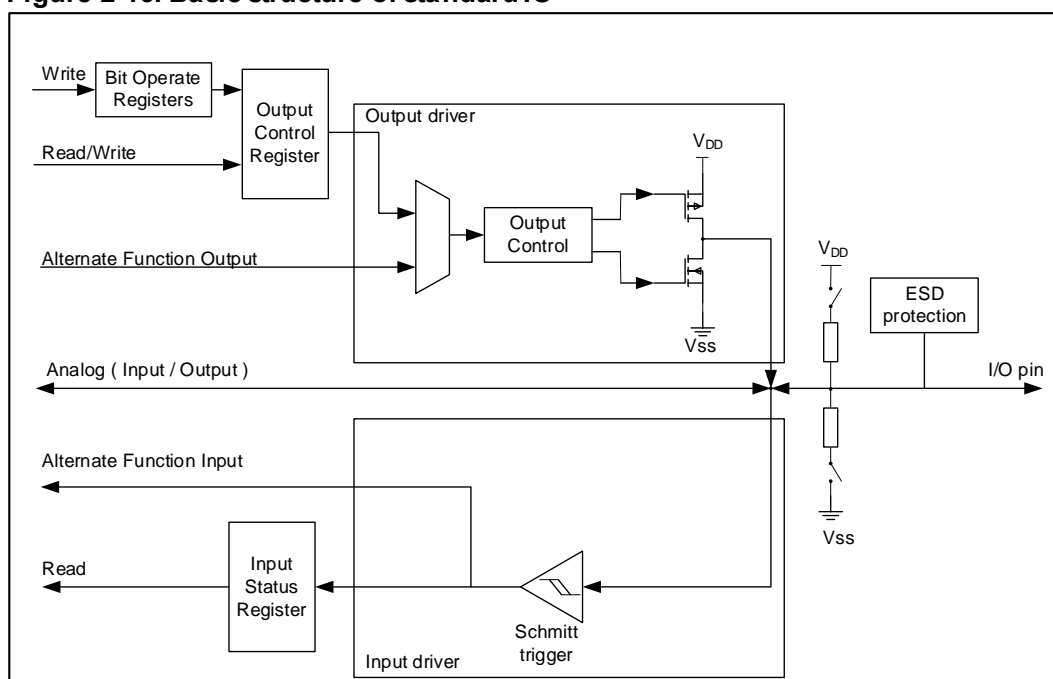
Note:

1. The IO port is divided into 5V tolerant and non-5V tolerant. When using, pay attention to distinguish the IO port withstand voltage. For the GD32F20x chip, except PA4 and PA5, the two pins are non-5V tolerant pins, and the other pins are 5V tolerant.

2. When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.

3. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).

4. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.

5. The four IO ports of PC13, PC14, PC15 and PI8 have weak drive capability and limited output current capability(about 3mA). When configured in output mode, their working

speed cannot exceed 2MHz(maximum load is 30pF).

6. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.

7. Non-5V tolerant IO, when the external voltage exceeds V_{DD}, a sink current may be generated.

2.5.2. ADC Circuit

The GD32F20x series integrates a 12-bit SAR ADC, which has up to 18 channels and can measure 16 external and 2 internal signal sources. The internal signal is the temperature sensor channel (ADC0_IN16) and the internal reference voltage input channel (ADC0_IN17). The temperature sensor reflects the change in temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a regulated voltage output (1.2V) to the ADC and is internally connected to ADC0_IN17.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin. It is recommended to place a small capacitor of 500pF.

Figure 2-17. ADC Acquisition Circuit Design
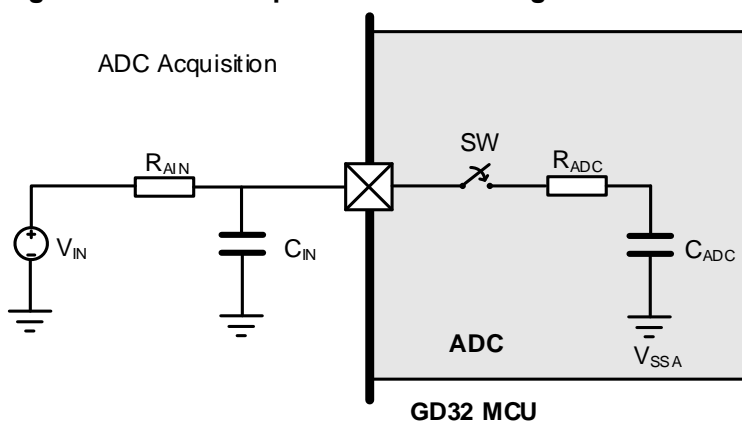
When f_{ADC} = 28MHz, the relationship between the input impedance and the sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, and select a larger value for the sampling period. When designing external circuits, try to reduce the input Impedance, if necessary, use the op amp to follow to reduce the input impedance.

Table 2-4. f_{ADC} =28 MHz Relationship between sampling period and external input impedance

T_S(cycles)	t_S(us)	R_{AINmax} (kΩ)
1.5	0.05	0.41

T$_s$(cycles)	t$_s$(us)	R$_{AINmax}$ (kΩ)
7.5	0.27	3.86
13.5	0.48	7.31
28.5	1.02	15.9
41.5	1.48	23.4
55.5	1.98	31.5
71.5	2.55	40.67
239.5	8.55	137.2

2.5.3.　USB Circuit

GD32F20x interconnected MCU has a built-in USB interface, which is a USBFS module. The USB protocol requires a clock accuracy of not less than 500ppm, and the internal clock may not be able to achieve such accuracy, so it is recommended to use an external crystal or an active crystal oscillator as the USB module clock source when using the USB function.

GD32F20x series USB can be designed as either a USB device or a USB hsot. When designed as USB device, PA9 is connected to VBUS, the DP line does not need an external 1.5K pull-up resistor. if PA9 is not connected to VBUS, if the VBUSIG control bit in the USBFS_GCCFG register has been configured, the USB_DP data line can not be connected with a 1.5K pull-up resistor. If this register is not configured, the USB_DP data line needs to be connected with a 1.5K pull-up resistor.

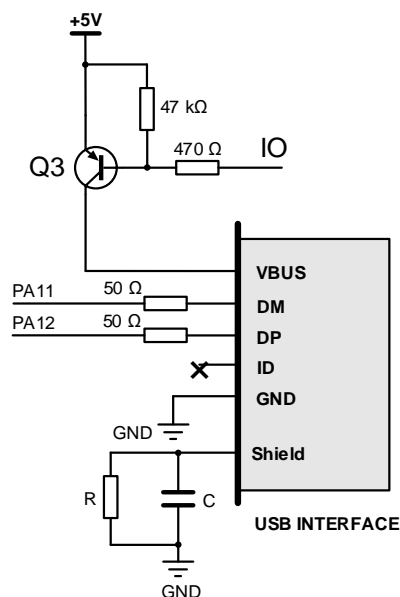**Figure 2-18. Recommend USB-Device Reference Circuit**
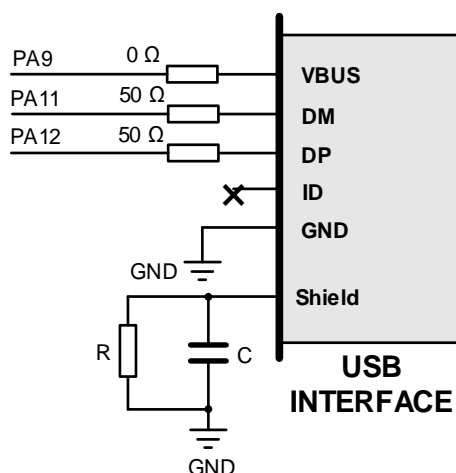
Recommendation: R = 1MΩ, C = 4700pF

Note: If the VBUSIG control bit in the USBFS_GCCFG register has been configured, the VBUS need not to be connected with PA9; if the VBUSIG control bit is not configured, PA9 need to be connected with the VBUS.

Figure 2-19. Recommend USB-Host Reference Circuit

Recommendation: R = 1MΩ, C = 4700pF

2.5.4. Standby mode wake-up circuit

The GD32F20x series supports three low-power modes, named sleep mode, deep-sleep mode and standby mode. The lowest power consumption is the standby mode, which requires the longest wake-up time. It can be woken up from standby mode by the rising edge of the WKUP pin. At this time, there is no need to configure the corresponding GPIO, just configure the WUPEN bit in the PMU_CS register. The WKUP pin reference circuit is designed as follows:

Figure 2-20. Recommend Standby external wake-up pin circuit design
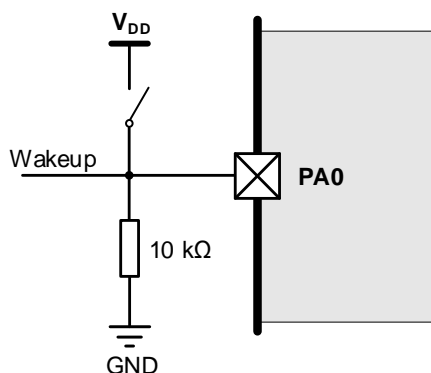
Note: In this mode, attention should be paid to the circuit design that If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.

2.6. Download and debug circuit

GD32F20x series cores support JTAG debug interface and SWD debug interface. The JTAG interface standard is a 20-pin interface, including 5 signal interfaces, and the SWD interface standard is a 5-pin interface, including 2 signal interfaces.

Note: After reset, the debug related ports are in input PU/PD mode, where:

PA15: JTDI is in pull-up mode.

PA14: JTCK/SWCLK in pull-down mode.

PA13: JTMS/SWDIO in pull-up mode.

PB4: NJTRST is in pull-up mode.

PB3: JTDO is floating mode.

Table 2-5. JTAG download debug interface assignment

Alternate function	GPIO port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-21. Recommend JTAG Wiring Reference Design
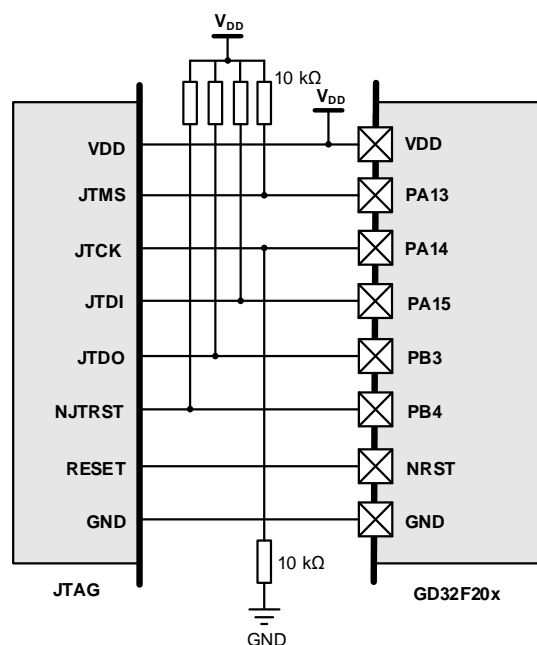
Table 2-6. SWD Download Debug Interface Assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-22. Recommend SWD Wiring Reference Design
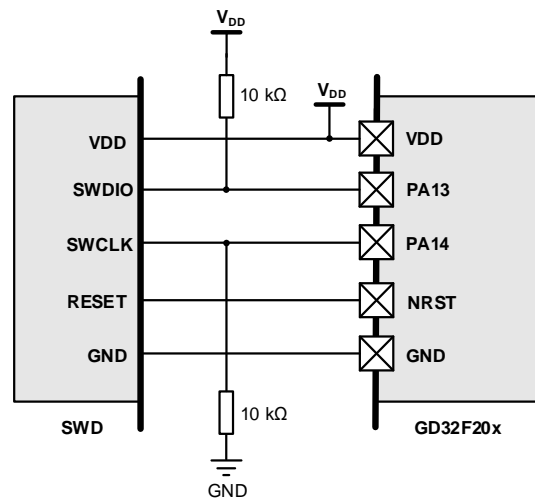
There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω~1kΩ resistor.

2.7. Reference Schematic Design

Figure 2-23. GD32F20x Recommend Reference Schematic Design

Peripheral

VDD

C5 50V/0.1uF C6 50V/0.1uF C7 50V/0.1uF C8 50V/0.1uF C9 50V/0.1uF C10 50V/0.1uF C11 50V/0.1uF C12 50V/0.1uF C13 50V/0.1uF C14 50V/0.1uF C15 50V/0.1uF C16 50V/4.7uF

GND

VDDA
C17 50V/1uF C18 50V/10nF
GND

VREFP
C19 50V/1uF C20 50V/10nF
GND

VBAT
C21 50V/0.1uF
GND

PC14 OSC32_IN
PC15 OSC32_OUT
DT-26-C06N-32.768KHz
Y2
C3 50V/10pF
C4 50V/10pF
GND

VDD
RP1 10K Ω
VDD
JP1
JNTRST
JTDI
JTMS/SWDIO
JTCK/SWDCLK
R1 10K RTCK
R2 10K JTDO
NRST
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
JTAG
GND
GND

C1 50V/20pF
HC-49S-G20SSA-25MHz
OSC_IN
GND
Y1
C2 50V/20pF
R3 1M Ω
OSC_OUT

JP2
3
2
1
BOOT0
GND R4 BOOT0
+3V3 10K Ω

JP3
3
2
1
BOOT1
GND R5 PB2 BOOT1
+3V3 10K Ω

RESET
+3V3
R6 10K Ω
K1
K-1102B
C22 50V/0.1uF
NRST
GND

3.   PCB Layout Design

In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1.   Power Supply Decoupling Capacitors

The GD32F20x series power supply has three power supply pins: VDD, VDDA, VREFP and VBAT. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, it is recommended to punch holes near the capacitor pad to connect with GND.

Figure 3-1. Recommend Power Pin Decoupling Layout Design
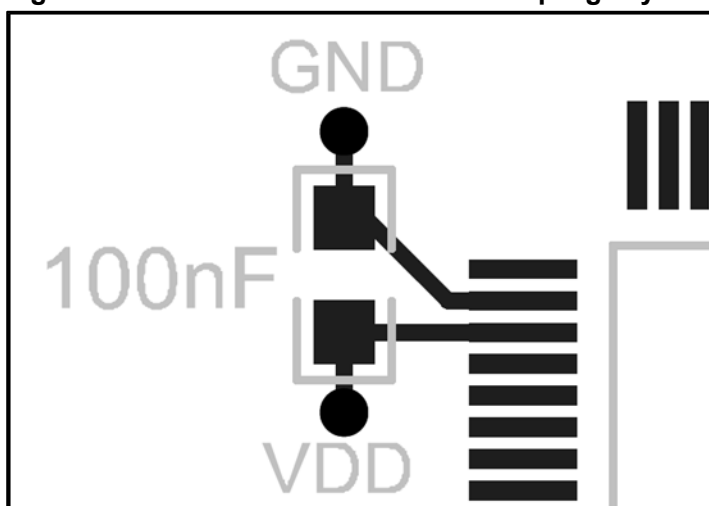
3.2.   Clock Circuit

GD32F20x series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

**Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)**
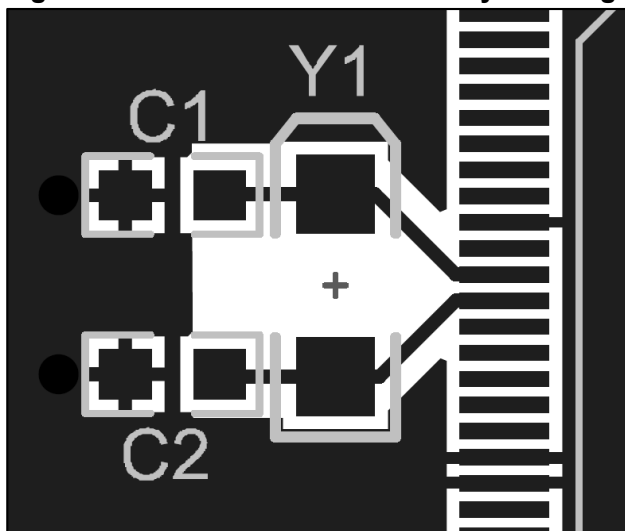
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3.   Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design
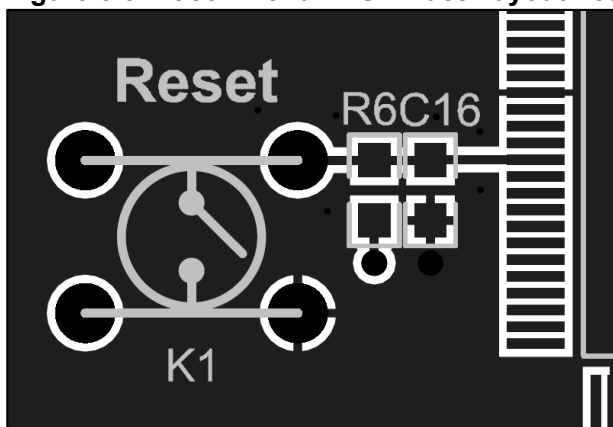
Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better

to wrap the NRST traces for better shielding effect.

3.4.   USB Circuit

The USB module has two differential signal lines, DM and DP. It is recommended that the PCB traces require a characteristic impedance of 90ohm. The differential traces should be run in strict accordance with the rule of equal length and equal distance, and the traces should be kept as short as possible. If the two differential lines are not equal in length , the short line can be compensated with a serpentine line at the terminal.

Due to impedance matching considerations, the series matching resistance is recommended to be about 50Ω. When the USB terminal interface is far away from the MCU, the series resistance value needs to be appropriately increased.

The USB differential trace reference is as follows:

Figure 3-4. Recommend USB Differential Trace Layout Design
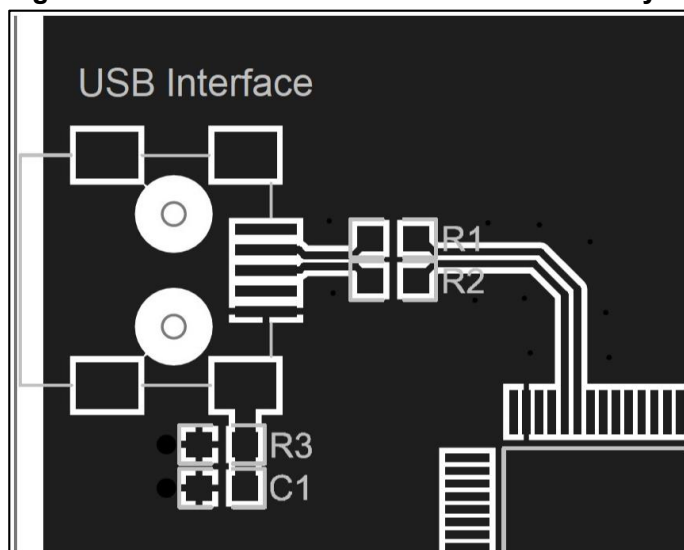
Recommendation: R1 = R2 = 50Ω, R3 = 1MΩ, C = 4700pF

Note:
1. Reasonable placement during layout to shorten the differential trace distance.
2. Draw differential lines first, try not to exceed two pairs of vias for a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring to ensure that the two lines are tightly coupled, avoiding 90°, arc or 45° wiring.
4. Devices such as resistance-capacitor, EMC connected to the differential traces, or test points should also be symmetrical.

4.   Package Description

GD32F20x series has a total of 4 package types, namely LQFP176, LQFP144, LQFP100 and LQFP64.

Table 4-1. Package Description

Ordering code	Package
GD32F20xRxT6	LQFP64(10x10, 0.5 pitch)
GD32F20xVxT6	LQFP100(14x14, 0.5 pitch)
GD32F20xZxT6	LQFP144(20x20, 0.5 pitch)
GD32F207lxT6	LQFP176(24x24, 0.5 pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.7, 2023
1.1	Update section 2.1.3 to provide all packageing power supply design drawings, explaining the connection of revelant pins within the chip.	Jun.21, 2023
1.2	Refine the content related to power supply detection and reset, and add Section 2.2.	Dec.15, 2024

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