GigaDevice Semiconductor Inc.

GD32A503 Hardware Development Guide

Application Notes
AN110

Revision 1.2

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1. Foreword

This document is specially provided for developers of the general-purpose 32-bit GD32A503 MCU based on the Arm® Cortex®-M33 architecture. It provides a general introduction to the hardware development of GD32A503, such as the settings of power supply, reset, clock, boot mode, and download debug. The purpose of the Application Notes is to enable developers to quickly get started with GD32A503, quickly develop and use the product hardware, and save time for studying the manual, thus accelerating the product development progress.

The Application Notes is described in seven parts:

1. Power supply: It mainly introduces the design of the power management, power supply, and reset functions of GD32A503.
2. Clock: It mainly introduces the design of the high and low speed clock functions of GD32A503.
3. Boot configuration: It mainly introduces the BOOT configuration and design of GD32A503.
4. Typical peripheral module: It mainly introduces the hardware design of the main functional modules of GD32A503.
5. Download debug circuit: It mainly introduces the typical download debug circuits recommended for GD32A503.
6. Reference circuit and PCB layout design: It mainly introduces the precautions for hardware circuit design and PCB layout design of GD32A503.
7. Package description: It mainly introduces the types and names of packages included in GD32A503.

This document also introduces the minimum system hardware resources used in GD32A503 application development.

Table 1-1. Applicable product

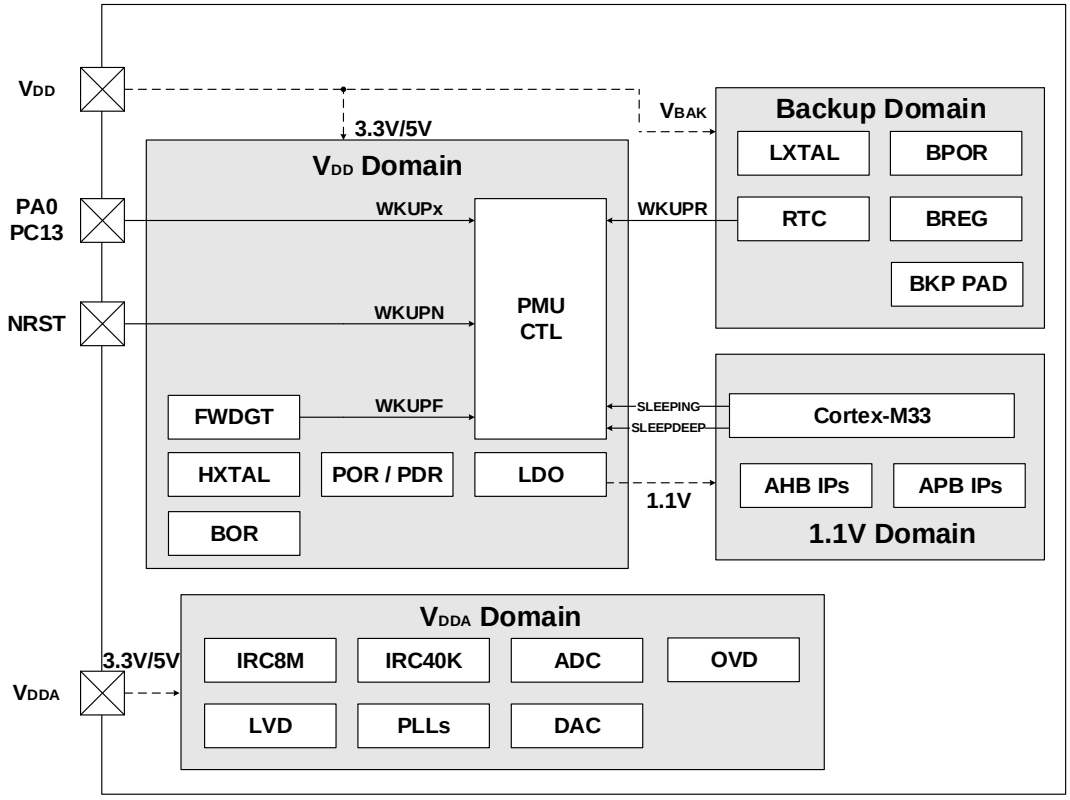
Type	Part Numbers
MCU	GD32A503xx

2. Hardware design

2.1. Power supply

The operating voltage of V_{DD}/V_{DDA} of GD32A503 ranges from 2.7 V to 5.5 V. As shown in *Figure 2-1. Overview of power domains of GD32A503*, GD32A503 device has three power domains, including V_{DD}/V_{DDA} domain, 1.1 V domain, and backup domain. V_{DD}/V_{DDA} domain and backup domain are powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to provide 1.1 V power for 1.1 V domain.

Figure 2-1. Overview of power domains of GD32A503



LVD: Low Voltage Detector
LDO: Voltage Regulator
OVD:Over Voltage Detector
POR: Power On Reset
PDR: Power Down Reset
BREG: Backup registers
BPOR: V_{BAK} Power On Reset
BOR: Brownout Reset

2.1.1. Backup domain

The supply voltage of backup domain ranges from 2.7 V to 5.5 V. To ensure normal operation of the backup register and RTC, the V_{DD} power supply cannot be turned off; otherwise, all data of backup domain and the register will be reset.

Note: Functions that can work normally after power failure such as RTC and backup domain are unavailable for GD32A503 MCU without VBAT pin.

2.1.2. V_{DD}/V_{DDA} power domain

V_{DD}/V_{DDA} power domain includes two parts: V_{DD} domain and V_{DDA} domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between them must not exceed 300 mV (V_{DDA} and V_{DD} inside the chip are connected through back-to-back diodes). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and V_{SSA} can be connected to V_{SS} through a specific circuit (single-point grounding through 0 Ω resistors or magnetic beads, etc.).

To improve the conversion accuracy of ADC, an independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. The large package provides VREFP pins (2.7 V ≤ V_{REFP} ≤ V_{DDA}, V_{REFN} = V_{SSA}) to supply exclusive power to ADC.

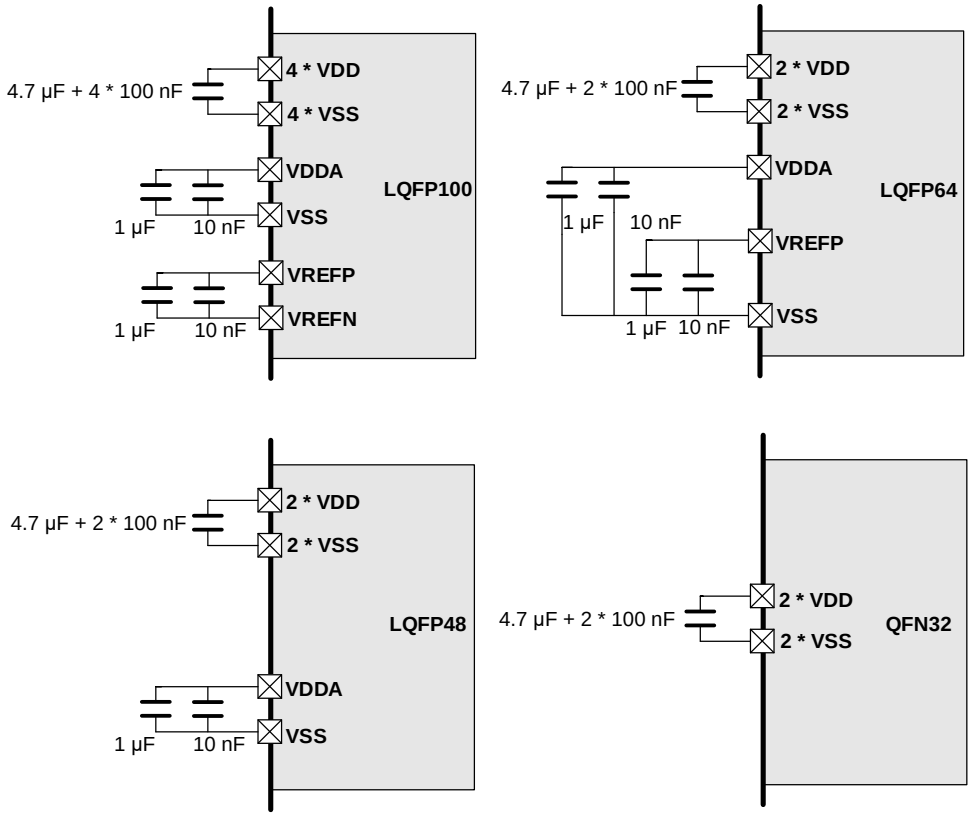
- Packaged chips with 64 pins or more contain VREFP. The VREFP can be powered by an external reference power supply or be directly connected to VDDA, while VREFN must be connected to VSSA.
- Without VREFP and VREFN, packaged chips with 48 pins and 32 pins are directly connected to VDDA internally, and all analog modules are powered by VDDA (including ADC/DAC).

2.1.3. Power supply design

The system requires a stable power supply, and pay attention to the following precautions during development and use:

- The VDD pins must be connected to external capacitors (100 nF ceramic capacitor + not less than 4.7 uF tantalum capacitor; a not less than 4.7 uF capacitor should be connected to GND via at least one VDD pin, and the other VDD pins are connected to 100 nF capacitors).
- The VDDA pins must be connected to external capacitors (10 nF + 1 uF ceramic capacitors are recommended).
- VREFP pin is powered externally, and a 10 nF + 1 μF ceramic capacitor should be connected to ground near the VREFP pin.

Figure 2-2. Power supply design recommended for GD32A503



Note:

1. All decoupling capacitors need to be as close as possible to the pins on the PCB board.
2. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
3. LQFP100: VSS and VSSA are connected internally.
4. LQFP64: VSSA、VREFN、VSS are connected internally.
5. LQFP48: VREFP and VDDA are connected internally, VSS、VSSA、VREFN are connected internally.
6. QFN32: VDD、VDDA、VREFP are connected internally, VSS、VSSA、VREFN are connected internally.

2.2. Reset and power management

In this section, the default is that the VDD and VDDA pins remain connected and are powered by the same power source. The reset control of GD32A503 includes three types: power reset, system reset, and backup domain reset. The power reset is a cold reset, and all systems except the backup domain are reset when the power is turned on. Except for the SW-DP controller and backup domain, the processor core and peripheral IP address will be reset together with the system. During the power and system reset process, NRST will maintain a low level until the reset is over. In case of MCU execution failure, you can monitor the waveform of NRST pin through an oscilloscope to determine whether the chip reset event

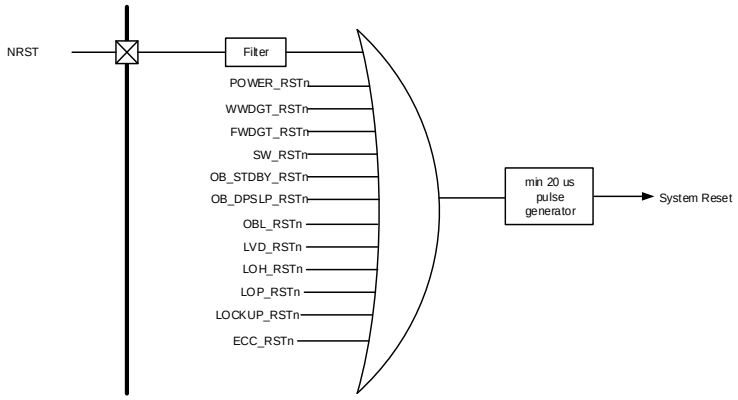
occurs continuously. The reset source of MCU can be determined by querying the register RCU_RSTSCK (0x40021024). During use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that when the watchdog reset event or other reset events occur again, the RCU_RSTSCK register can accurately reflect the reset source.

Figure 2-3. RCU_RSTSCK register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LP RSTF	WWDGT RSTF	FWDGT RSTF	SW RSTF	POR RSTF	EP RSTF	OBL RSTF	RSTFC	V11 RSTF	LOP RSTF	LOH RSTF	ECC RSTF	LVD RSTF	LOCKUP RSTF	BOR RSTF	Reserved
r	r	r	r	r	r	r	rw	r	r	r	r	r	r	r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	LOPRSTEN	LOHRSTEN	ECC RSTEN	LVD RSTEN	LOCKUP RSTEN	Reserved								IRC40K STB	IRC40K EN
	rw	rw	rw	rw	rw									r	rw

MCU has integrated POR/PDR circuit. In the design of the external reset circuit, a capacitor (typically 100 nF) must be installed at the NRST pins to make sure that a low pulse delay of at least 20 us can be generated when the NRST pins are powered on, to complete an effective power-on reset process.

Figure 2-4. System reset circuit



2.2.1. LVD

LVD is used to detect whether the supply voltage of V_{DD}/V_{DDA} is lower than the low voltage detection threshold (2.9 V to 4.6 V), which is configured by the LVDT[2:0] bit in the power control register (PMU_CTL). LVD is enabled by setting LVDEN. The LVDF bit in the power control and status register (PMU_CS) indicates whether the voltage event occurs when V_{DD}/V_{DDA} is higher or lower than the LVD threshold. The event is connected to line 16 of EXTI, and the user can generate interrupt by configuring line 16 of EXTI. ***Figure 2-5. LVD threshold waveform*** shows the relation between the supply voltage of V_{DD}/V_{DDA} and the output signal of LVD. (The interrupt signal of LVD depends on the rising or falling edge configuration of line 16 of EXTI). The hysteresis voltage V_{hyst} is 100 mV.

LVD application scenario: When the power supply of MCU is subject to external interference, such as voltage drop, we can set the low voltage detection threshold (greater than the PDR value) through LVD. Once the voltage drops to the threshold, LVD interrupt is enabled, and some protective measures can be taken in the interrupt function to avoid other exceptions in

MCU.

OVD is used to detect whether the supply voltage of V_{DD}/V_{DDA} is higher than the voltage detection threshold, which is configured by the OVDT bit in the power control register (PMU_CTL). OVD is enabled by setting OVDEN. The OVDF bit in the power control and status register (PMU_CS) indicates whether the overvoltage event occurs. The event is connected to line 24 of EXTI, and the user can generate interrupt by configuring line 24 of EXTI. ***Figure 2-6. OVD threshold waveform*** shows the relation between the supply voltage of V_{DD}/V_{DDA} and the output signal of OVD. (The interrupt signal of OVD depends on the rising or falling edge configuration of line 24 of EXTI). The figure also shows the relation between the supply voltage and the OVD signal. The hysteresis voltage V_{hyst} is 25 mV.

Figure 2-5. LVD threshold waveform

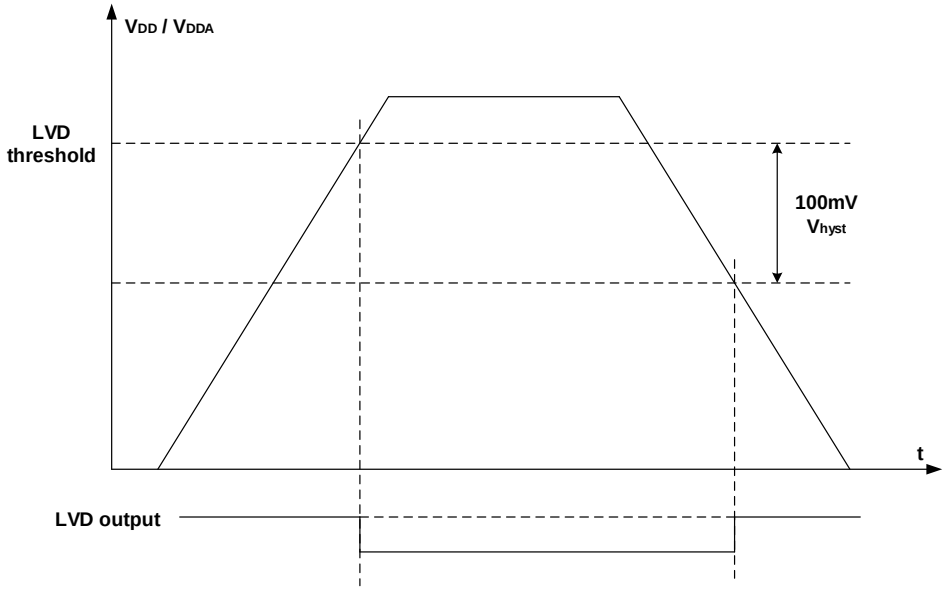
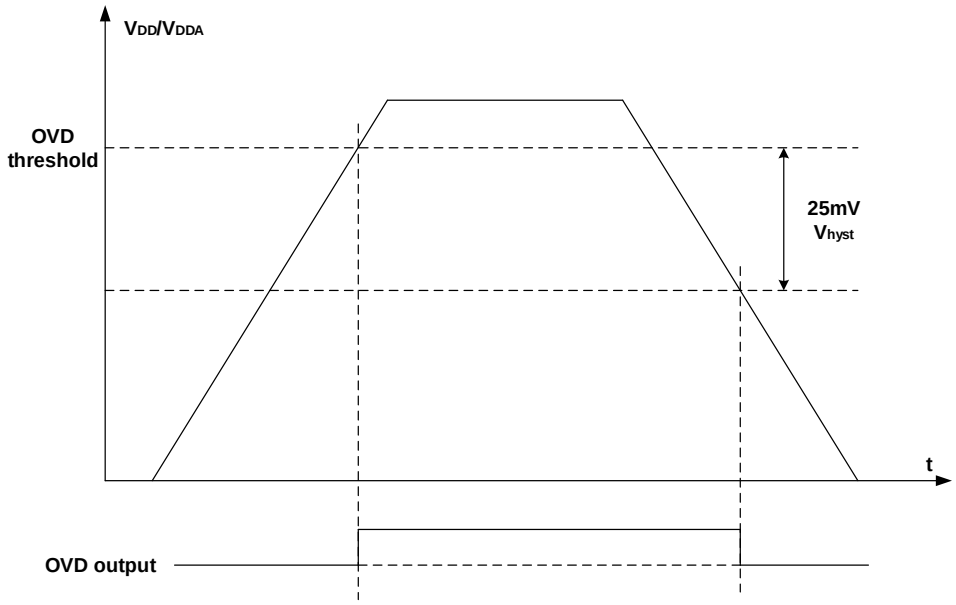


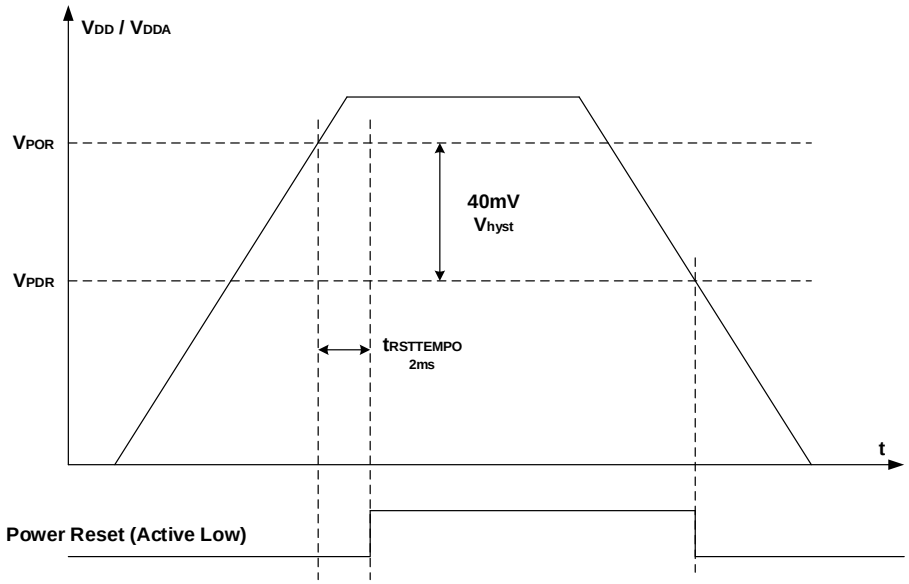
Figure 2-6. OVD threshold waveform



2.2.2. POR/PDR

The chip integrates the POR/PDR (power-on/power-down reset) circuit in the chip is used to detect V_{DD}/V_{DDA} and generates a power reset signal to reset the entire chip except the backup domain when the voltage is lower than a specific threshold. V_{POR} represents the threshold voltage of POR, and V_{PDR} represents the threshold voltage of PDR. The hysteresis voltage V_{hyst} is about 40 mV.

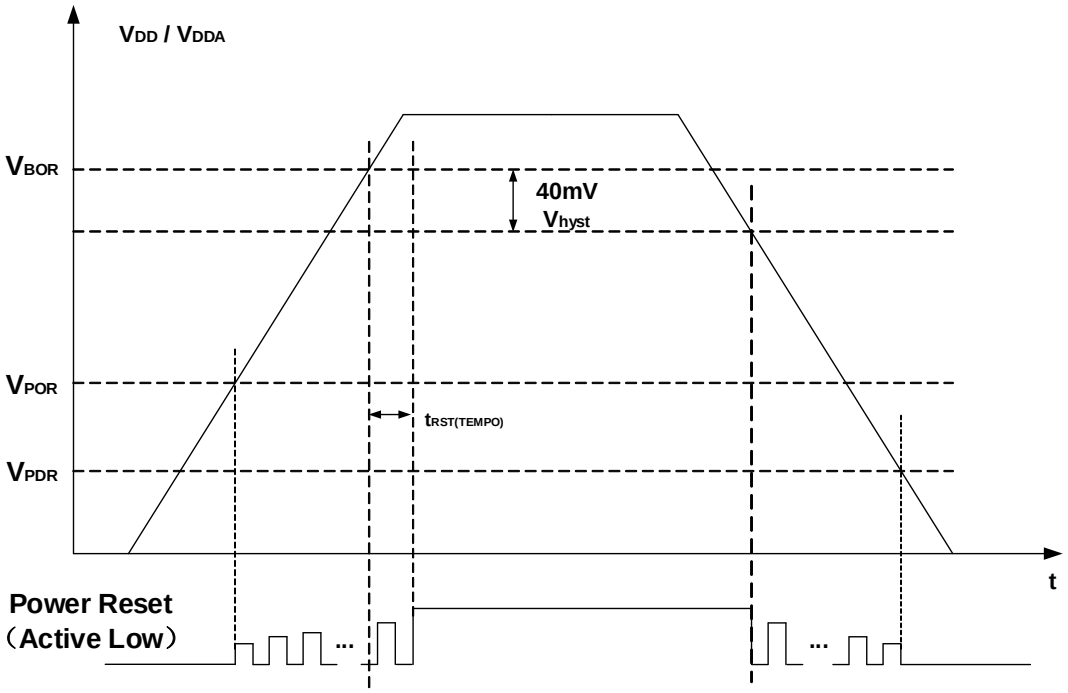
Figure 2-7. POR/PDR waveform



2.2.3. BOR

The MCU of GD32A503 also integrates the BOR circuit. The BOR (brown-out reset) circuit detects the V_{DD}/V_{DDA} and generates a power reset signal to reset the entire chip except the backup domain when the voltage is lower than the threshold defined by the option byte BOR_TH. ***Figure 2-8. BOR threshold waveform***shows the relation between the power supply voltage and the BOR reset signal. V_{BOR} represents the voltage threshold of the BOR, which is defined in the option byte BOR_TH. The hysteresis voltage V_{hyst} is about 40 mV.

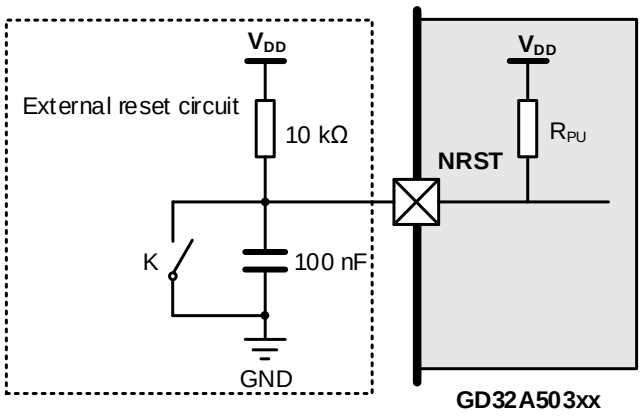
Figure 2-8. BOR threshold waveform



2.2.4. NRST Pin

For the MCU's NRST pin, to prevent false reset triggering, it is recommended to place a capacitor (typical value of 100nF) on the NRST pin.

Figure 2-9. Recommended external reset circuit



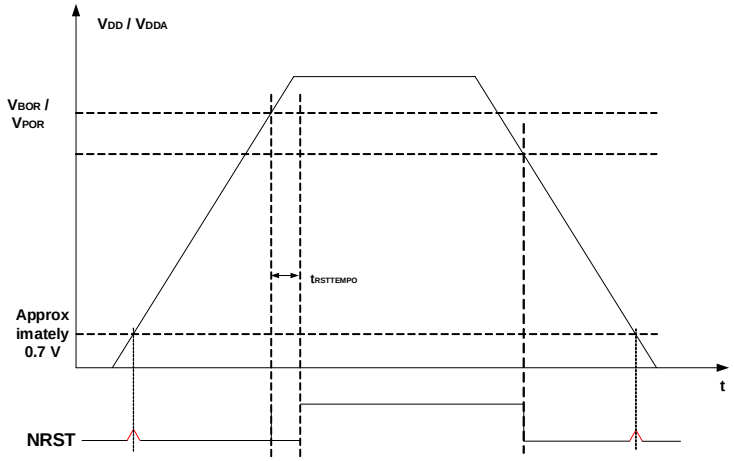
Notes:

1. It is recommended to connect 40 kΩ internal pull-up resistor R_{PU} to 10 kΩ external pull-up resistor to avoid abnormal operation of the chip due to voltage interference.
2. Considering the impact of static electricity, an ESD protection diode can be installed at the NRST pins.
3. Although there is a hardware POR circuit inside MCU, it is recommended to add an external NRST reset resistance-capacitance circuit.
4. If MCU starts abnormally (due to voltage fluctuation), the capacitance of NRST to ground

can be appropriately increased to extend the MCU reset completion time and avoid the abnormal power-on sequence zone.

Due to the threshold voltage characteristics of the MOS transistor, during the power-up and power-down process of the chip, when VDD / VDDA < 0.7 V, the internal pull-down MOS transistor of the chip will not pull down the NRST pin. Therefore, during the power-up and power-down process, when VDD / VDDA ≈ 0.7 V, a small pulse occurs, which does not affect the normal operation of the chip, as shown by the red pulse in ***Figure 2-10. The illustration of the pulse of the NRST pin power-up/down MOS transistor***.

Figure 2-10. The illustration of the pulse of the NRST pin power-up/down MOS transistor



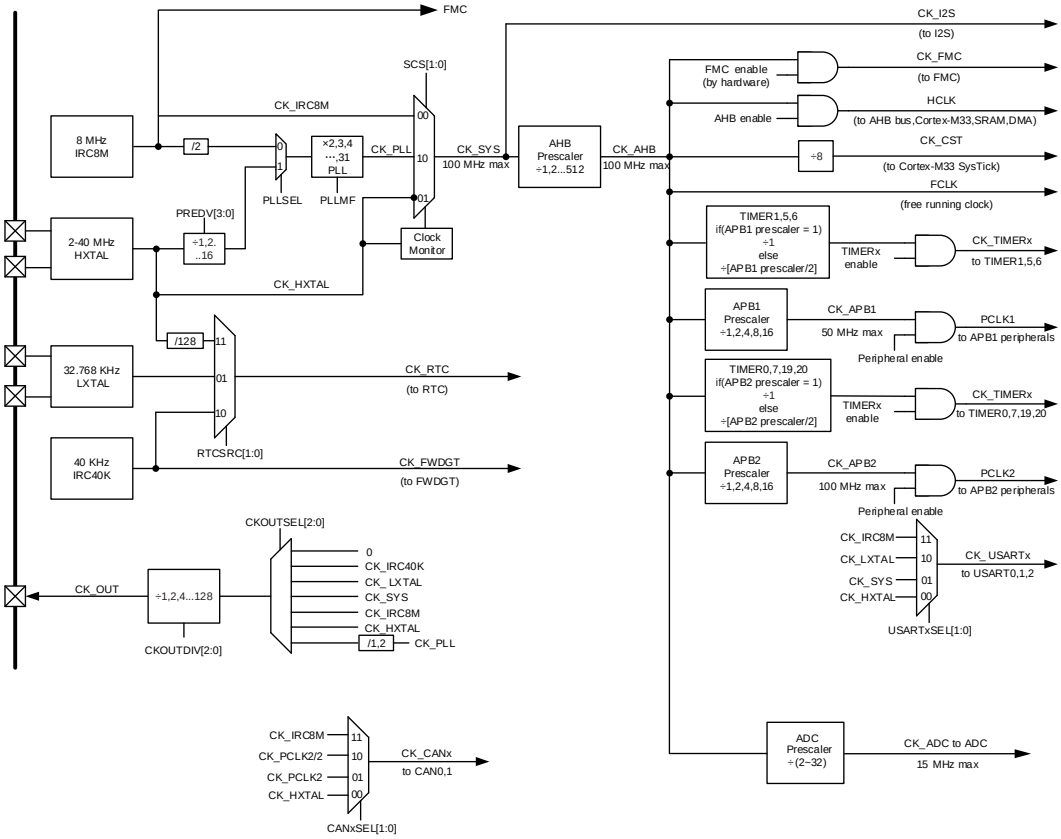
Due to the difference in charge and discharge speeds, the duration of the pulse on the falling edge is slightly longer than that on the rising edge, both of which are at the millisecond level.

2.3. Clock

GD32A503 contains a complete built-in clock system, and the appropriate clock sources can be selected according to different application scenarios. The main features of the clock are as follows:

- 2-40 MHz external high-speed crystal oscillator (HXTAL)
- 8 MHz internal high-speed RC oscillator (IRC8M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- 40 kHz internal low-speed RC oscillator (IRC40K)
- Optional PLL clock source: HXTAL or IRC8M
- HXTAL clock monitoring
- LXTAL clock monitoring

Figure 2-11. Clock tree



2.3.1. External high-speed crystal oscillator clock (HXTAL)

2-40 MHz external high-speed crystal oscillator (passive crystal) can provide an accurate master clock for the system. The crystal of specific frequency must be installed close to the HXTAL pins, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the selected oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator). In the bypass input mode, the signal is connected to OSCIN, OSCOUT remains suspended, and the Bypass function of HXTAL needs to be enabled on the software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-12. HXTAL external crystal circuit

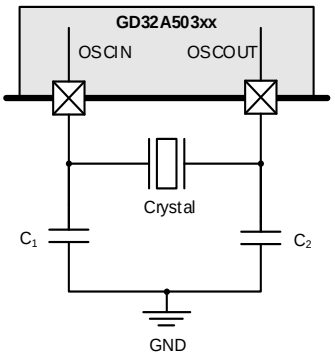
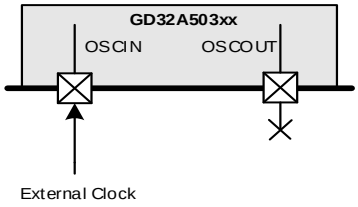


Figure 2-13. HXTAL external clock circuit



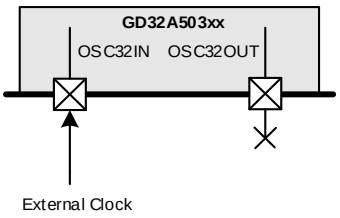
Notes:

1. When the bypass input mode is used, the signal is input from OSCIN, and OSCOUT remains suspended;
2. For the size of the external matching capacitor, refer to the formula: $C_1 = C_2 = 2 * (C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, typically 10 pF. When an external high-speed crystal is recommended, try to choose a crystal with a load capacitance of about 20 pF, so that the external matching capacitors C_1 and C_2 can be 20 pF, and the crystal should be installed as close as possible to the crystal oscillator pins during PCB layout.
3. C_S is the parasitic capacitance on the PCB layout and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU and works abnormally, the capacitance of the external matching capacitor can be appropriately reduced;
4. When an external high-speed crystal is used, it is recommended to connect 1 MΩ resistors in parallel at both ends of the crystal to make the crystal easier to start oscillation.
5. Accuracy: external active crystal oscillator > external passive crystal > IRC8M;
6. Normally, Bypass is enabled when an active crystal oscillator is used. At this time, the high level should not be lower than 0.7 V_{DD}, and the low level should not be higher than 0.3 V_{DD}. If Bypass is not enabled, the amplitude requirements for the active crystal oscillator will be greatly reduced.
7. The wiring between the resonator and the MCU clock pins may lead to inconsistent lengths of cables connected to the OSCOUT and OSCIN pins due to the space limit of the PCB layout. As a result, the stray capacitance introduced by the two PCB cables will be inconsistent, resulting in unequal load capacitance values on both sides of the resonator. A difference is required to match the actual PCB. In this case, it is recommended to contact the resonator manufacturer to measure the actual value.
8. When a passive crystal oscillator is used, the HXTAL frequency range needs to be selected through the HXTALSCAL bit in the control register (RCU_CTL). If the HXTAL frequency is higher than 8 MHz, the HXTALSCAL bit must be set to 1.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768 KHz external low-speed crystal, which can provide a low-power consumption and high-precision clock source for RTC. In this series, only the active crystal oscillator can be used, and the bypass mode needs to be enabled (the LXTALBPS bit is 1).

Figure 2-14. LXTAL external clock circuit



Note: When the bypass input mode is used, the signal is input from OSC32IN, and OSC32OUT remains suspended.

2.3.3. Clock output capability (CKOUT)

GD32A503 MCU can output clocks from 32 kHz to 100 MHz. Different clock signals can be selected by setting the CK_OUT clock source selection bit field CKOUTSEL in the clock configuration register RCU_CFG0. GPIO pins (PC13, PC2, and PA1) should be configured in the alternate function I/O (AFIO) mode to output the selected clock signal.

Table 2-1. CKOUTSEL[2:0] control bit

Clock source selection bit	Clock source
000	No clock
001	Reserved
010	CK_IRC40K
011	CK_LXTAL
100	CK_SYS
101	CK_IRC8M
110	CK_HXTAL
111	CK_PLL or CK_PLL/2

2.3.4. HXTAL clock monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the clock control register RCU_CTL, and the HXTAL can enable the clock monitoring function. The function must be enabled after the HXTAL boot delay is over and disabled after HXTAL stops. Once a HXTAL fault is detected, the generation of the HXTAL loss reset will be determined by the LOHRSTEN bit in the register RCU_RSTSCK, Or the NMI interrupt can be determined by the CKMNMIIE bit of the register SYSCFG_CFG3.

If CKMNMIIE and LOHRSTEN are 0, the HXTAL clock blocking flag bit CKMIF in the clock interrupt register RCU_INT will be set to '1' to generate an HXTAL fault event. The HXTAL will be automatically disabled. This fault interrupt is connected to the non-maskable interrupt (NMI) of Arm® Cortex®-M33. If HXTAL is selected as the clock source for CK_SYS or PLL, the HXTAL fault will force the CK_SYS source to be IRC8M, and PLL will be automatically disabled.

If CKMNMIIE is 0 and LOHRSTEN is 1, the HXTAL loss reset will be generated.

2.3.5. LXTAL clock monitor (LCKM)

You can write LCKMEN in the control register (RCU_CTL) through the software to activate the clock monitor on the LXTAL. LCKMEN cannot be enabled until LXTAL and IRC40K are enabled and ready.

When LCKMEN is enabled, the 4-bit + 1 counter will work in the IRC40K domain. If the LXTAL clock has a 0/1 error or slows down by about 20 KHz, the counter will overflow. The LXTAL clock fault will be detected.

2.4. Boot configuration

GD32A503 provides three boot modes, which can be selected through the BOOT0 and BOOT1 pins to determine the boot options. The level state of the two pins will be latched at the rising edge of the fourth CK_SYS (system clock) after resetting.

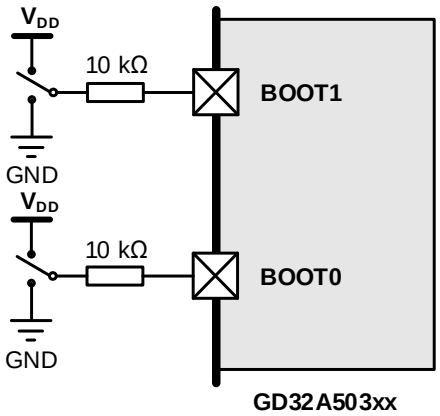
During the circuit design, when the user program runs, the BOOT0 pin cannot be suspended, and it is recommended to connect it to GND through a 10 kΩ resistor. To run the System Memory to update the program, it is required to connect the BOOT0 pin to a high voltage and the BOOT1 pin to a low voltage. After the update is completed, it is necessary to connect the BOOT0 to a low voltage and power on before the user program can be run. If it is required to boot from SRAM, both the BOOT0 and BOOT1 pins need to be connected to a high voltage.

The embedded Bootloader is stored in the system memory space and is used to reprogram the FLASH memory. Bootloader can interact with the external devices through USART0 (PA10 and PA11), LIN (PA3 and PA4) or CAN0 (PB13 and PB14).

Table 2-2. BOOT mode

BOOT mode	BOOT1	BOOT0
Main FLASH memory	x	0
System memory	0	1
On-chip SRAM	1	1

Figure 2-15. Recommended BOOT circuit design



Notes:

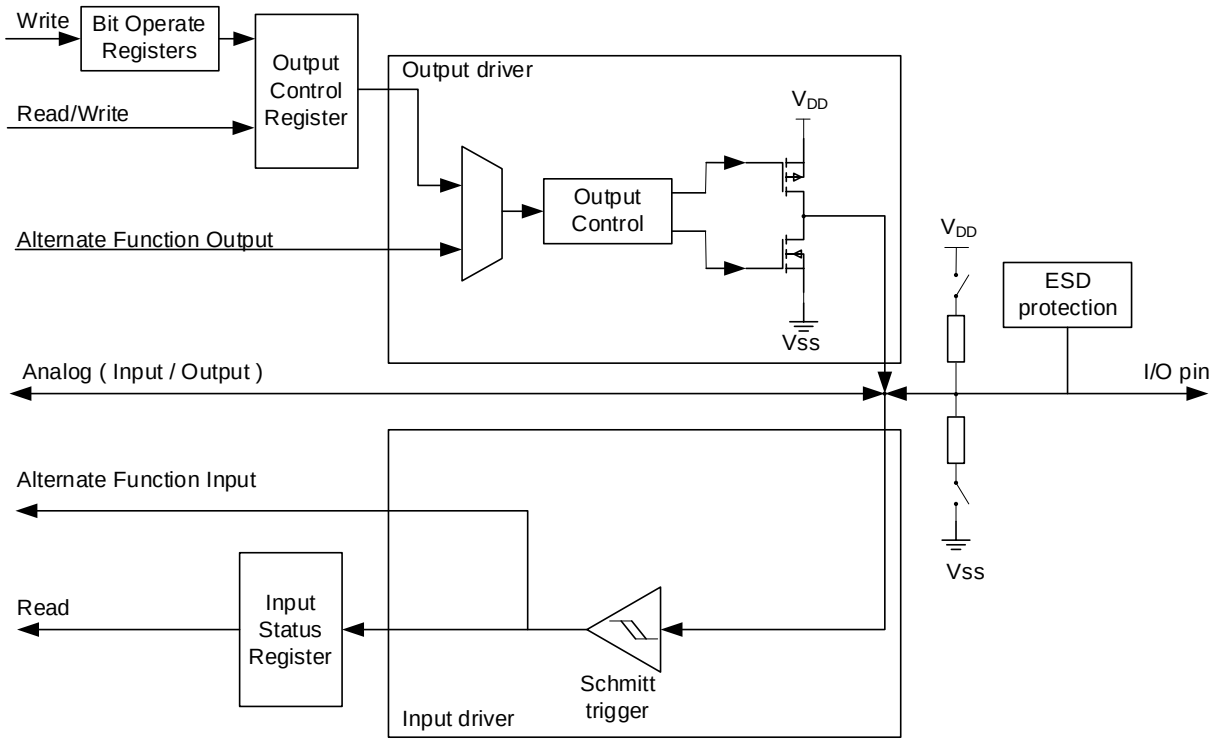
1. After MCU runs, if the BOOT state is changed, it will take effect only after the system is reset.
2. Once the BOOT pin states are sampled, they can be released for other purposes.

2.5. Typical peripheral modules

2.5.1. GPIO circuit

GD32A503 supports up to 88 general-purpose I/O (GPIO) pins, including PA0 - PA15, PB0 - PB15, PC0 - PC15, PD0 - PD15, PE0 - PE15, and PF0 - PF7. Each pin can be configured separately through the register. The basic structure of the GPIO port is shown in the figure below:

Figure 2-16. Basic structure of standard IO



Notes:

1. After the IO ports are powered on and reset, the default mode is floating input, and the level characteristics are uncertain. To achieve consistent power consumptions, it is recommended that all IO ports be configured to analog input and then modified to the corresponding mode according to application requirements (ports that are not led out from the inside of the chip also need to be configured);
2. To improve the EMC performance, unused IO port pins are recommended to be pulled up or down by the hardware;
3. For pins with the same label in multiple groups, only one IO port can be configured as

an external interrupt. For example: PA0, PB0, and PC0 only support one of the three IO ports to generate an external interrupt, and the three pins cannot be in the external interrupt mode at the same time.

2.5.2. ADC circuit

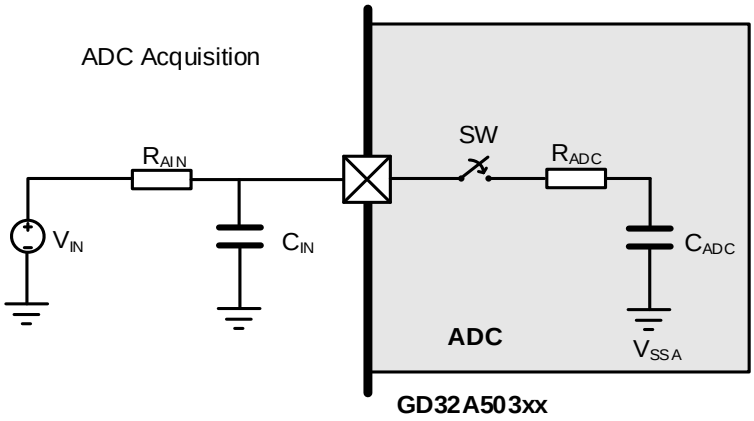
GD32A503 integrates a 12-bit SAR ADC, which has up to 18 channels and can measure 16 external signal sources and 2 internal signal sources. The internal signals are the temperature sensor channel (ADC_IN16) and the internal reference voltage input channel (ADC_IN17).

The temperature sensor reflects temperature changes and is not suitable for measuring absolute temperature. To measure the accurate temperature, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a stable voltage output (1.2V) for ADC.

If ADC collects the external input voltage during use and the sampled data fluctuates greatly, it may be caused by interferences due to power supply fluctuation. In this case, calibration can be done by sampling the internal VREFINT to derive the external sampled voltage.

When designing the ADC circuit, it is recommended to install a small capacitor of 500 pF at the ADC input pins.

Figure 2-17. Design of ADC acquisition circuit



When f_{ADC} is 15 MHz, the relation between the input impedance and the sampling period is as follows. To obtain better conversion results, it is recommended to reduce f_{ADC} as much as possible during use, try to select a large value of sampling period, and minimize the input impedance when designing external circuits. If necessary, the op-amp following should be used to reduce the input impedance.

Table 2-3. Relation between sampling period and external input impedance when f_{ADC} is 15MHz

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (KΩ)
2.5	0.17	1.4
14.5	0.97	10.5
27.5	1.83	20.5

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (KΩ)
55.5	3.7	41.8
83.5	5.57	63.2
111.5	7.43	84.6
143.5	9.57	109
479.5	31.97	365.5

2.5.3. DAC circuit

The digital/analog converter of GD32A503 MCU can convert 12-bit digital data into voltage output on external pins. The data can be in 8-bit or 12-bit mode and left-aligned or right-aligned mode. When the external trigger is enabled, DMA can be used to update the digital data at the input. When the voltage is output, the DAC output buffer can be enabled to obtain higher drive capability.

Table 2-4. Description of related DAC pins

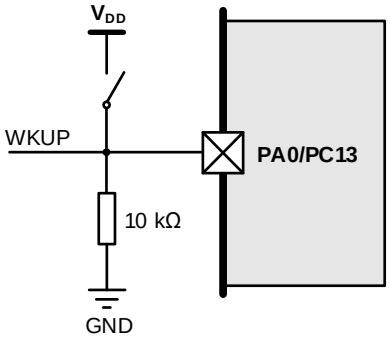
Name	Description	Signal type
V_{DDA}	Analog power	Input analog power
V_{SSA}	Analog power ground	Input analog power ground
V_{REFP}	DAC positive reference voltage, $2.7V \le V_{REFP} \le V_{DDA}$	Input analog positive reference voltage
DAC_OUTx	DAC analog output	Analog output signal

Before the DAC module is enabled, the GPIO port (PA7 corresponds to DAC_OUT) should be configured as analog mode.

2.5.4. Wake-up circuit in standby mode

GD32A503 supports three power saving modes, including sleep mode, deep sleep mode, and standby mode. The mode with the minimum power consumption is the standby mode, which requires the maximum wake-up time. In the standby mode, wake-up can be realized through the rising edge of the WKUP pin. At this time, just configure the WUPEN0/WUPEN1 bit in the register PMU_CS rather than GPIO. The reference circuit design of the WKUP wake-up pin is as follows:

Figure 2-18. Recommended circuit design for external wake-up pin in standby mode



Notes:

1. During circuit design in this mode, if there are series resistors between the WKUP pin and V_{DD}, additional power consumption may be generated.
2. If the WUPEN0 bit is set to 1 before entering the standby mode, the rising edge of PA0 will wake up the system from the standby mode. After WUPEN0 is set, PA0 will be internally configured as input pull-down mode. When the PA0 input is already high, setting the WUPEN0 bit will set the WUF bit. The same applies to other WKUP bits. For details, see the user manual.

2.6. Download debug circuit

The core of GD32A503 supports JTAG debug interface and SWD interface. The standard JTAG interface is a 20-pin interface, including 5-wire signal interface. The standard SWD interface is a 5-pin interface, including 2-wire signal interface. JTAG interface includes JTAG clock pin (JTCK), JTAG mode selection pin (JTMS), JTAG data input pin (JTDI), JTAG data output pin (JTDO), and JTAG reset pin (NJTRST, active low level). Serial Wire Debug (SWD) provides an interface with two pins: data input and output pin (SWDIO) and clock pin (SWCLK). The two pins of the SWD interface are multiplexed with the two pins of the JTAG debug interface: SWDIO is multiplexed with JTMS, and SWCLK is multiplexed with JTCK.

Note: After resetting, the debug related ports are in input PU/PD mode, where:

PB7: JTDI is in pull-up mode.
PB8: JTCK/SWCLK is in pull-down mode.
PB9: JTMS/SWDIO is in pull-up mode.
PB3: NJTRST is in pull-up mode.
PB4: JTDO is in floating mode.

Table 2-5. Allocation of JTAG download debug interfaces

Alternate function	GPIO port
JTMS	PB9
JTCK	PB8
JTDI	PB7
JTDO	PB4
NJTRST	PB3

Figure 2-19. Recommended JTAG wiring reference design

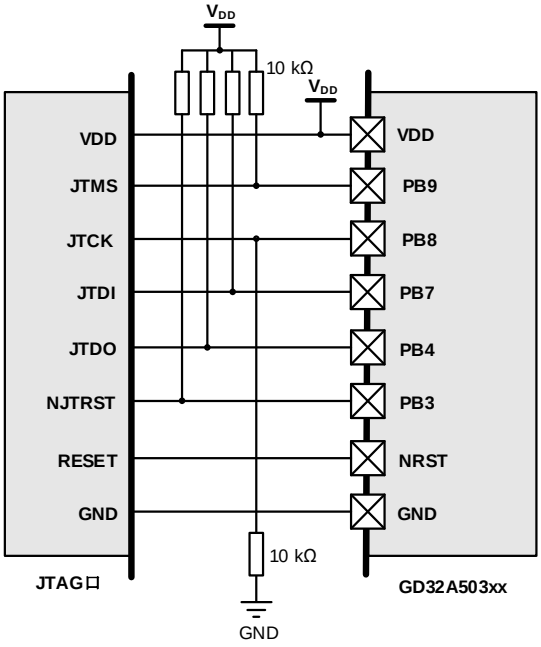
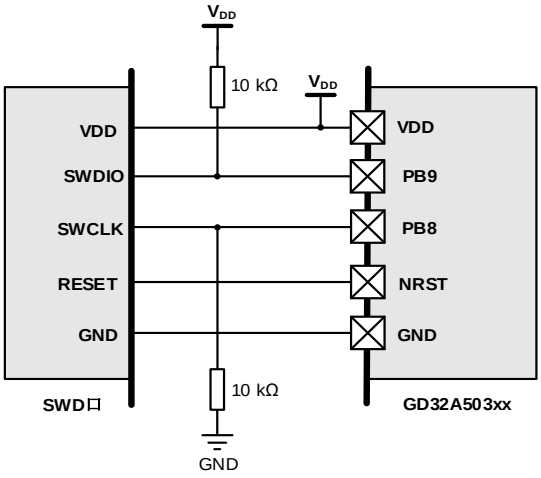


Table 2-6. Allocation of SWD download debug interfaces

Alternate function	GPIO port
SWDIO	PB9
SWCLK	PB8

Figure 2-20. Recommended SWD wiring reference design

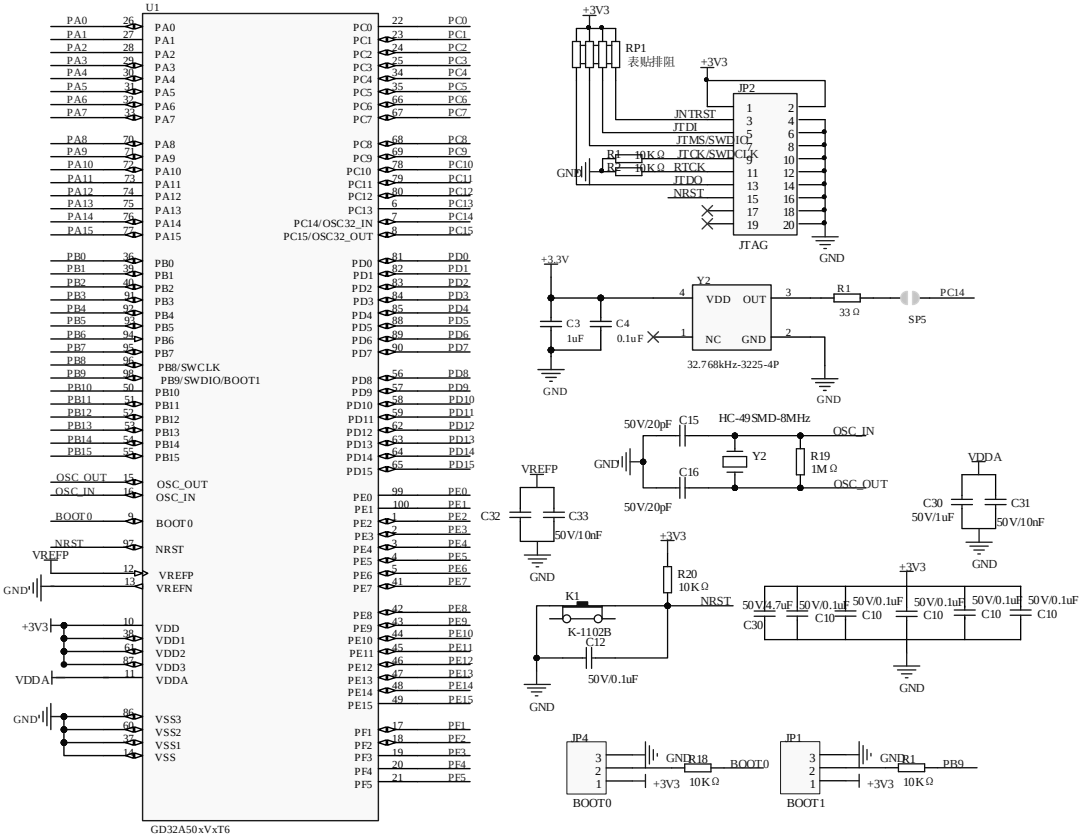


The following methods can be used to improve the reliability of SWD download debug communication and enhance the anti-interference capacity of download debug.

1. Shorten the length of the two signal wires of SWD to not more than 15 cm.
2. Twist the two SWD wires and the GND wire together.
3. Connect a small capacitor of tens of pF in parallel at two signal wires of SWD to GND.
4. Connect a 100 Ω - 1 KΩ resistor in series to any IO of two signal wires of SWD.

2.7. Reference schematic diagram design

Figure 2-21. Reference schematic diagram design recommended for GD32A503



3. PCB layout design

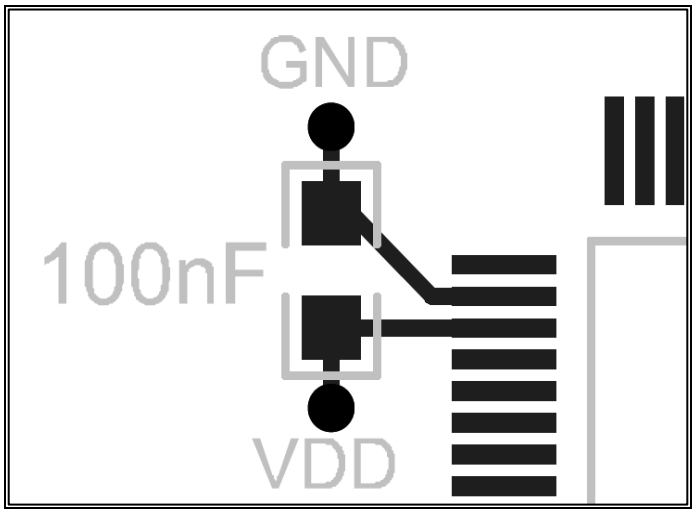
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design scheme with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping MCU away from these strong interference sources.

3.1. Power supply decoupling capacitor

The power supply of GD32A503 has VDD, VDDA, VREF, and other power supply pins. The 100nF decoupling capacitor can be ceramic MLCC which should be installed as close as possible to the power supply pins. The power supply should be wired to the power supply pins of MCU through the capacitor. It is recommended to punch holes close to the capacitor pad for the layout.

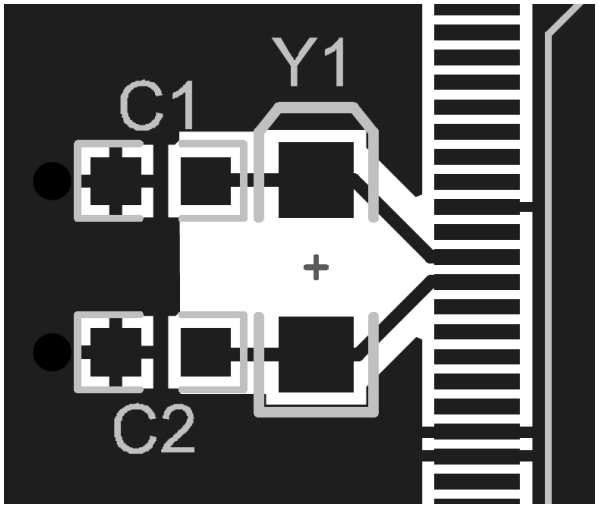
Figure 3-1. Recommended layout design of decoupling capacitor at power supply pins



3.2. Clock circuit

When HXTAL (passive crystal oscillator) is used as the clock source of GD32A503, the clock circuit (including the crystal or crystal oscillator and capacitors, etc.) should be installed close to the clock pins of MCU, and the clock wiring should be wrapped by GND as much as possible.

Figure 3-2. Recommended clock pin layout design (passive crystal)



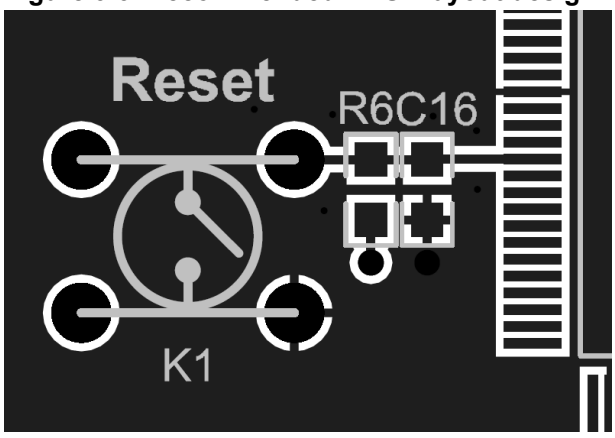
Notes:

1. The crystal shall be as close as possible to the clock pins of MCU, and the matching capacitors should be as close as possible to the crystal.
2. The whole circuit should be arranged on the same layer as MCU as much as possible, and the wiring should not pass through the layer as much as possible.
3. The PCB area of the clock circuit should be kept empty as much as possible and free of any wiring irrelevant to the clock.
4. Components with high power and strong interference risks and high-speed wiring should be kept away from the clock crystal circuit as much as possible;
5. The clock wire shall be wrapped by GND to achieve a shielding effect.

3.3. Reset circuit

The reference PCB layout for NRST wiring is as follows:

Figure 3-3. Recommended NRST layout design



Note: The resistors and capacitors of the reset circuit should be installed as close as possible to the NRST pins of MCU, and the NRST wiring should be kept away from components with strong interference risks and high-speed wiring as much as possible. If conditions permit, it is better to wrap the NRST wiring by GND to achieve a better shielding effect.

4. Package description

GD32A503 has a total of 4 package types, namely LQFP100, LQFP64, LQFP48, and QFN32.

Table 4-1. Description of package types

Ordering code	Package
GD32A503VxT6	LQFP100(14x14, 0.5pitch)
GD32A503RxT6	LQFP64(10x10, 0.5pitch)
GD32A503CxT6	LQFP48(7x7, 0.8pitch)
GD32A503KxQ6	QFN32(5x5, 0.5pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial release	April.7, 2023
1.1	Update section 2.1.3 to provide all packaging power supply design drawings, explaining the connection of relevant pins within the chip	Jun.21, 2023
1.2	Refine the content related to power detection and reset, adding Section 2.2	Dec.15, 2024

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