GigaDevice Semiconductor Inc.

IEC61000-4-2 System-Level ESD Test

Application Note
AN127

Revision 1.0

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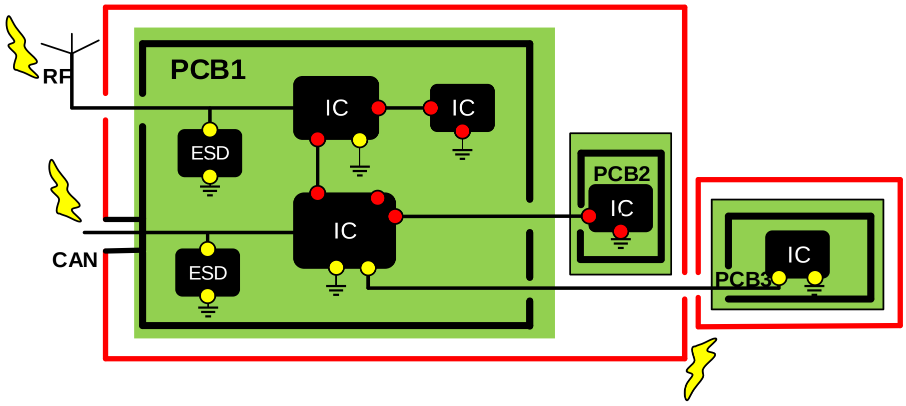
1. Introduction

With the reduction of semiconductor process and the improvement of performance, MCU faces a more complex electromagnetic environment. Especially when MCU suffers from direct discharge from operators and electrostatic discharge from neighboring objects, it may lead to reset, crash, hard failure and other problems of MCU control module in the system, affecting the normal work of the entire control system. Therefore, it is necessary to evaluate the anti-interference ability of MCU to electrostatic discharge in order to design a system that meets the application requirements. IEC61000-4-2 is an internationally unified standard for the evaluation of electrostatic discharge immunity. It describes the anti-interference requirements and test methods of electrical and electronic equipment subjected to electrostatic discharge from direct discharge by the operator and from adjacent objects. The standard provides the standard electrostatic discharge current waveform parameters, test voltage grade range, test equipment requirements, test Settings, test procedures and other specifications as well as the grade evaluation method of electrostatic discharge immunity, which establishes a general and repeatable standard for designers and testers to evaluate the performance of electrical and electronic equipment subjected to electrostatic discharge. Product developers can according to IEC61000-4-2 system level ESD testing, to simulate the actual end user ESD events, test the MCU resistance to electrostatic discharge anti-interference ability and according to the experience gained in the test, product optimization design. This application note introduces the IEC61000-4-2 system-level ESD test of GD32 MCU.

2. IEC61000-4-2 Overview of system-level ESD testing

The electrostatic discharge (ESD) immunity test provided in the IEC61000-4-2 system-level ESD test can be used to evaluate the immunity of GD32 MCU to electrostatic interference during the system protection design process. One type of static interference received by MCU is transmitted to MCU through the global pin of MCU, and the other type of static interference generated by operators or neighboring objects directly radiates to MCU from space. As is shown in ***Figure 2-1. Electrostatic coupling path***, global pins refer to pins susceptible to static interference in system protection design. For example, the static interference generated by operators or neighboring objects on RF ports, CAN ports or cables connected between boards outside PCB boards of MCU exposed to external environment is directly transmitted to MCU through global pins.

Figure 2-1. Electrostatic coupling path



In IEC61000-4-2 system-level ESD testing can choose MCU in the process of system protection design may be affected by electrostatic interference using ESD test system for contact discharge or air discharge test.

Contact discharge test can be applied directly to the global pin of MCU through the electrostatic gun head, or discharged to the horizontal coupling plate(HCP)or vertical coupling plate(VCP) through the electrostatic gun head, and the coupling plate indirectly carries out radioactive ESD discharge to MCU.

Air discharge test is to discharge MCU's global pin test by means of arc pulling of electrostatic gun head. Until MCU operation is abnormal, record the failure status and level of the system at this time and analyze the cause.

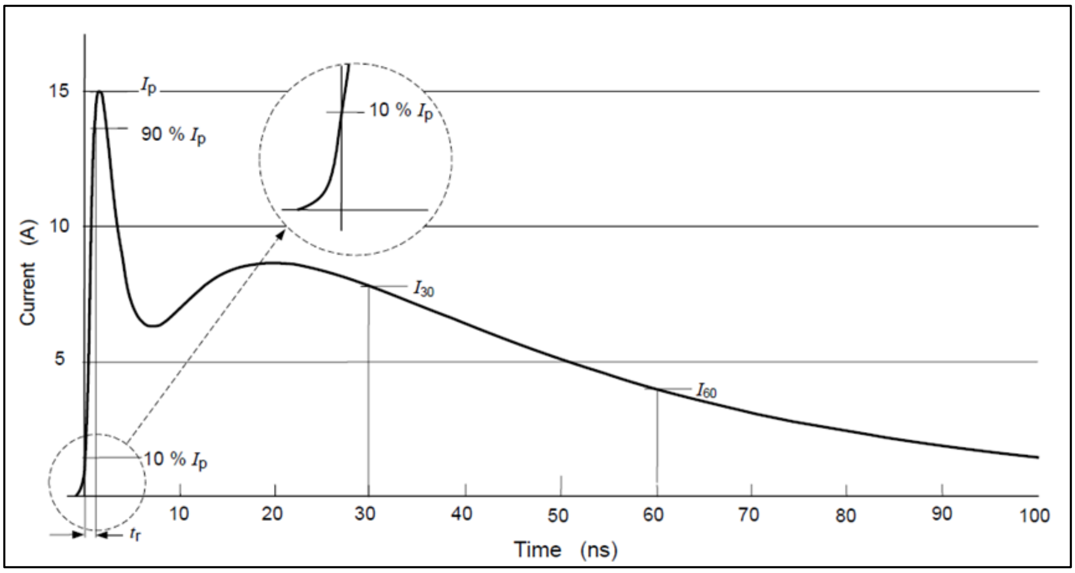
3. Waveform parameters of electrostatic discharge current (ESD)

The electrostatic discharge pulse applied to the tested equipment in the test is generated by the ESD generator. The manufacturer of the ESD generator has designed and manufactured in accordance with the standard to output the ESD pulse in line with the specification. It should be noted that the equipment in the test needs to be calibrated regularly to ensure the reliability of the test results. As is shown in ***Table 3-1. Contact discharge current waveform parameters***, the waveform parameters of IEC61000-4-2 contact discharge current are given. As is shown in ***Figure 3-1. Contact discharge 4kV ideal current waveform***, the ideal current waveform of 4kV contact discharge is given. Experimenters need to ensure that the specifications of the test equipment ESD electrostatic generator comply with the standard contact discharge current waveform parameters.

Table 3-1. Contact discharge current waveform parameters

Level	Voltage kV	First peak current ±15% A	Rise time tr (±25%) ns	Current (±30%) At 30 ns A	Current (±30%) At 60 ns A
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	6	8
The reference point for measuring the current at 30 ns and 60 ns is the moment when the current first reaches 10% of the first peak of the discharge current. Note: The rise time t_r is the interval between 10% and 90% of the first peak current.					

Figure 3-1. Contact discharge 4kV ideal current waveform

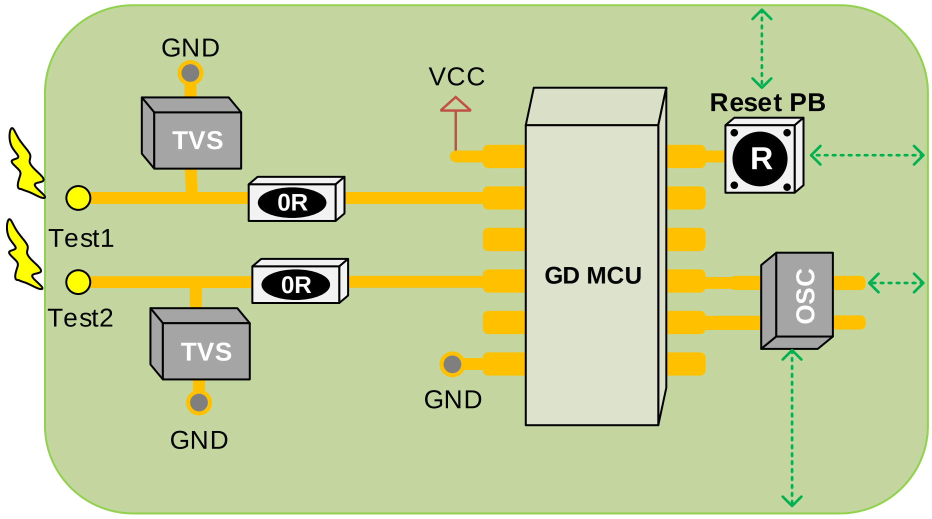


4. GD32 MCU system-level ESD test scheme

The GD32's system-level ESD and chip-level ESD tests are two different tests, referring to different test standards, and the two test result parameters are not related. The purpose of chip-level ESD testing is to test the antistatic performance of the chip in the process of wafer cutting, packaging, pre-factory testing, transportation, and PCB assembly and placement, and chip-level ESD occurs in the ESD protection area (EPA) power-off operation. System-level ESD testing is to measure the complex electrostatic environment faced by the chip in practical applications, rather than ESD controlled areas, and most MCU systems are in the process of power-on operation.

GD32 MCU IEC61000-4-2 system-level ESD test scheme is shown in ***Figure 4-1. GD32 MCU system-level ESD test scheme block diagram*** below, GD will Test 5V pins and non-5V pins of USART, I2C, CAN and other global pins that are easily exposed to the outside world. Here, the IO pins are equipped with TVS and a 0R resistor in series. System-level ESD discharge is located at the test point of the front end of TVS. The MCU is powered on to simulate system-level ESD events for real-world end users.

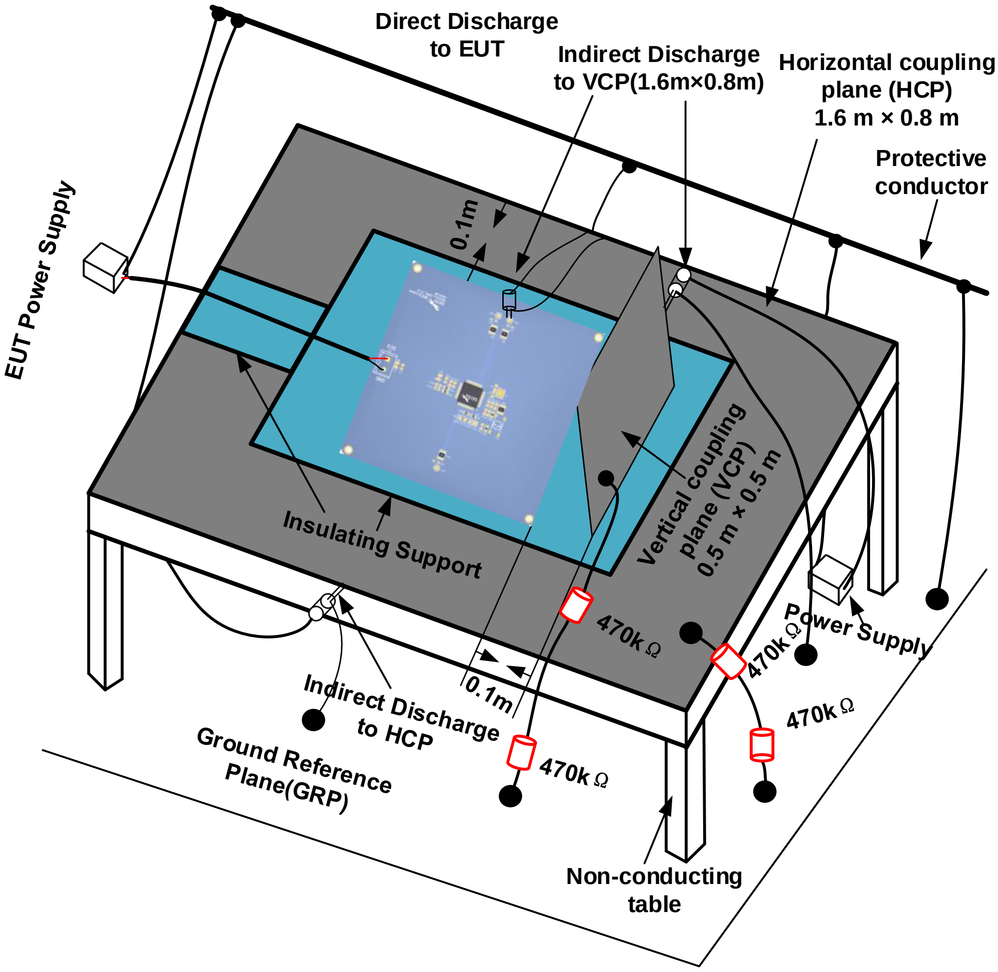
Figure 4-1. GD32 MCU system-level ESD test scheme block diagram



5. Test environment

The equipment used to perform system-level ESD testing is an ESD generator conforming to IEC 61000-4-2. The test methods are Contact Discharge (CD) and Air Discharge(AD). Contact discharge can be directly applied to the test pin of MCU through the electrostatic gun head, or it can be discharged to the horizontal coupling plate (HCP) or vertical coupling plate (VCP) through the electrostatic gun head, and the coupling plate indirectly carries out radioactive ESD discharge to MCU. Air discharge is the discharge of the test pin of MCU by the way of arc pulling of the electrostatic gun head. Contact discharge and air discharge use the corresponding electrostatic discharge gun head respectively. During the test, the ESD discharge level is from low to high, and positive and negative electrostatic voltage ≥10pcs is applied to each level until the MCU operation is abnormal, and the MCU failure state and failure level are recorded at this time. ***Figure 5-1. IEC61000-4-2 Console layout and grounding requirements*** shows the ESD console layout and grounding requirements.

Figure 5-1. IEC61000-4-2 Console layout and grounding requirements



The laboratory floor shall be equipped with a ground reference plane (GRP). It shall be sheet metal (copper or aluminum) with a minimum thickness of 0.25mm; Other metallic materials may be used, but their minimum thickness shall be at least 0.65mm. The grounding reference plane (GRP) should protrude at least 0.5 m from around the device or the horizontal coupling plane (when in use) and be connected to the Protective conductor system. Non-conductive table height (0.8 ± 0.08)m, placed on the ground reference plane (GRP). A (1.6 ± 0.02)m × (0.8 ± 0.02)m horizontal coupling plane (HCP) shall be placed on the work table, which shall consist of a metal sheet (copper or aluminum) of a minimum thickness of 0.25 mm (other metal materials may be used, but the minimum thickness shall be at least 0.65 mm), It should be connected to the GRP through a cable with a 470 kΩ resistance at both ends. The EUT equipment and its cables are isolated from the HCP coupling plane with an insulating support of (0.5 ± 0.05)mm thickness. The EUT equipment is at least 0.1m away from all HCP boundaries. A (0.5 ± 0.02)m × (0.5 ± 0.02)m vertical coupling plane (VCP) is placed on the insulating bracket, it consists of a metal sheet (copper or aluminum) with a minimum thickness of 0.25 mm (other metal materials can be used, but the minimum thickness is at least 0.65 mm) and is connected to the GRP by a cable with a 470 kΩ resistance at both ends. The distance between the EUT device and the VCP plane must be at least 0.1 m. The HCP and VCP grounding cables contain 470 kΩ drain resistors to prevent the charge from disappearing instantly after the generator is discharged on the coupling plane, increasing the impact of ESD events on the EUT. The resistance shall be able to withstand the maximum discharge voltage applied to the EUT plane during the test. Keep as close to both ends of the ground cable as possible to form a distributed resistance. EUT shall be arranged and connected according to their functional requirements. The distance between the EUT and the laboratory walls and any other metal structures should be at least 0.8 m. The discharge loop cable of the ESD generator should be connected to the ground reference plane.

In order to minimize the influence of environmental parameters on the experimental results, the experimental environment should meet the environmental temperature of 15°C ~ 35°C, relative humidity of 30% ~ 60%, atmospheric pressure of 86 kPa ~ 106 kPa, in which the environmental relative humidity will vary greatly with the seasons. Before the experiment, it is necessary to check the environmental relative humidity of the laboratory. If the humidity is higher than 60%, it is necessary to use a dehumidifier to reduce the air humidity to a suitable range before the experiment can be carried out. In order not to affect the experimental results, the electromagnetic conditions of the laboratory should ensure the normal operation of the tested equipment, and try to avoid other EMC experiments with strong interference at the same time. The test can be carried out after the completion of the test platform and parameter setting.

6. Evaluation of immunity level

In the process of testing, experiment grades are selected according to the standard. As is shown in ***Table 6-1. Test level*** ESD test voltage beyond the given value can be selected for some special application requirements.

Table 6-1. Test level

Contact discharge mode		Air discharge mode	
Level	Test voltage (kV)	Level	Test voltage (kV)
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
Special(1)	Customized	Special	Customized
(1). Special is any level of voltage, higher, lower, or somewhere in between. Special level According to the requirements of the specific application environment of the special device to be measured. If the voltage is higher than the specified voltage, a special test device must be used.			

After the test, records shall be made according to MCU's working conditions and functional requirements. The test results can be divided into 5 failure mode levels for MCU's system-level ESD according to IEC62132-1. As is shown in ***Table 6-2. IEC62132-1 Failure mode level of the MCU***, Where level A is no problem, BCD is soft failure type, and E is hard failure type.

Table 6-2. IEC62132-1 Failure mode level of the MCU

Level	Description
A	Unaffected: During and after the injection of pulses, ESD interference does not affect the chip.
B	Automatic recovery: During the pulse injection process, the chip operation becomes abnormal, but after the pulse injection, the chip will return to the original normal state.
C	Manual recovery: During the pulse injection process, the chip operation becomes abnormal. After the pulse injection, the chip cannot automatically return to the original normal state, but after the manual intervention (reset), the chip will return to the original normal state.
D	Restart: The chip does not work properly during or after pulse injection (reset does not work). The chip returns to the normal state only after the chip is powered on again, usually due to the latch up phenomenon.
E	Hard failure: Pulse injection of ESD has caused physical damage to the chip.

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Intial Release	Jul.01, 2023

Important Notice