

GigaDevice Semiconductor Inc.

GD32A513_Firmware_Library

Release Note

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1. 发布内容 Publishing content

1.1. 代码 Code

- GD32A513 Standard Peripheral Firmware
- GD32A513 Peripheral Examples
- GD32A513 Utilities
- GD32A513 Template

1.2. 文档 Document

- 《GD32A513_固件库使用指南》
- 《GD32A513_Firmware_Library_User_Guide》

2. 版本信息 Version information

名称Name	GD32A513_Firmware_Library.7z
版本Version	V1.2.0
发布日期Release date	2024.12.12
支持的开发板Supported boards	GD32A513V-EVAL-V1.0
编译环境Compiling environment	<ul style="list-style-type: none">■ IAR Embedded Workbench 8.32.1■ ARM Keil 5.29

3. 发布版本功能描述 Release feature description

类型Type	例程名称Demo Name	备注Description
Examples- ADC	ADC0_ADC1_regular_parallel	-
	ADC0_analog_watchdog_0	-
	ADC0_analog_watchdog_1	-
	ADC0_oversample_shift	-
	ADC0_regular_channel_discontinuous_mode	-
	ADC0_regular_channel_with_DMA	-
	ADC0_resolution	-
	ADC0_software_trigger_regular_channel_polling	-

	ADC0_temperature_Vref	-
Examples-BKP	Tamper	-
Examples-CAN	communication_classical_CAN	-
	communication_FDmode	展示如何使用CAN FD帧。 Demonstrate how to use CAN FD frames.
	communication_Loopback	-
	Pretended_Networking_mode	-
Examples-CMP	Blanking_output	-
	Interrupt	
	Port_output	-
	Timer0_CH0IC	-
Examples-CRC	CRC_calculate	-
Examples-DAC	DAC_ADC_convert	-
	DAC_output_voltage	-
	DAC_DMA_convert	-
	DAC_LFSR_noise_mode	-
	DAC_TRIGSEL_trigger	通过TRIGSEL选配触发信号，触发DAC。 Trigger the DAC by selecting the trigger signal through TRIGSEL.
	DAC_triangle_noise_mode	-
Examples-DBG	DBG_timer1_stop	-
Examples-DMA	DMA_RequestGen	-
	DMA_SYNC	-
	RAM_TO_RAM	-
	RAM_TO_USART	-
	Reload_exti	-
Examples-EXTI	Key_external_interrupt_mode	-
Examples-FMC	Data_flash_erase_program	展示对Data flash进行擦除和编程，包括正常编程和快速编程操作。 Demonstrate the erasing and programming of Data flash, including normal programming and fast programming operations.
	Erase_Program	-
	Write_protection	-
Examples-FWDGT	FWDGT_key	-
Examples-GPIO	Keyboard_polling_mode	-
	Running_led	-

Examples-I2C	I2C_EEPROM	-
	I2C_EEPROM_dma	-
	I2C_EEPROM_interrupt	-
	Master_receiver	-
	Master_receiver&slave_transmitter	-
	Master_receiver&slave_transmitter_interrupt	-
	Master_transmitter	-
	Master_transmitter&slave_receiver	-
	Master_transmitter&slave_receiver_dma	-
	Master_transmitter&slave_receiver_interrupt	-
	Slave_receiver	-
	Slave_transmitter	-
Examples-MFCOM	MFCOM_I2C	-
	MFCOM_I2S	-
	MFCOM_SPI	-
	MFCOM_UART	-
Examples-PMU	Deepsleep_wakeup_exti	-
	Deepsleep_wakeup_RTC	-
	Low_voltage_detector	-
	Over_voltage_detector	-
	Standby_wakeup_pin	-
	Standby_wakeup_RTC	-
Examples-RCU	Ckout_pin_clock_output	-
	Reset_source_detect	-
	System_clock_switch	-
Examples-RTC	Calendar_demo	-
Examples-SPI	I2S_master_transmit_dma	-
	I2S_slave_recieve_dma	-
	SPI_master_slave_full duplex_dma	-
	SPI_master_slave_full duplex_nssp_mode	-
	SPI_master_slave_full duplex_polling	-
	SPI_master_slave_full duplex_ti_mode	-
	SPI_master_slave_simplex_dma	-
	SPI_master_transmit_slave_receive_interrupt	-
Examples-TIMER	TIMER0_6-steps	展示如何配置TIMER0外设以生成带有死区时间的三个互补信号。 Demonstrate how to configure the TIMER0 peripheral to generate three complementary signals with dead time.
	TIMER0_deadtime_break	-
	TIMER0_dma	-

	TIMER0_dma_burst	-
	TIMER0_pwmout_complementarysignals	-
	TIMER0_pwmout_independtsignals	-
	TIMER1_extclock_count	-
	TIMER1_exttrigger	-
	TIMER1_inputcapture	-
	TIMER1_ocactive	-
	TIMER1_ocinactive	-
	TIMER1_octoggle	-
	TIMER1_pwminputcapture	-
	TIMER1_pwmout	-
	TIMER1_singlepulse	-
	TIMER1_timebase	-
	TIMERs_cascadesynchro	-
	TIMERs_parallelsynchro	-
Examples- TRIGSEL	cmp_trigger_extout	展示如何使用CMP和TRIGSEL输出CMP0_OUT。TRIGSEL选择CMP0_OUT作为触发源，然后CMP0_OUT输出到TRIGSEL EXTOUT0。 Demonstrate how to use CMP and TRIGSEL to output CMP0_OUT. TRIGSEL selects CMP0_OUT as the trigger source, and then CMP0_OUT is output to TRIGSEL EXTOUT0.
	extinput_trigger_timer1	-
	Timer0_pwm_trigger_adc	-
Examples- USART	DMA_transmitter&receiver	-
	DMA_transmitter&receiver_interrupt	-
	Half_duplex_transmitter&receiver	-
	IDLE_receiver_interrupt	-
	Printf	-
	Receiver_timeout	-
	Synchronous	-
	Transmitter&receiver_interrupt	-
Examples- WWDGT	WWDGT_delay_feed	-

4. 发布版本变更列表 Release the changelist

序号 Serial number	模块 Module	接口名 Interface name	变更原因 Reason of change	变更内容 Content of change	变更版本 Change version
1	System	void	为了增强MCU的健壮	在system_gd32a513.c文件中针对升频和	V1.2.0

		SystemInit(void) / static void system_clock_24m_ pll_irc8m(void) / static void system_clock_48m_ pll_irc8m(void) / static void system_clock_72m_ pll_irc8m(void) / static void system_clock_100m_ pll_irc8m(void) / static void system_clock_24m_ pll_hxtal(void) / static void system_clock_48m_ pll_hxtal(void) / static void system_clock_72m_ pll_hxtal(void) / static void system_clock_100m_ pll_hxtal(void)	性。 To enhance the robustness of the MCU operation, switch frequencies in a stepwise manner during frequency switching.	降频阶段增加3级切频功能。 Add a three-step frequency switching function in the system_gd32a513.c file for both increasing and decreasing frequency stages.	
2	FMC	-	GD32A513系列删除硬件EEPROM功能。 Remove the EEPROM function in the GD32A513 series.	在 FMC 标准库中删除所有关于硬件EEPROM相关的API接口。 Remove all API interfaces and function macros related to EPROM functions from the FMC standard library.	V1.2.0
3	USART	void usart_baudrate_set(uint32_t usart_periph, uint32_t baudval)	提升API接口的健壮性。 Improve the robustness of the API interface.	API接口内针对波特率参数增加除零的判断。 The API interface should add a judgment for the baud rate parameter being 0 to prevent the application layer from setting the baud rate parameter to 0, which would cause a divide-by-zero error.	V1.2.0
4	SYSCFG	-	缺少 SYSCFG_CFG0寄存器中PF0映射的宏定义。 There is a lack of macro definition for the PF0 remapping in the	增加 SYSCFG_CFG0寄存器中PF0映射的宏定义。 Add the SYSCFG_CFG0 register PF0 remapping operation macro.	V1.2.0

			SYSCFG_CFG0 register.		
6	CRC	uint32_t crc_block_data_calculate(void *array, uint32_t size, uint8_t data_format)	解决API接口的违反MISRA C 2004 17.4规则。 Resolve the issue of API interfaces violating the MISRA C 2004 rule 17.4.	修改API的内部实现，避免对指针使用数组索引。 Modify the internal implementation of the API interface to avoid using array indexing on pointers.	V1.2.0
7	CAN-Example	-	使用CAN的时钟源受到限制，可参考GD32A513系列的勘误手册。 The use of the CAN module clock source is restricted and should be referred to the errata.of GD32A513 series.	CAN的时钟源默认配置为PCLK2。 The CAN clock source defaults to PCLK2	V1.2.0

5. 发布版本已知问题勘误 Known errata in the release version

序号 Serial number	模块 Module	BUG 描述 BUG description	规避方式 Method of evasion

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