GigaDevice Semiconductor Inc.

Development Guide for GD32VW553 series MCU in SEGGER Embedded Studio IDE

Application Note
AN186

Revision 1.0

(Jan. 2024)

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1. Introduction

The devices of GD32VW553 series MCU are 32-bit general-purpose microcontrollers based on the Nuclei N307 processor. The N307 processor is based on the RISC-V architecture instruction set.

This application note is designed to help users to build and develop GD32VW553 series MCU project in SEGGER Embedded studio for RISC-V (SES) IDE.

2. Development environment

- Evaluation board: GD32VW553H-EVAL-V1.1
- Hardware debugger: J-Link V11 / V12
- IDE: SEGGER Embedded Studio for RISC-V V7.32a
- Operating system: WIN10 64-bit OS

3. Project development

3.1. Device support package installation

The device support package can be installed online or offline in SES (the offline package is available from https://gd32mcu.com), which refers to ***Figure 3-1. Device support package installation options***. Open SES software, online package can be installed by "Package Manager...", which refers to ***Figure 3-2. Device support package installation online***; offline package can be installed by "Manually Install Packages...", which refers to ***Figure 3-3. Device support package installation offline***..

Figure 3-1. Device support package installation options

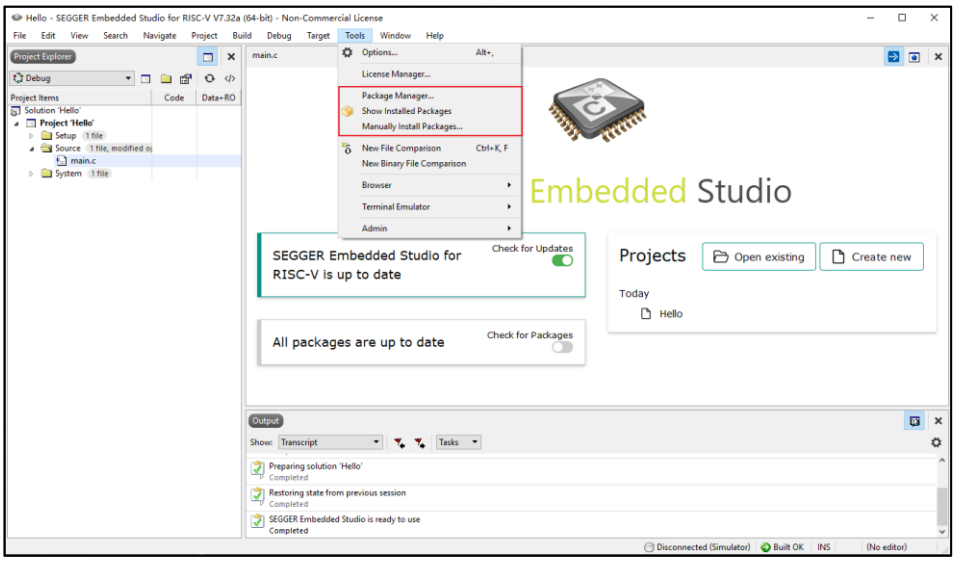


Figure 3-2. Device support package installation online

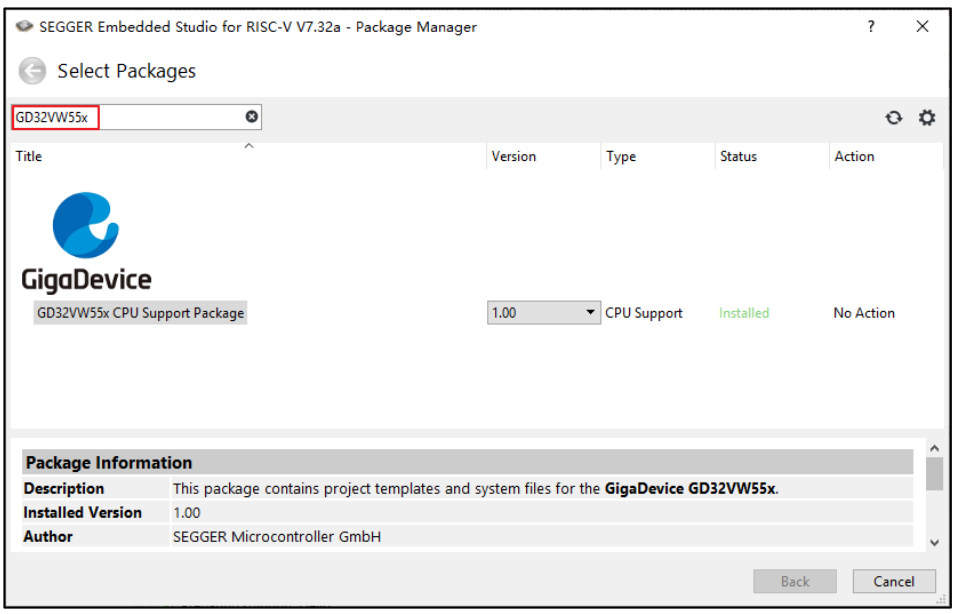
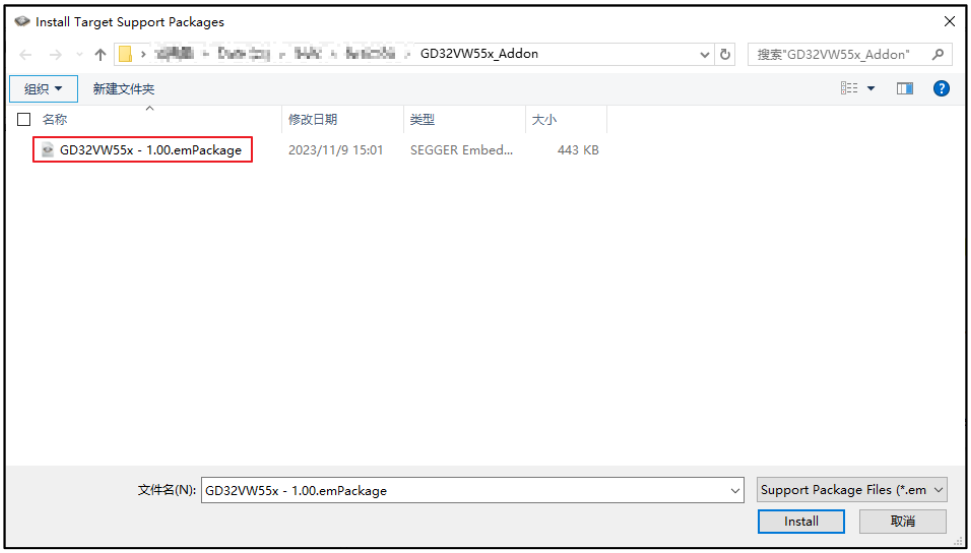


Figure 3-3. Device support package installation offline

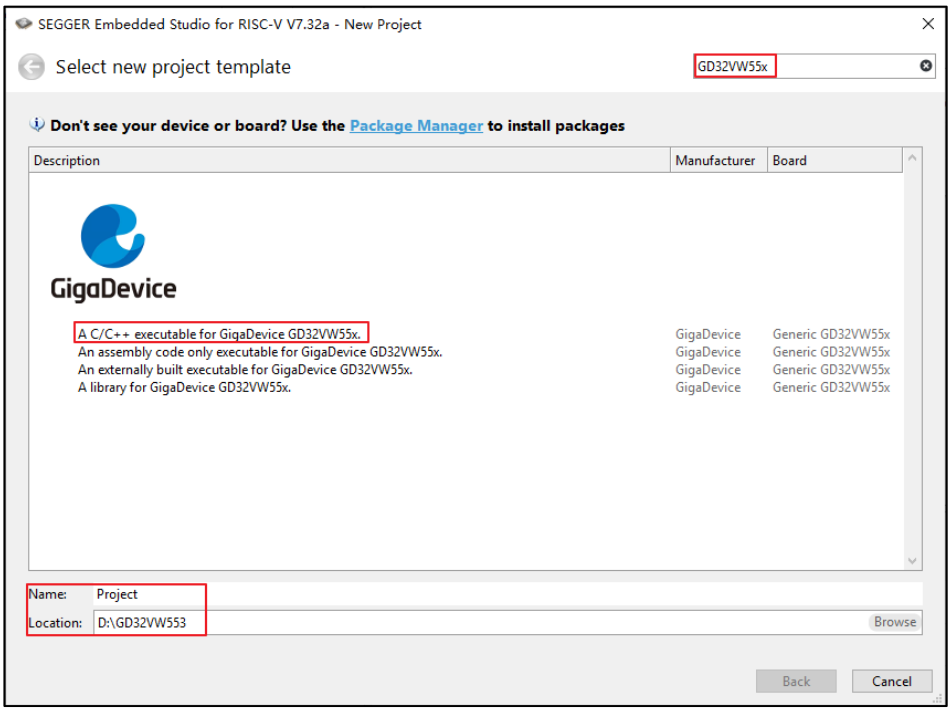


3.2. Create project based on the template

The steps to create a new project based on the template are as follows:

Step 1: Open SES software and clicking "File->New Project" option and then choose "A C/C++ executable for GigaDevice GD32VW55x" and set the project name and location to create project, which refers to ***Figure 3-4.Create a project based on the template***.

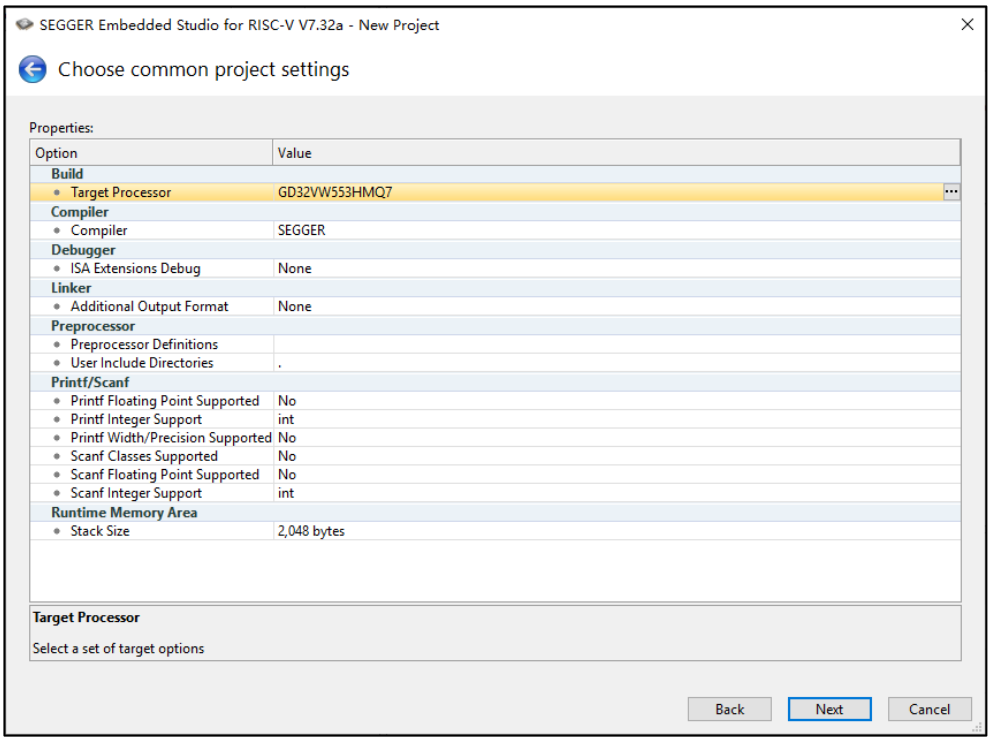
Figure 3-4.Create a project based on the template



Step 2: Click "Next" to enter the common project setting interface, including chip selection, compiler type selection, link output format selection, predefined macro setting, header file

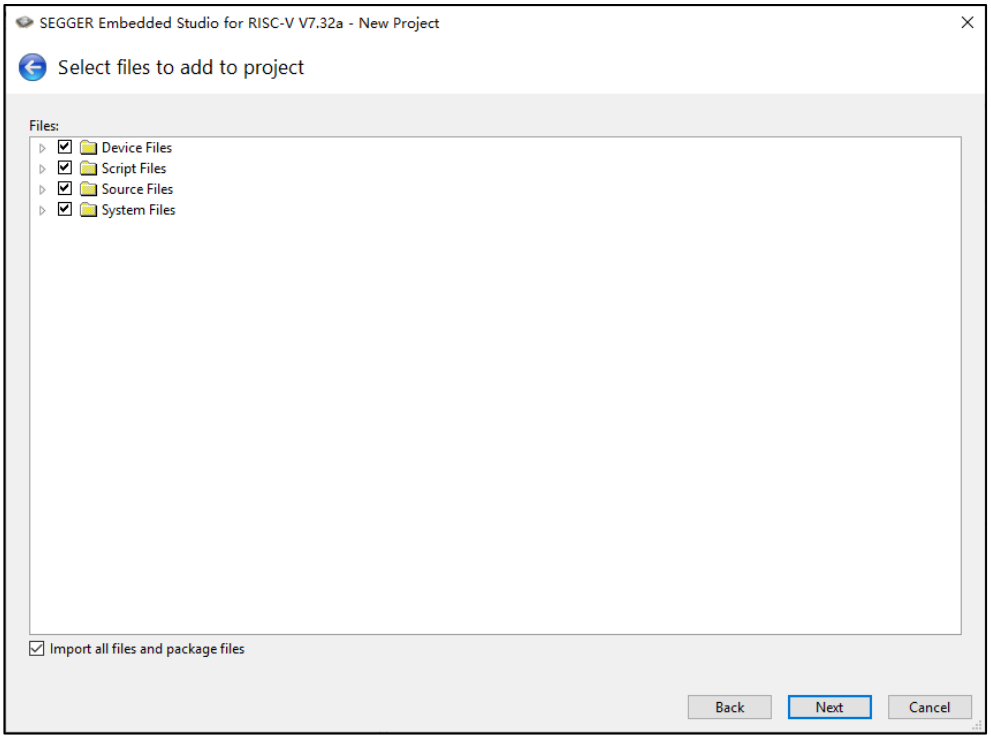
containing path setting, input/output support and stack size configuration, which refers to ***Figure 3-5.Common project settings based on the template***.

Figure 3-5.Common project settings based on the template



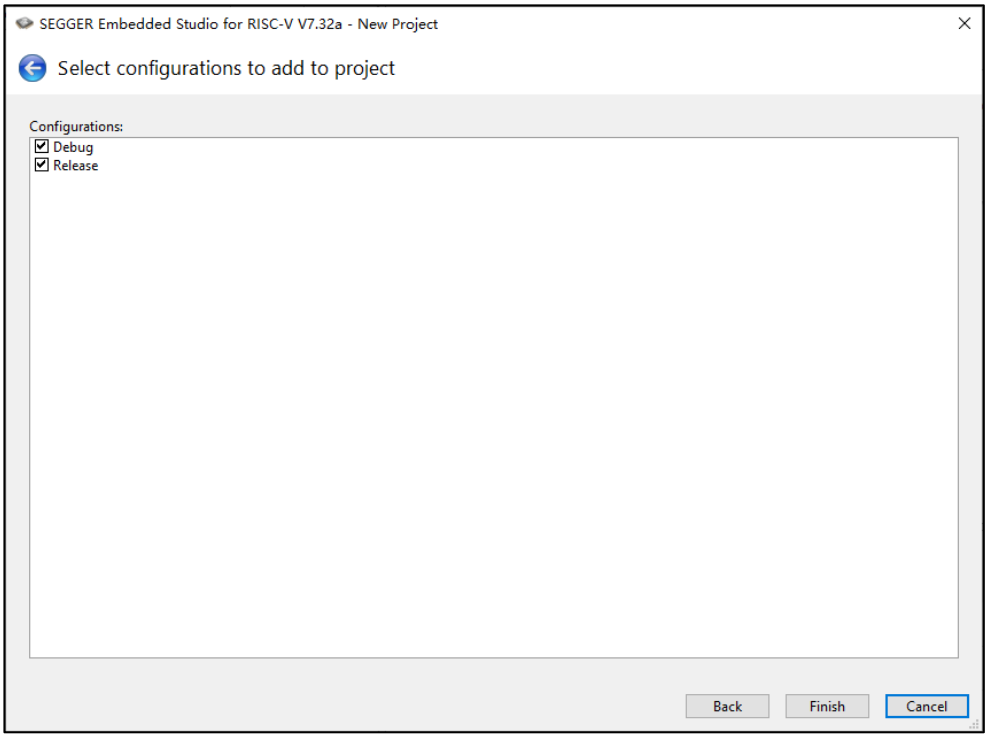
Step 3: Click "Next" to enter the project files selection interface and the default selection should be used, which refers to ***Figure 3-6.Project files selection based on the template***.

Figure 3-6.Project files selection based on the template



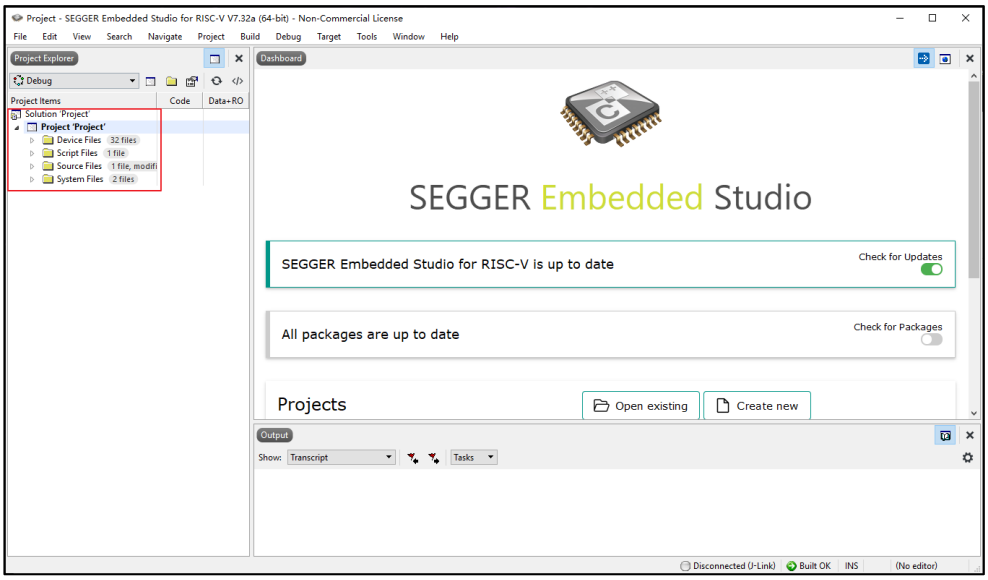
Step 4: Click "Next" to enter the project configurations interface, which refers to ***Figure 3-7.Project configurations based on the template***.

Figure 3-7.Project configurations based on the template



Step 5: Click "Finish" to enter the project interface, users can carry out secondary development based on this template project, which refers to ***Figure 3-8. New project based on the template***.

Figure 3-8. New project based on the template

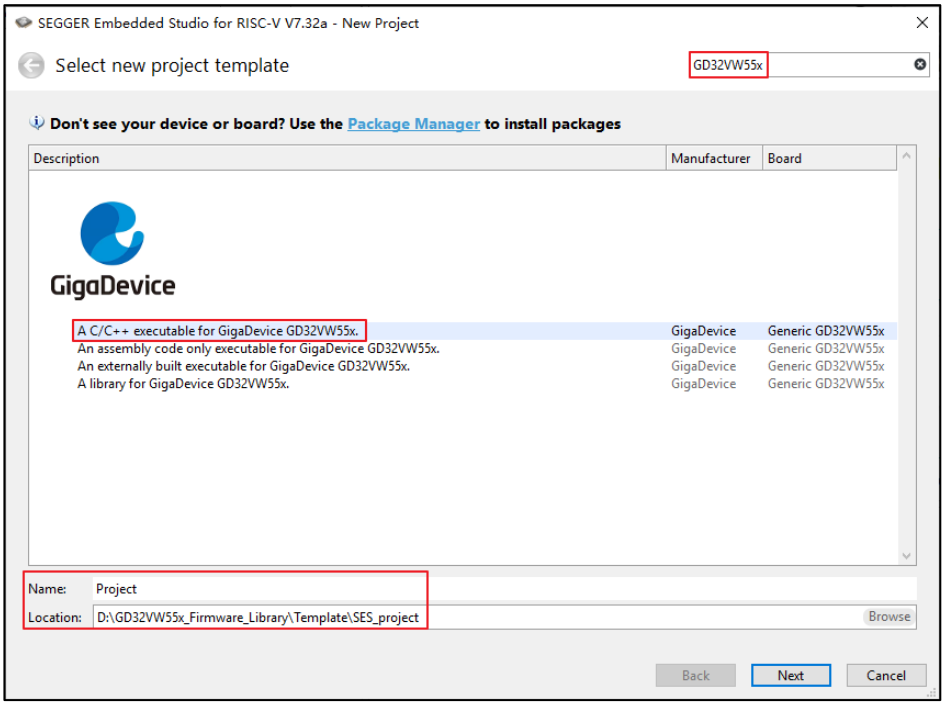


3.3. Create project based on the standard firmware library

The steps to create a new project based on the standard firmware library are as follows:

Step 1: Open SES software and clicking "File->New Project" option and then choose "A C/C++ executable for GigaDevice GD32VW55x" and set the project name and location to create project, which refers to ***Figure 3-9. Create a new project based on the standard firmware library***.

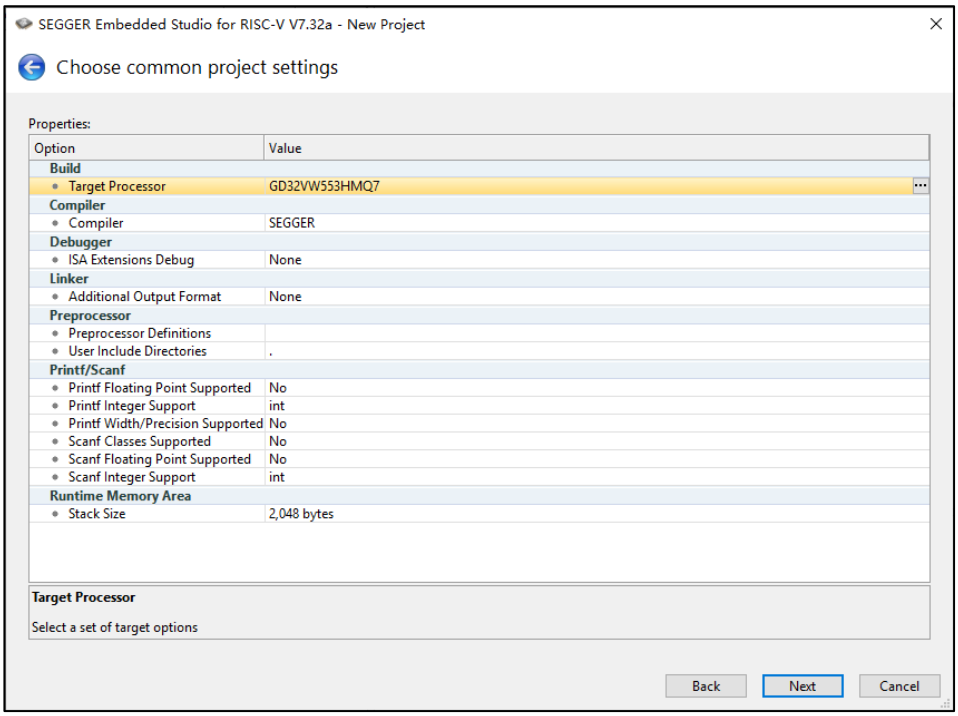
Figure 3-9. Create a new project based on the standard firmware library



Step 2: Click "Next" to enter the common project setting interface, including chip selection,

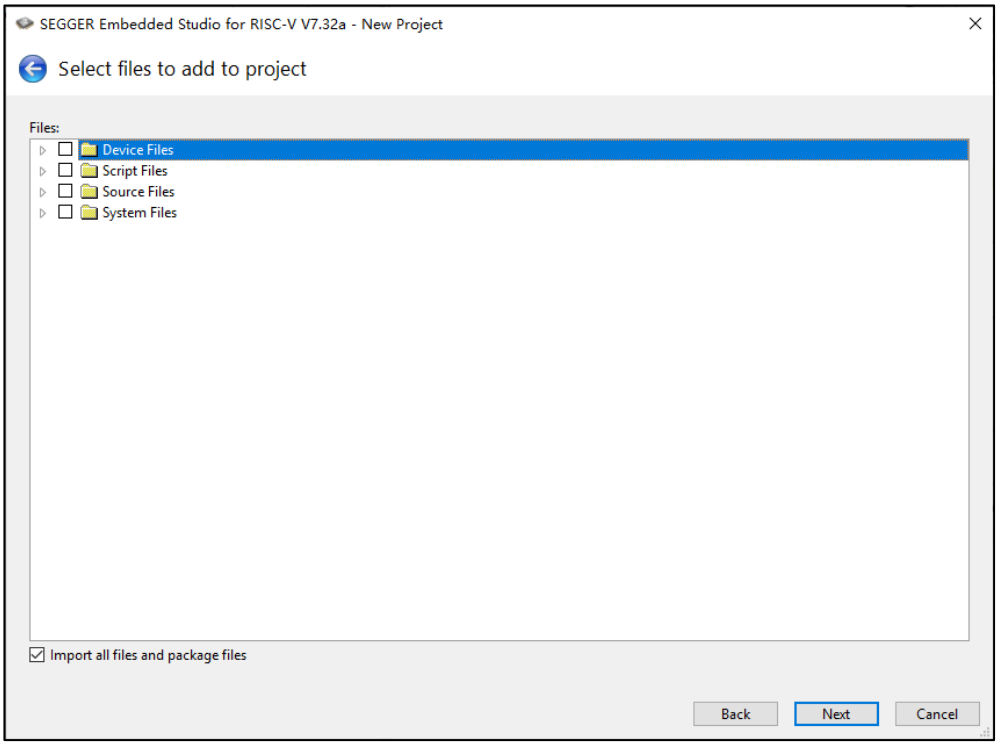
compiler type selection, link output format selection, predefined macro setting, header file containing path setting, input/output support and stack size configuration, which refers to ***Figure 3-10. Common project settings based on the standard firmware library***.

Figure 3-10. Common project settings based on the standard firmware library



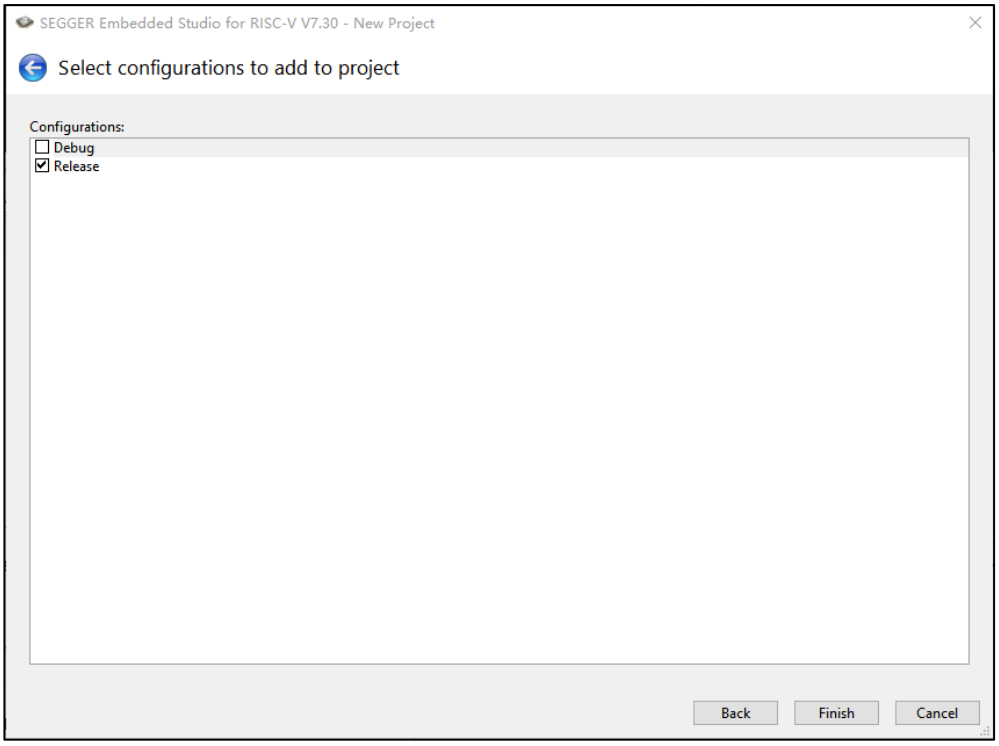
Step 3: Click "Next" to enter the project files selection interface, uncheck all the default configuration items, which refers to ***Figure 3-11. Project files selection based on the standard firmware library***.

Figure 3-11. Project files selection based on the standard firmware library



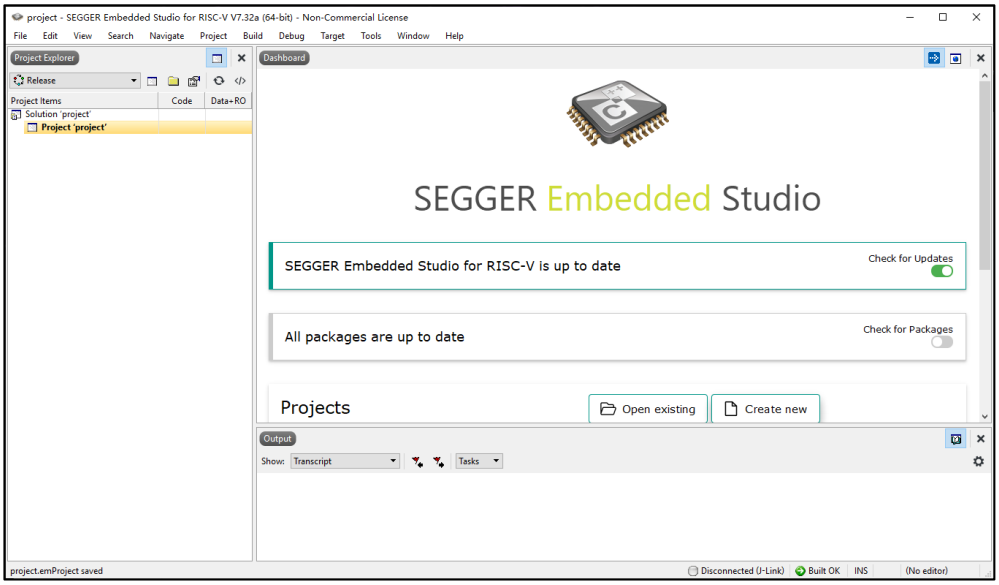
Step 4: Click "Next" to enter the project configuration interface, which refers to ***Figure 3-12. Project configurations based on the standard firmware library***.

Figure 3-12. Project configurations based on the standard firmware library



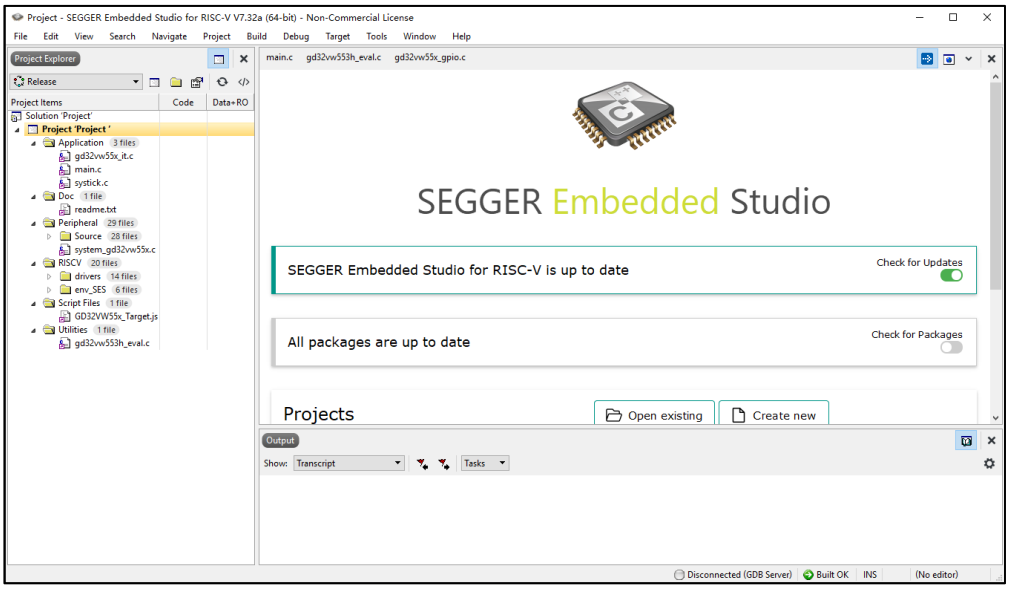
Step 5: Click "Finish" to enter the project interface, users can carry out secondary development based on this empty project, which refers to ***Figure 3-13. Empty project***.

Figure 3-13. Empty project



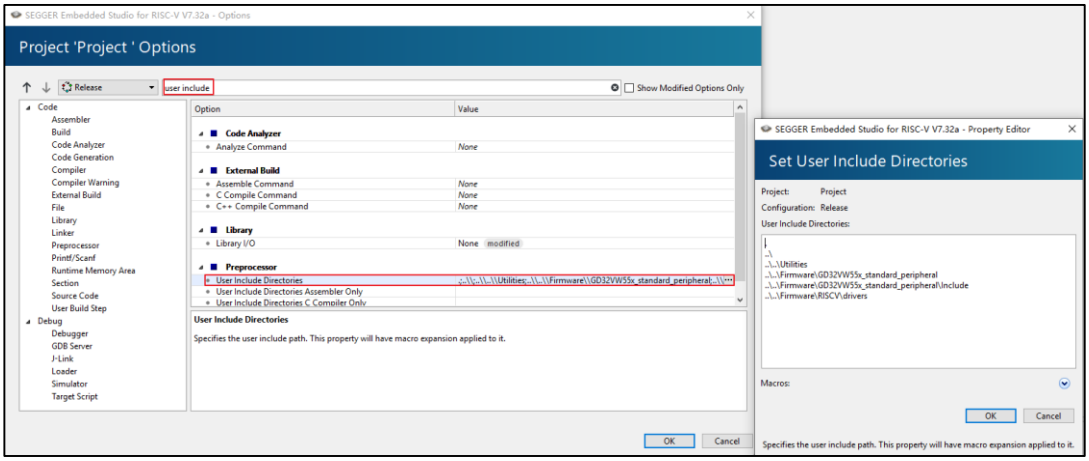
Step 6: Organize the firmware library files according to the following structure, which refers to ***Figure 3-14. Project files*** . The specific file structure can refer to firmware library template project.

Figure 3-14. Project files structure



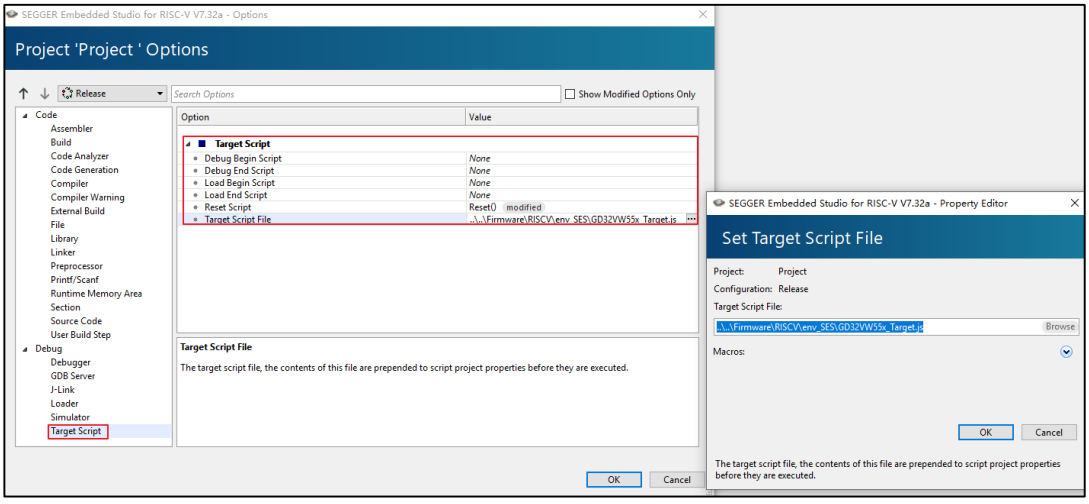
Step 7: Click "Project->Options" to enter project options interface and configure header file containing path, which refers to ***Figure 3-15. User include directory configurations***.

Figure 3-15. User include directory configurations



Step 8: Click "Project->Options" to enter project options interface and configure the script file, which refers to ***Figure 3-16. Scripts configurations***.

Figure 3-16. Scripts configurations

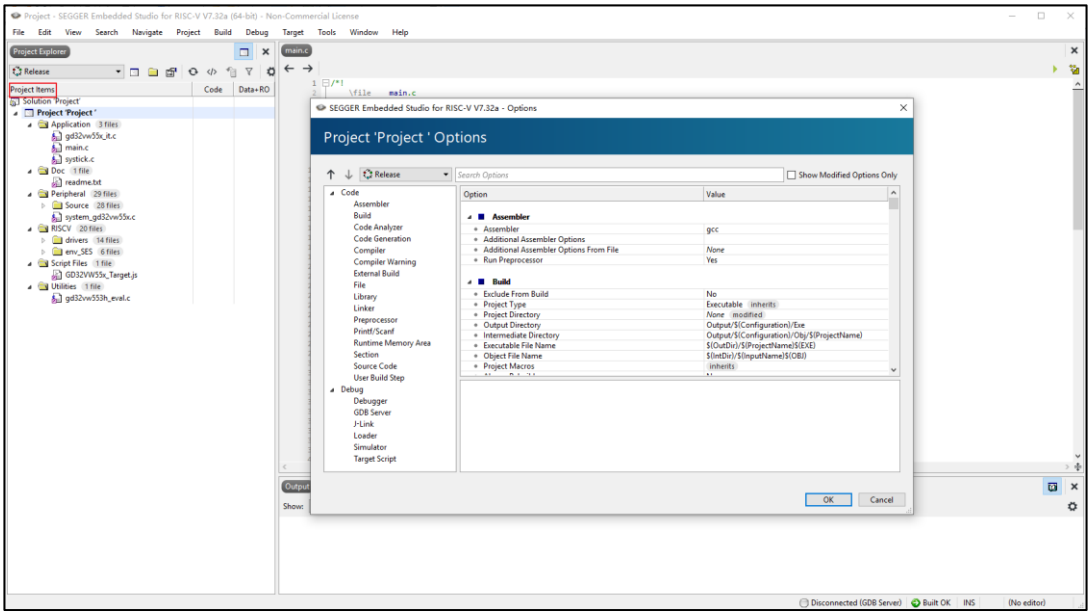


4. IDE interface introduction

4.1. Project configuration options

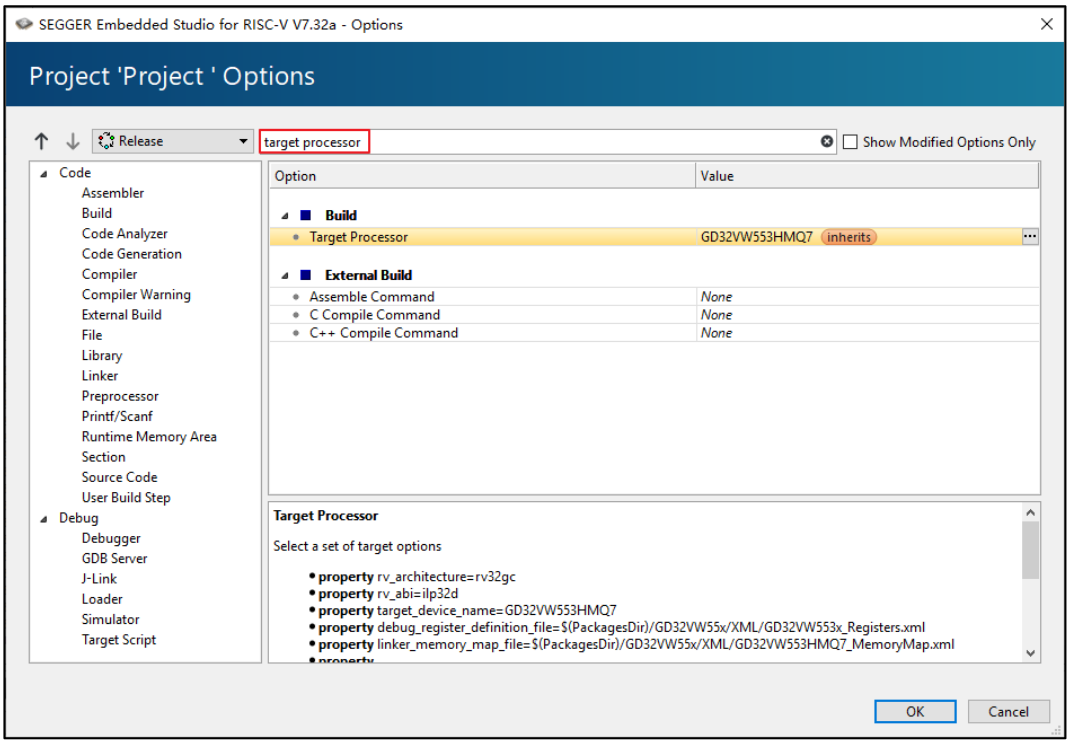
Users can right-click the Solution / Project / folder / file under the "Project Items" column and select "Options..." to set the configuration options, which refers to ***Figure 4-1. Project configuration options***.

Figure 4-1. Project configuration options



4.1.1. Chip selection

Figure 4-2.Chip selection



4.1.2. Assembler / compiler selection

Figure 4-3. Assembler selection

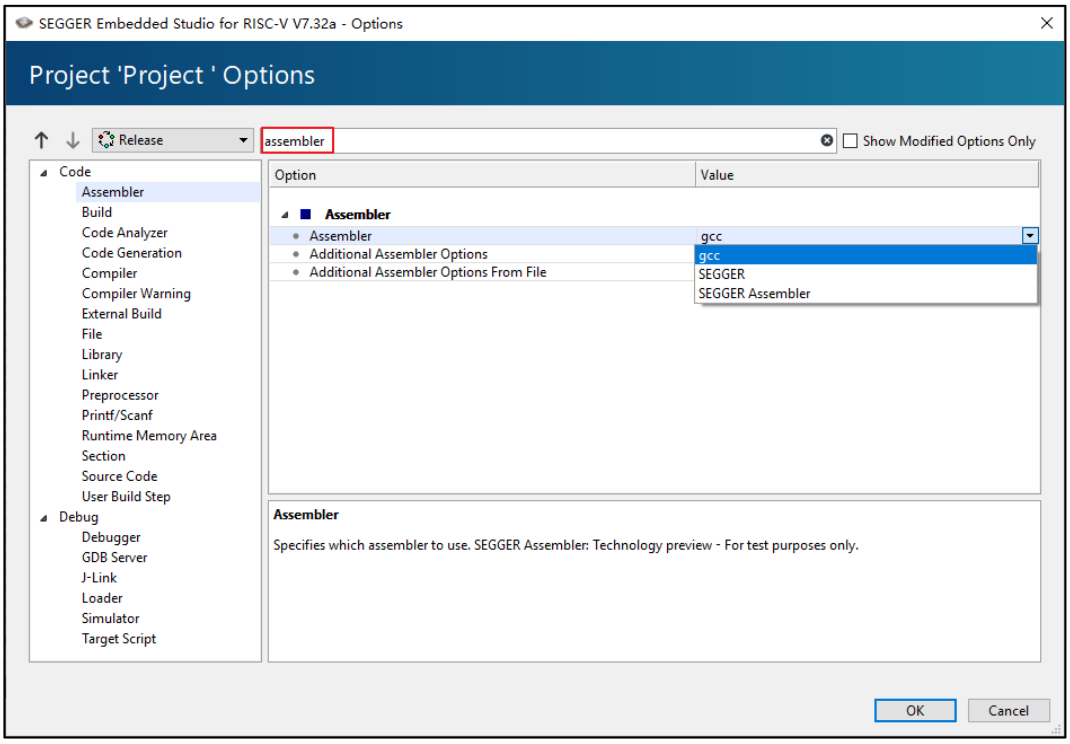
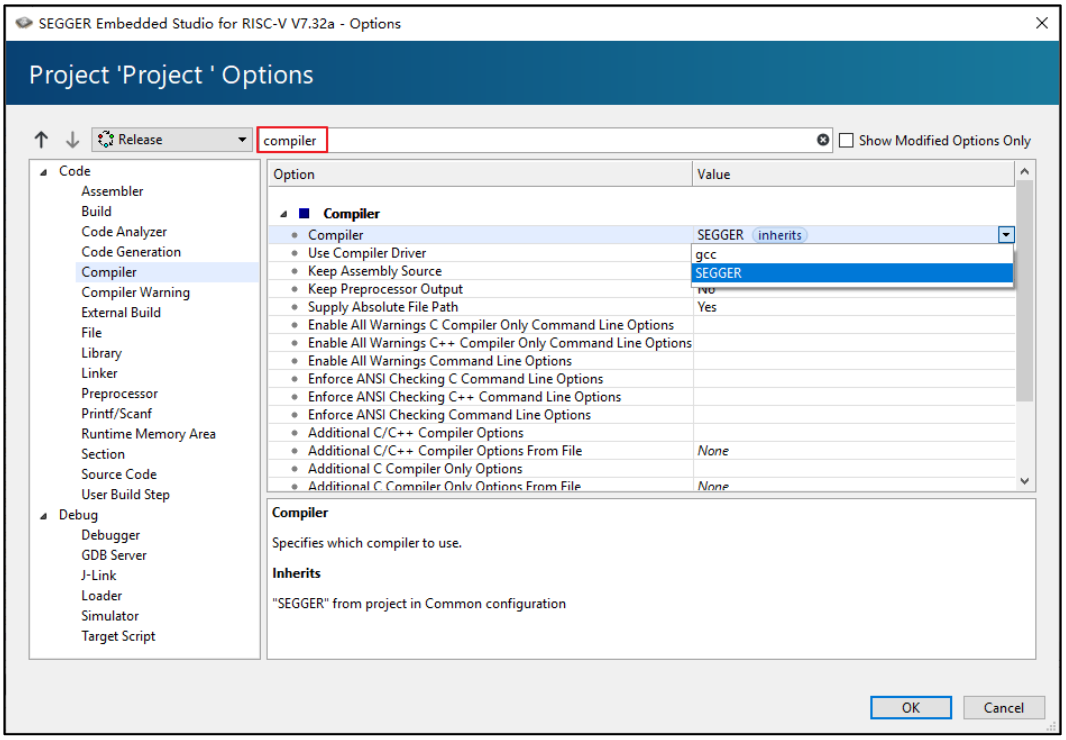
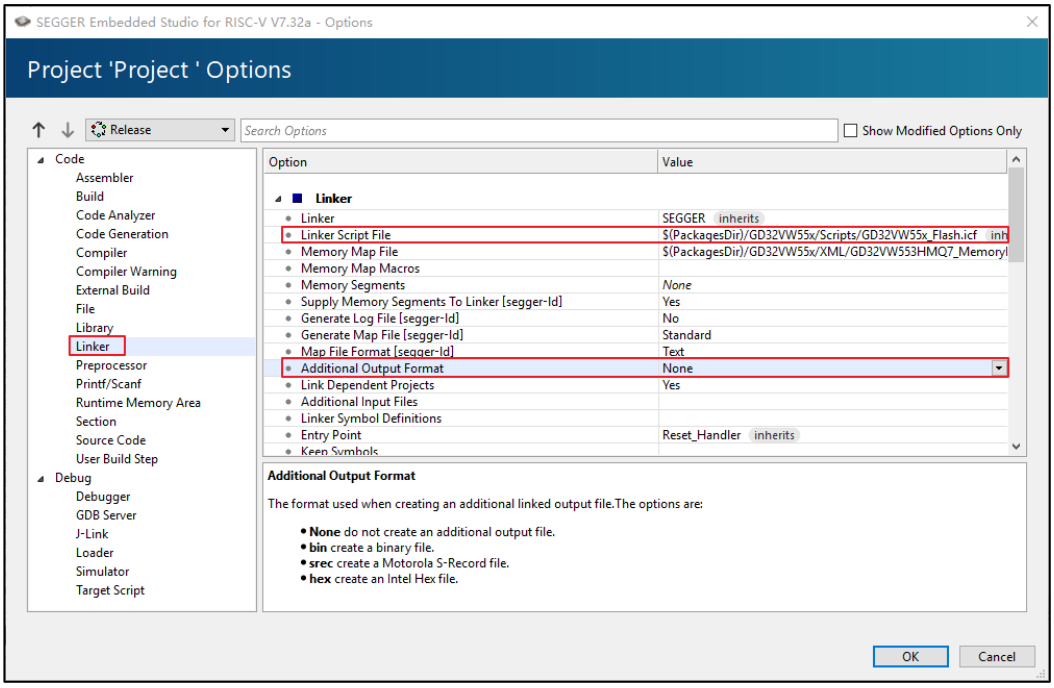


Figure 4-4. Compiler selection



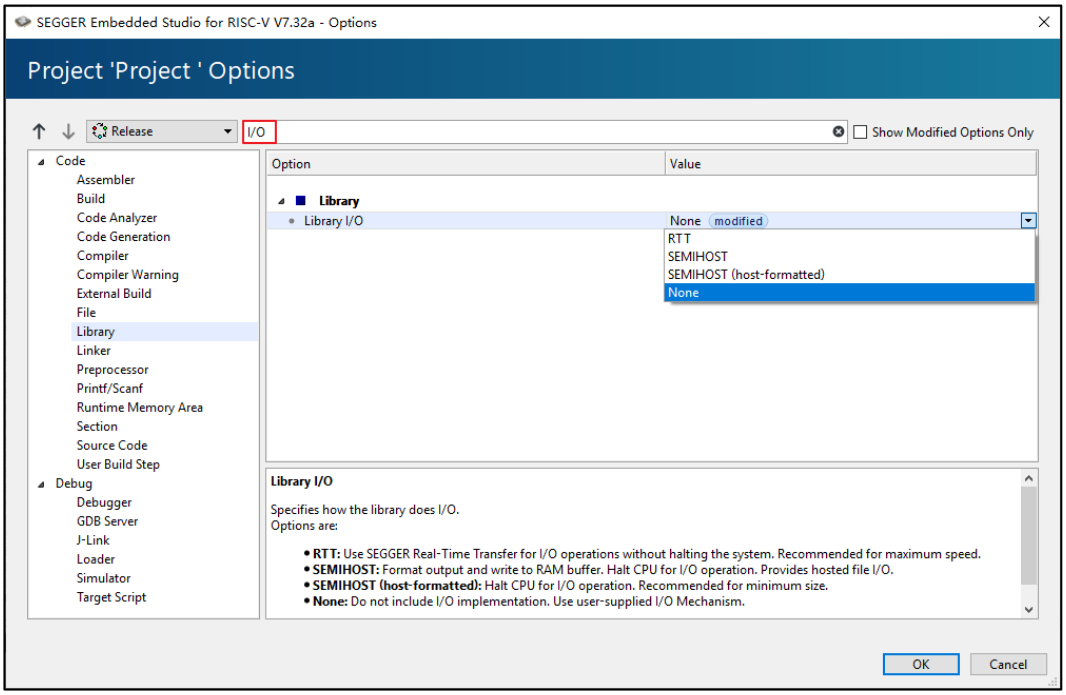
4.1.3. Link script and link output format configuration

Figure 4-5. Link script and link output format configuration



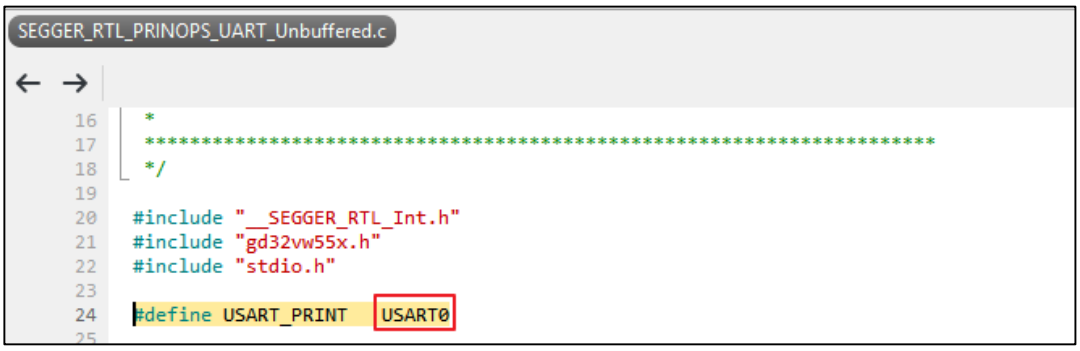
4.1.4. Input / output library configuration

Figure 4-6. I/O library configuration



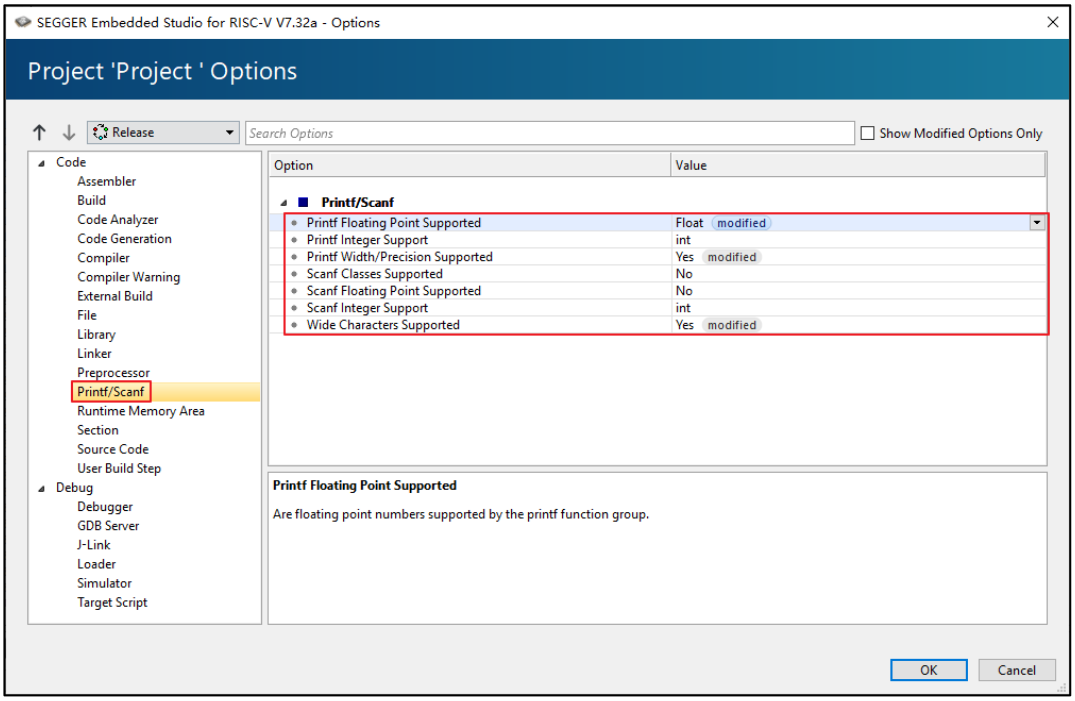
When the "None" is selected, user can specify the print serial port by modifying the macro USART_PRINT in the "SEGGER_RTL_PRINOPS_UART_Unbuffered.c " file, which refers to *Figure 4-7. Hardware USART configuration*.

Figure 4-7. Hardware USART configuration



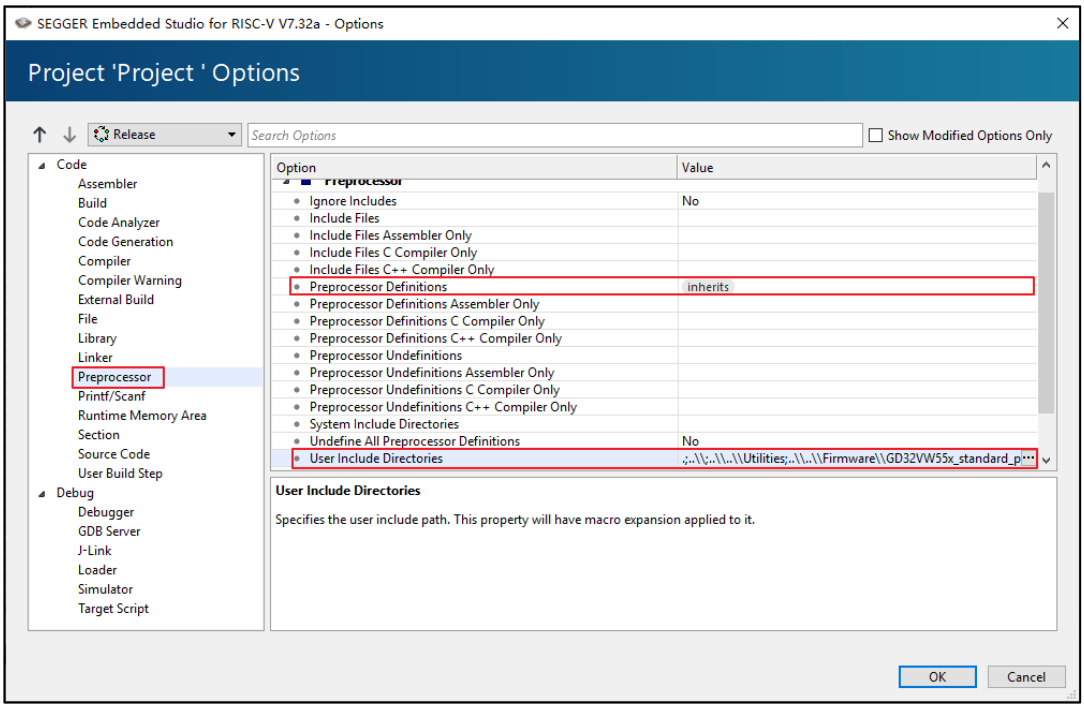
4.1.5. Input / output format support configuration

Figure 4-8. Input/output format support configuration



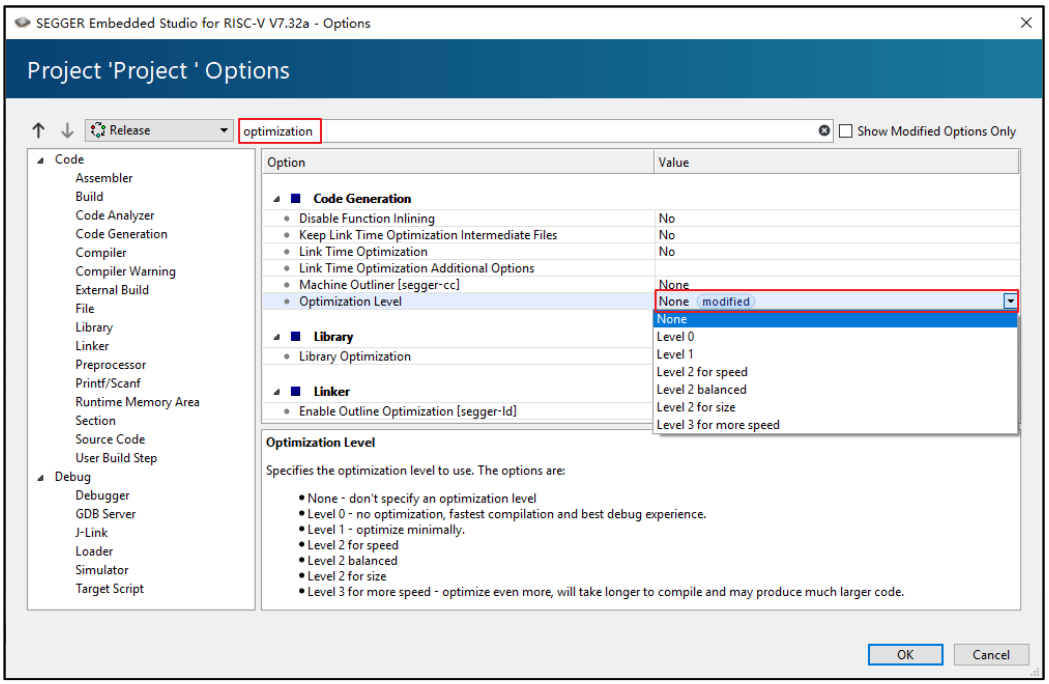
4.1.6. Preprocess configuration

Figure 4-9. Preprocess configuration



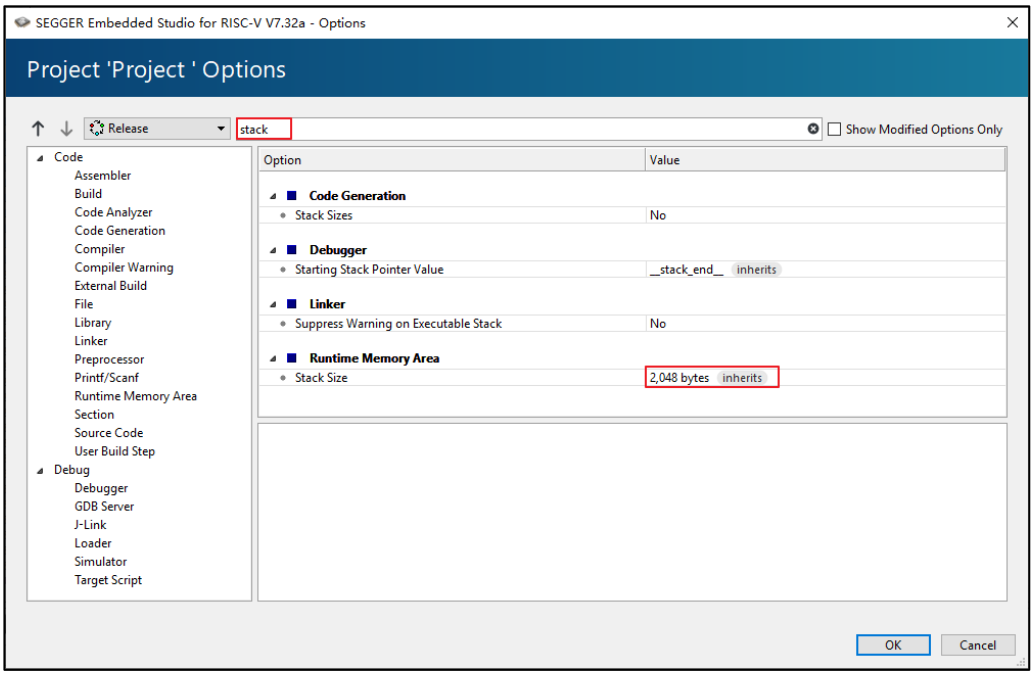
4.1.7. Optimize level configuration

Figure 4-10. Optimize level configuration



4.1.8. Stack configuration

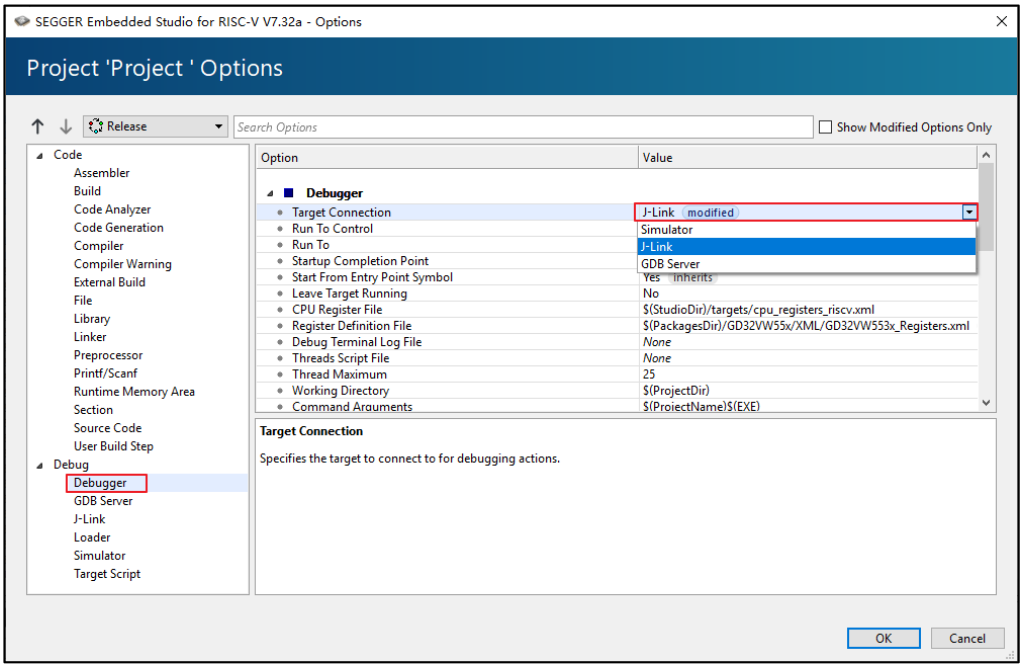
Figure 4-11. Stack configuration



4.1.9. Debugger configuration

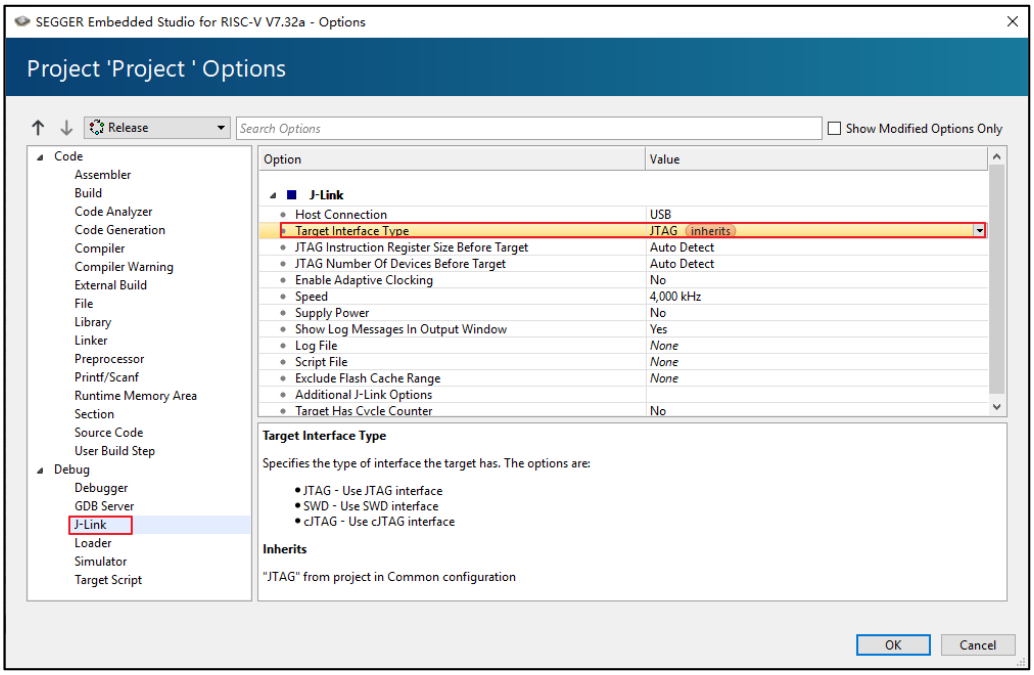
Users can choose J-Link or GDB Server to download and debug the project, which refers to *Figure 4-12. Debugger configuration*.

Figure 4-12. Debugger configuration



When choosing J-Link mode for project development, J-Link settings refers to *Figure 4-13. J-link configuration*.

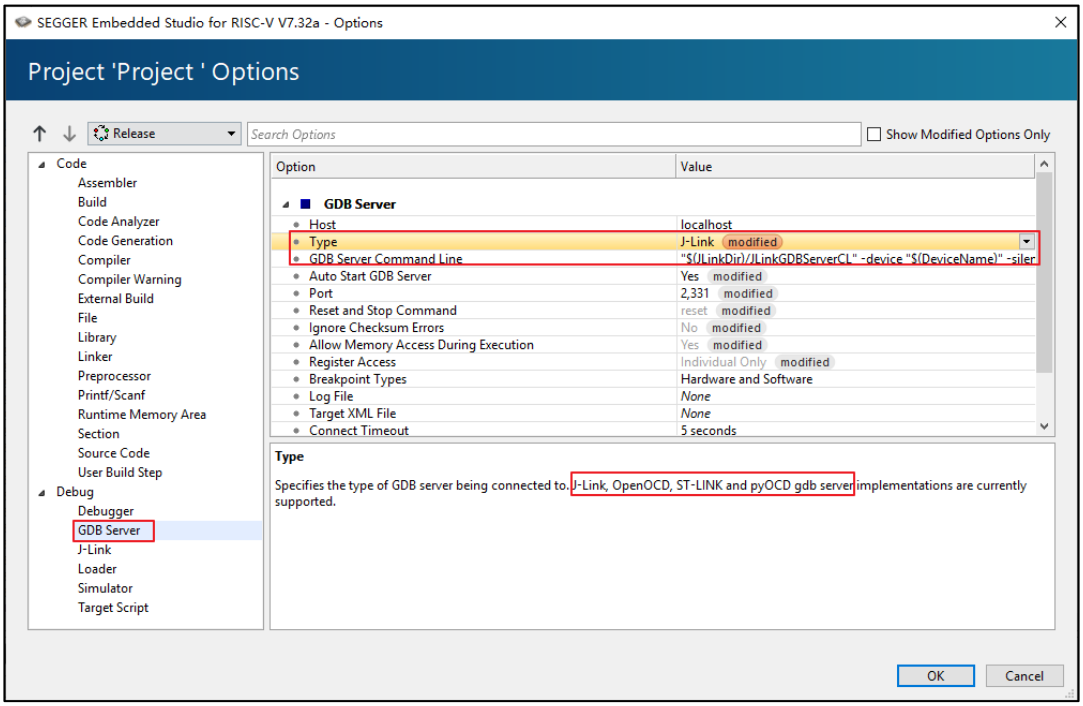
Figure 4-13. J-link configuration



When choosing the GDB Sever method for project development, select the appropriate GDB

Server according to the requirements, which refers to ***Figure 4-14. GDB server configuration***.

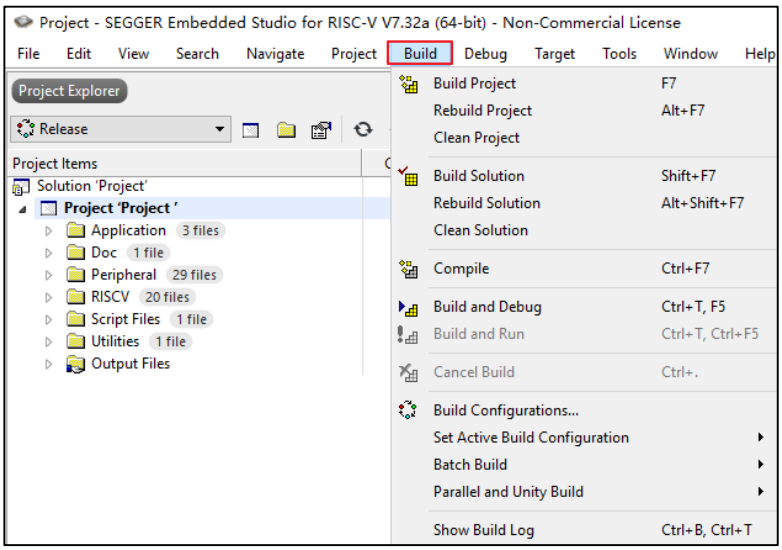
Figure 4-14. GDB server configuration



4.2. Project build options

By clicking "Build" option in the menu bar, user can clear, compile and recompile the Project / Solution; In addition, the current active project can be run or debug after compilation, which refers to ***Figure 4-15. Project build options***.

Figure 4-15. Project build options



4.3. Project Debug options

By clicking the "Debug" option in the menu bar, the target chip can be debugged, breakpoint set and other operations, which refers to ***Figure 4-16. Project debug options*** and ***Figure 4-17. Project debug interface***.

Figure 4-16. Project debug options

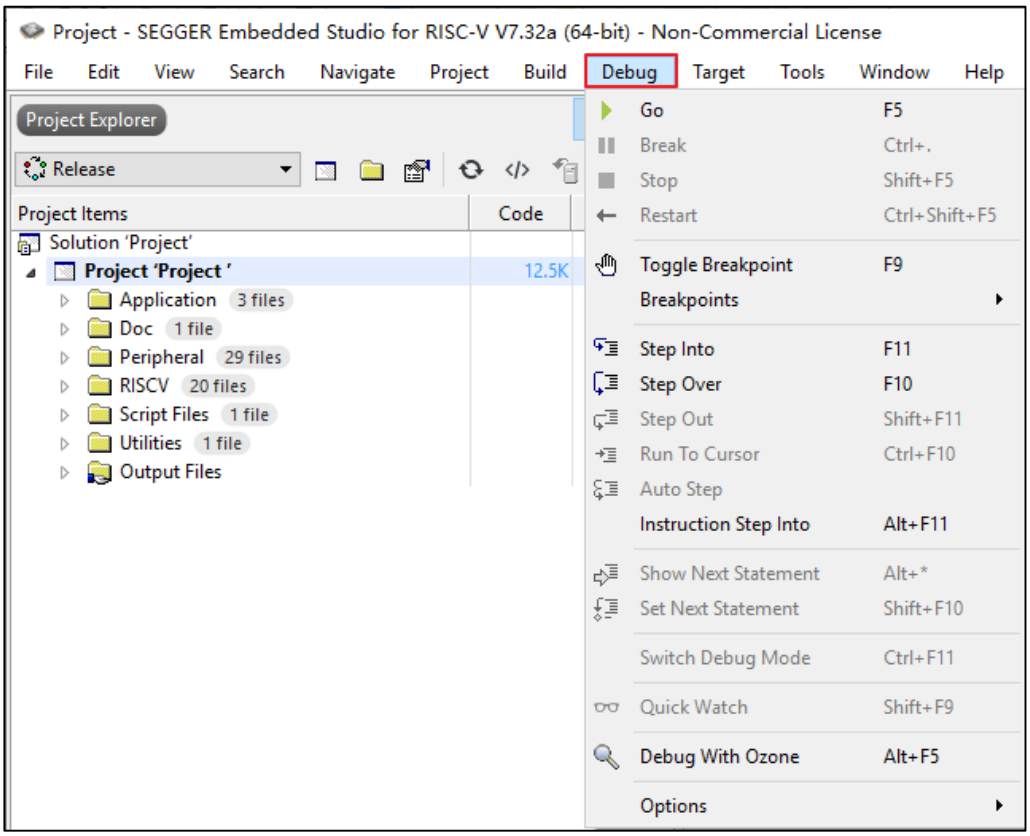
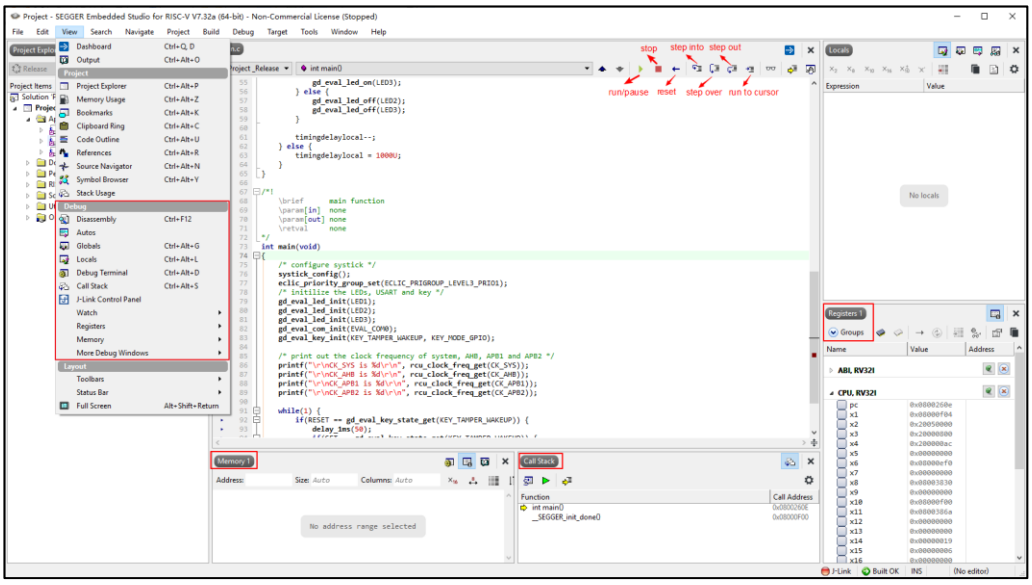


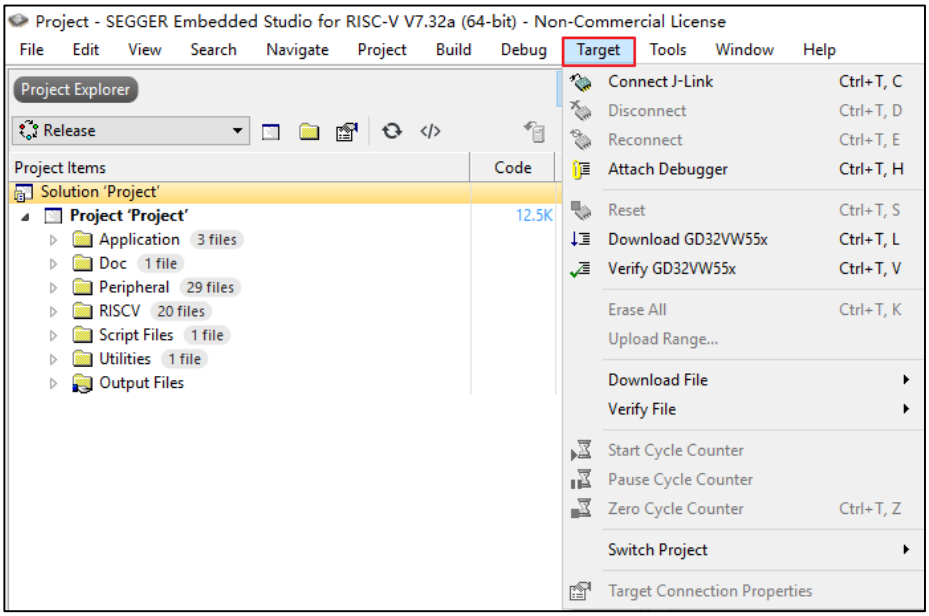
Figure 4-17. Project debug interface



4.4. Target operation options

By clicking the "Target" option in the menu bar, the operations such as connect, disconnect, attach, download and verify can be performed on the target chip, which refers to ***Figure 4-18. Target operation options.***

Figure 4-18. Target operation options



5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jan.15 2024

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