GigaDevice Semiconductor Inc.

Development Guide for GD32VW553 series MCU in SEGGER Embedded Studio IDE

Application Note AN186

Revision 1.0

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1. Introduction

The devices of GD32VW553 series MCU are 32-bit general-purpose microcontrollers based on the Nuclei N307 processor. The N307 processor is based on the RISC-V architecture instruction set.

This application note is designed to help users to build and develop GD32VW553 series MCU project in SEGGER Embedded studio for RISC-V (SES) IDE.



2. Development environment

- Evaluation board: GD32VW553H-EVAL-V1.1
- Hardware debugger: J-Link V11 / V12
- IDE: SEGGER Embedded Studio for RISC-V V7.32a
- Operating system: WIN10 64-bit OS



3. **Project development**

3.1. Device support package installation

The device support package can be installed online or offline in SES (the offline package is available from https://gd32mcu.com), which refers to *Figure 3-1. Device support package installation options*. Open SES software, online package can be installed by "Package Manager...", which refers to *Figure 3-2. Device support package installation online*; offline package can be installed by "Manually Install Packages...", which refers to *Figure 3-3. Device support package installation offline*...

Hello - SEGGER Embedded Stud	dio for RIS	.C-V V7.	.32a	(64-bit) - Non-Co	mmerci	ial Lic	ense					- C	2	\times
File Edit View Search Nav	vigate P	roject	Bui	ild Debug Ta	arget	Tools	Window Help							
Project Explorer			×	main.c	1	¢ (Options	Alt+,				•	۲	×
🗘 Debug 🔹 🗖	🗀 🗳	0	$\langle \rangle$			L	License Manager							
Project Items	Code	Data+I	RO			F	Package Manager							
Solution 'Hello'					9	9 9	Show Installed Packages		13	- ANT				
Figer Head					L	,	Manually Install Packages			ma				
a 🔄 Source 1 file, modified of						δ Ι	New File Comparison	Ctrl+K, F		•				
System 1 file						1	New Binary File Comparison							
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						7	Terminal Emulator	•	EIIIL	Jeuueu	Studio			
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						_				Today				
										🗅 Hell	0			
								Check f	or Packages					
				All pac	:kage	is ai	re up to date	Checkin	or Packages					
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				Completed	ate from	i previ	ious session							
				SEGGER Emb Completed	bedded S	Studio	o is ready to use							~
										C Direct	exected (Simulater)	INC (No edito	0	

Figure 3-1. Device support package installation options

Figure 3-2. Device support package installation online

SEGGER Embedde	d Studio for RISC-V V7.32a - Package I	Manager		?	×
G Select Packa	ages				
GD32VW55x	٢			0	¢
Title	^	Version Type	Status	Action	
GD32VW55x CPU Sup	oport Package	1.00 v CPU S	Support Installed	No Action	
Package Informa	tion				^
Description	This package contains project templa	tes and system files for the Gigal	Device GD32VW55x.		
Installed Version	1.00				
Author	SEGGER Microcontroller GmbH				~
			Back	Cance	4



Figure 3-3. Device support package installation offline



3.2. Create project based on the template

The steps to create a new project based on the template are as follows:

Step 1: Open SES software and clicking "File->New Project" option and then choose "A C/C++ executable for GigaDevice GD32VW55x" and set the project name and location to create project, which refers to *Figure 3-4.Create a project based on the template*.

Figure 3-4.Create a project based on the template

SEGGER	Embedded Studio	o for RISC-V V7.32a - New Project			×
G Sele	ect new project	t template	GD32VW55	x	0
🌵 Don't	see your device	or board? Use the <u>Package Manager</u> to install pa	ckages		
Descriptio	on		Manufacturer	Board	^
Gigo A Ari A	C/C++ executable fr n assembly code on n externally built exe library for GigaDevic	or GigaDevice GD32VW55x. y executable for GigaDevice GD32VW55x. cutable for GigaDevice GD32VW55x. e GD32VW55x.	GigaDevice GigaDevice GigaDevice GigaDevice	Generic GD32VW55x Generic GD32VW55x Generic GD32VW55x Generic GD32VW55x	~
Name:	Project				
Location:	D:\GD32VW553			Brow	vse
			1	Back Canc	cel

Step 2: Click "Next" to enter the common project setting interface, including chip selection, compiler type selection, link output format selection, predefined macro setting, header file



containing path setting, input/output support and stack size configuration, which refers to *Figure 3-5.Common project settings based on the template*.

Figure 3-5.Common project settings based on the template

Properties:		
Option	Value	
Build		
 Target Processor 	GD32VW553HMQ7	•••
Compiler		
Compiler	SEGGER	
Debugger		
 ISA Extensions Debug 	None	
Linker		
 Additional Output Format 	None	
Preprocessor		
 Preprocessor Definitions 		
 User Include Directories 		
Printf/Scanf		
 Printf Floating Point Supported 	No	
 Printf Integer Support 	int	
Printf Width/Precision Supported	No	
 Scanf Classes Supported 	No	
 Scanf Floating Point Supported 	No	
 Scanf Integer Support 	int	
Runtime Memory Area		
 Stack Size 	2,048 bytes	
T / D		
larget Processor		

Step 3: Click "Next" to enter the project files selection interface and the default selection should be used, which refers to *Figure 3-6.Project files selection based on the template*.

Figure 3-6.Project files selection based on the template

SEGGER Embedded Studio for RISC-V V7.32a - New Project		×
G Select files to add to project		
Files: Image: Source Files Image: Source Files <		
✓ Import all files and package files		
	Back Next Cance	



Step 4: Click "Next" to enter the project configurations interface, which refers to <u>Figure</u> <u>3-7.Project configurations based on the template</u>.

Figure 3-7.Project configurations based on the template

Sector Embedded Studio for NSC-V V.2.2a - New Project X Sector Configurations to add to project Sector		
Sector on figurations to add to project	SEGGER Embedded Studio for RISC-V V7.32a - New Project	×
Configurations:	Select configurations to add to project	
	Configurations:	
Back Finish Cancel	Back Finish C	ancel

Step 5: Click "Finish" to enter the project interface, users can carry out secondary development based on this template project, which refers to *Figure 3-8. New project based on the template*.



Figure 3-8. New project based on the template

Project - SEGGER Embedded Studio for RISC-V V7.3	2a (64-bit) - Non-Commercial License	- 🗆	×
File Edit View Search Navigate Project E	uild Debug Target Tools Window Help		
Project Explorer	Dashboard	Image: A state of the state	×
🕄 Debug 🔹 🕤 📄 📾 😔 🛷			^
Project Items Code Data+RO			
B Solution 'Project'			
Project 'Project'	The section		
Script Files 1 file			
Source Files 1 file, modifi			
System Files 2 files			
	SEGGER Empedded Studio		
	SEGGER Embedded Studio for BISC-V is up to date	Check for Updates	
	SEGGER Embedded Studio for RISC-V is up to date		
	All packages are up to date	Check for Packages	
			1
	Projects		
			~
	Output	Q	×
	Show: Transcript		0
	C Disconnected (LLink)	INS (No editor)	

3.3. Create project based on the standard firmware library

The steps to create a new project based on the standard firmware library are as follows:

Step 1: Open SES software and clicking "File->New Project" option and then choose "A C/C++ executable for GigaDevice GD32VW55x" and set the project name and location to create project, which refers to *Figure 3-9. Create a new project based on the standard firmware library*.

SEGGER Embedded Studio for RISC-V V7.32a - New Project			×
🕝 Select new project template	GD32VW55x		0
$\dot{\psi}$ Don't see your device or board? Use the <u>Package Manager</u> to install packages			
Description	Manufacturer	Board	^
AC/C++ executable for GigaDevice GD32VW55x An assembly code only executable for GigaDevice GD32VW55x. An externally built executable for GigaDevice GD32VW55x. A library for GigaDevice GD32VW55x.	GigaDevice GigaDevice GigaDevice GigaDevice	Generic GD32VW55x Generic GD32VW55x Generic GD32VW55x Generic GD32VW55x	
Name: Project			
Location: D:\GD32VW55x_Firmware_Library\Template\SES_project		Brow	/se
	Back	Next Canc	el

Figure 3-9. Create a new project based on the standard firmware library

Step 2: Click "Next" to enter the common project setting interface, including chip selection,



compiler type selection, link output format selection, predefined macro setting, header file containing path setting, input/output support and stack size configuration, which refers to *Figure 3-10. Common project settings based on the standard firmware library*.

Figure 3-10. Common project settings based on the standard firmware library

G Choose common project	settings	
Properties:		
Option	Value	
Build		
 Target Processor 	GD32VW553HMQ7	
Compiler		
Compiler	SEGGER	
Debugger		
 ISA Extensions Debug 	None	
Linker		
 Additional Output Format 	None	
Preprocessor		
 Preprocessor Definitions 		
 User Include Directories 		
Printf/Scanf		
 Printf Floating Point Supported 	No	
 Printf Integer Support 	int	
 Printf Width/Precision Supported 	No	
 Scanf Classes Supported 	No	
 Scanf Floating Point Supported 	No	
 Scanf Integer Support 	int	
Runtime Memory Area		
 Stack Size 	2,048 bytes	
Target Processor		
Select a set of target options		

Step 3: Click "Next" to enter the project files selection interface, uncheck all the default configuration items, which refers to *Figure 3-11. Project files selection based on the standard firmware library*.

SEGGER Embedded Studio for RISC-V V7.32a - New Project iles: Origon Device Files Script Files Source Files System Files //// The files /// The files /// The files /// The files /// The files /// The files /// The files /// The files /// The files /// The files /// The files /// The files //		ite instaty
Select files to add to project Image:	SEGGER Embedded Studio for RISC-V V7.32a - New Project	
Import all files and package files	Select files to add to project	
Import all files and package files	es:	
Comparison Source Files Source Files Source Files Import all files and package files	Device Files	
Import all files and package files	L L Script Files Surce Files	
Import all files and package files	□ □ System Files	
] Import all files and package files		
Import all files and package files		
Import all files and package files		
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Import all files and package files		
Import all files and package files		
] Import all files and package files		
Import all files and package files		
	Import all files and package files	
Back Nevt Canc	Back	Next Cancel

Figure 3-11. Project files selection based on the standard firmware library

Step 4: Click "Next" to enter the project configuration interface, which refers to <u>Figure 3-12</u>. <u>Project configurations based on the standard firmware library</u>.

Figure 3-12. Project configurations based on the standard firmware library



Step 5: Click "Finish" to enter the project interface, users can carry out secondary development based on this empty project, which refers to *Figure 3-13. Empty project*.



Figure 3-13. Empty project

project - SEGGER Embedded Studio for RISC-V V	2a (64-bit) - Non-Commercial License	- 0	×
File Edit View Search Navigate Project	uild Debug Target Tools Window Help		
Project Explorer	Dashboard	Image: A state of the state	×
🗘 Release 🔹 🗖 🛅 🔂 🔇			^
Project Items Code Data+R			
Solution 'project'			
Project project	The second se		
	v - v.		
	SECCED Emboddod Studio		
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		Check for Lindates	
	SEGGER Embedded Studio for RISC-V is up to date		
	All packages are up to date	Check for Packages	
	All packages are up to date		
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		-	
	Comput	Q	^
	Show: Transcript 🔹 🍾 Tasks 💌		\$
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projectioni roject saveu	O Disconnected (PLINK) V Built OK	(ivo cuitor)	-11

Step 6: Organize the firmware library files according to the following structure, which refers to *Figure 3-14. Project files*. The specific file structure can refer to firmware library template project.

Figure 3-14. Project files structure

He tat ver Sate Novat Project and Debug tage tool window Hep Concentrations Code Data-RO States Traject Code Data-RO States Traject Code Data-RO States Traject States Traject Code Data-RO States Traject States Traject States Traject Code Data-RO States Traject States Traject Code Data-RO States Traject States Traject Code Data-RO States Traject States Traject	Project - SEGGER Embedded Studio for RISC-V V	32a (64-bit) - Non-Commercial License	- 🗆 X
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Code Variance Subtrace Subt	Project Explorer	(main.c gdsz/w/osh_eval.c gdsz/w/osk_gpio.c	🔁 💿 👻 🗙
Project Code Data-NO Solution Flight Improved Transcript Improved Transcript Solution F	🗘 Release 🔹 🗖 📄 😭 😌		^
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system_gd32w53kc is gd52w53k_evalc SEGGER Embedded Studio for RISC-V is up to date Check for Updates Check for Updates Check for Updates Check for Packages All packages are up to date Projects Projects Projects Show: Tenscript T T T T T T T T	Peripheral 29 files Source 28 files		
Stort rie The Stort rie The South Strategy South Strategy South Str	system_gd32vw55x.c arr gd32vw55x.c arr gd32vw55x.c arr gd32vw55x.c arr gd32vw55x.c arr gd32vw55x.c arr gd32vw55x.c	SEGGER Embedded Studio for RISC-V is up to date	Check for Updates
Projects Dopen existing Create new	GO32VW55x_Target.js GO32VW55x_Target.js GO32Vw553h_eval.c	All packages are up to date	Check for Packages
Courput Show: Transcript		Projects 🕞 Open existing	
Show: Transcript		Output	x 🖾
		Show: Transcript	0
Objective and the second		🗇 Disconnected (GDB Server)	OK INS (No editor)

Step 7: Click "Project->Options" to enter project options interface and configure header file containing path, which refers to *Figure 3-15. User include directory configurations*.



Figure 3-15. User include directory configurations

SEGGER Embedded Studio for RIS	C-V V7.32a - Options		×	
Project 'Project ' Opt	ions			
↑↓ Ç Release -	user include		Show Modified Options Only]
a Code	Option	Value	^	
Assembler				SEGGER Embedded Studio for RISC-V V7.32a - Property Editor
Code Anabarr	A Code Analyzer			
Code Generation	Analyze Command	None		Cat Haar Include Directories
Compiler	4 External Build			Set User Include Directories
Compiler Warning	* Assemble Command	None		
External Build	C Compile Command	None		Project: Project
File	C++ Compile Command	None		Configuration: Release
Library				User Include Directories:
Linker	A Library			
Preprocessor	* Library I/O	None modified		
Printf/Scanf				-\
Runtime Memory Area	Instanting Disasteries	A MARKEN AND AND AND AND AND AND AND AND AND AN	WSS, standard exciptionsh Wash	\\Firmware\GD32VW55x_standard_peripheral
Section	User Include Directories	ç.\Ç.\(\(Otnides;\(\(Pirmware\(db32)	wsbx_standard_peripherat()	\\Firmware\GD32VW55x_standard_peripheral\Include
Source Code	User Include Directories C Compiler Only		~	\\Firmware\RISCV\drivers
User Build Step	Urer Include Directorier			
Debugger	User include Directories			
GDB Septer	Specifies the user include path. This property will have ma	cro expansion applied to it.		
Itlink				
Loader				[]
Simulator				Macros:
Target Script				
				OK Cancel
			OK Cancel	Specifies the user include path. This property will have macro expansion applied to it.

Step 8: Click "Project->Options" to enter project options interface and configure the script file, which refers to *Figure 3-16. Scripts configurations*.

Figure	3-16.	Scripts	configurations
--------	-------	---------	----------------

SEGGER Embedded Studio for RI	ISC-V V7.32a - Options		×		
Project 'Project ' Op	otions				
↑ ↓ 🕄 Release 🔹	Search Options		Show Modified Options Only		
▲ Code Assembler	Option	Value			
Build Code Analyzer Code Generation	Target Script Debug Begin Script Debug End Script Load Berin Script	None None None			
Compiler Warning External Build	Load End Script Reset Script Reset Script	None Reset0 modified	and SEC (D22)(WES). Tourist in the	SEGGER Embedded Studio for RISC-V V7.32a - Prop	perty Editor X
File Library Linker	• Target Script Pile		env ses/dbszvwbb largers m	Set Target Script File	
Preprocessor Printf/Scanf Runtime Memory Area Section				Project: Project Configuration: Release Target Script File:	
Source Code				.\\Firmware\RISCV\env_SES\GD32VW55x_Target.js	Browse
Debug Debugger GDB Server	Target Script File The target script file, the contents of this file are	prepended to script project properties before	they are executed.	Macros:	۲
J-Link Loader Simulator Target Script					OK Cancel
	JI		OK Cancel	The target script file, the contents of this file are prepended t before they are executed.	o script project properties



4. **IDE** interface introduction

4.1. **Project configuration options**

Users can right-click the Solution / Project / folder / file under the "Project Items" column and select "Options..." to set the configuration options, which refers to <u>Figure 4-1. Project</u> <u>configuration options</u>.



Project Stoff Enhanced Studio for REC VV238 (cH40) Nov File Site View Search Navigate Project Bould Debug Control States Project Novel Studion Project Project Novel Application States Application States	n-Commercial licence Target Tools Window Help ← → 1 /1 2 /1 2 /1 3 /1 5 /1 5 /1 1 /1 1 /1 5 /1 5 /1 1 /1	5C-V V7.32a - Options tions	×	×
A) protoc.c Doc 1166 Jordanut.t Bourd 12666 Bourd 1266 Bourd 126		Storet Option	Show Modified Options Only Value Grc Grc Nove Ves No Nove Nove Nove Nove Nove Nove Nove	
	Chappe Show	Π	OK Cince	G ×



4.1.1. Chip selection

Figure 4-2.Chip selection

SEGGER Embedded Studio for R	SC-V V7.32a - Options		
Project 'Project ' Op	tions		
↑↓ Cot Release -	target processor	Show Mor	dified Options Only
✓ Code Assembler Build	Option	Value	
Code Analyzer Code Generation Compiler	Target Processor	GD32VW553HMQ7 (inherits)	
Compiler Warning External Build File Library Linker Preprocessor Printf/Scanf Runtime Memory Area Section Source Code	Assemble Command Compile Command C++ Compile Command	None None None	
User Build Step Debug GDB Server J-Link Loader Simulator Target Script	Target Processor Select a set of target options • property rv_architecture=rv32gc • property rv_abi=ilp32d • property target_device_name=GD32V • property debug_register_definition_fil • property linker_memory_map_file=\$(W553HMQ7 le=\$(PackagesDir)/GD32VW55x/XML/GD32VW553x_Registers.xm PackagesDir)/GD32VW55x/XML/GD32VW553HMQ7_MemoryMa	l p.xml v

4.1.2. Assembler / compiler selection

Figure 4-3. Assembler selection

Project 'Project ' Op	ptions	
↑ ↓ 🕄 Release 👻	assembler	Show Modified Options Only
▲ Code Assembler Build	Option	Value
Code Analyzer	Assembler	955
Code Generation	Additional Assembler Ontions	gee
Compiler	 Additional Assembler Options From File 	SEGGER
Compiler Warning		SEGGER Assembler
External Build		
File		
Library		
Linker		
Preprocessor		
Printf/Scanf		
Runtime Memory Area		
Section		
Source Code		
Licer Build Step		
A Debug	Assembler	
Debugger		
GDB Server	Specifies which assembler to use. SEGGER Assembler: Tech	nology preview - For test purposes only.
I-Link		
Loader		
Simulator		
Target Script		



Figure 4-4. Compiler selection

roject 'Project ' O	ptions		
🔶 🎲 Release 🔹	compiler	Sho	w Modified Options On
Code	Option	Value	
Assembler			
Build	⊿ ■ Compiler		
Code Analyzer	Compiler	SEGGER (inherits)	•
Code Generation	Use Compiler Driver	gcc	
Compiler	Keep Assembly Source	SEGGER	
Compiler Warning	Keep Preprocessor Output	טאו	
External Build	 Supply Absolute File Path 	Yes	
File	 Enable All Warnings C Compiler Only Command Line Options 		
Librany	 Enable All Warnings C++ Compiler Only Command Line Option 	s	
Liplay	 Enable All Warnings Command Line Options 		
Linker	 Enforce ANSI Checking C Command Line Options 		
Preprocessor	 Enforce ANSI Checking C++ Command Line Options 		
Printf/Scanf	 Enforce ANSI Checking Command Line Options 		
Runtime Memory Area	 Additional C/C++ Compiler Options 		
Section	 Additional C/C++ Compiler Options From File 	None	
Source Code	Additional C Compiler Only Options		
User Build Step	Additional C Compiler Only Options From File	None	
ø Debug	Compiler		
Debugger GDB Server	Specifies which compiler to use.		
I-Link	Inherits		
Loader			
Simulates	"SEGGER" from project in Common configuration		
Simulator			
Target Script			

Link script and link output format configuration 4.1.3.

SEGGER Embedded Studio for RI	SC-V V7.32a - Options		×
Project 'Project ' Op	tions		
↑ ↓ tit Release -	Search Options		Show Modified Options Only
⊿ Code	Option	Value	^
Assembler Build	⊿ ■ Linker		
Code Analyzer	Linker	SEGGER inherits	
Code Generation	Linker Script File	\$(PackagesDir)/GD32VW55x/S	cripts/GD32VW55x_Flash.icf inh
Compiler	Memory Map File	<pre>\$(PackagesDir)/GD32VW55x/X</pre>	(ML/GD32VW553HMQ7_Memoryl
Compiler Warning	Memory Map Macros		
External Build	Memory Segments Second Memory Segments	None	
File	Supply Memory Segments To Linker [segger-td] Generate Leg File [segger-td]	Yes	
Library	Generate Log File [segger-ld] Generate Man File [segger-ld]	IND Standard	
Linker	Man File Format [segger-Id]	Text	
Preprocessor	Additional Output Format	None	T
Printf/Scanf	Link Dependent Projects	Yes	
Runtime Memory Area	Additional Input Files		
Section	Linker Symbol Definitions		
Source Code	Entry Point	Reset_Handler inherits	
User Build Step	Keen Symbols		~
a Debug	Additional Output Format		
Debugger GDB Server	The format used when creating an additional linked output file	.The options are:	
J-Link	 None do not create an additional output file. 		
Loader	• bin create a binary file.		
Simulator	 srec create a motorola S-Record file. her create an Intel Her file. 		
Target Script	· nex create an internex file.		
· · ·] [
			OK Cancel

Figure 4-5. Link script and link output format configuration



4.1.4. Input / output library configuration

Figure 4-6. I/O library configuration

SEGGER Embedded Studio for RISC-	V V7.32a - Options			×
Project 'Project ' Opti	ons			
↑ ↓ Trelease V	0		Show Modified Option	s Only
⊿ Code	Option	Value		
Assembler				
Code Applyger				
Code Generation	Library I/O	None (modified)		-
Compiler		SEMIHOST		
Compiler Warning		SEMIHOST (host-formatted)	
External Build		None		
File				
Library				
Linker				
Preprocessor				
Printf/Scanf				
Runtime Memory Area				
Section				
Source Code				
oser build Step	Library I/O			^
Debugger				
GDB Server	Specifies how the library does I/O.			
J-Link	options are:			
Loader	RTT: Use SEGGER Real-Time Transfer for I/O operations without	ut halting the system. Recomr	mended for maximum speed.	
Simulator	 SEMIHOSI: Format output and write to RAM buffer. Halt CPU SEMIHOST (bost-formatted): Halt CPU for I/O operation. Rec 	for I/O operation. Provides he	osted file I/O.	
Target Script	None: Do not include I/O implementation. Use user-supplied	I/O Mechanism.	L.	
				~
			ОК С	ancel

When the "None" is selected, user can specify the print serial port by modifying the macro USART_PRINT in the "SEGGER_RTL_PRINOPS_UART_Unbuffered.c " file, which refers to *Figure 4-7. Hardware USART configuration*.

Figure 4-7. Hardware USART configuration

SEGG	SEGGER_RTL_PRINOPS_UART_Unbuffered.c					
←	→					
	16	*				
	17	***************************************				
	18	_ */				
	19					
	20	<pre>#include "SEGGER_RTL_Int.h"</pre>				
	21	<pre>#include "gd32vw55x.h"</pre>				
	22	#include "stdio.h"				
	23					
	24	#define USART_PRINT USART0				
	25					



4.1.5. Input / output format support configuration

Figure 4-8. Input/output format support configuration

SEGGER Embedded Studio for RISC	-V V7.32a - Options		×
Project 'Project ' Opt	ons		
Project Project Opt	Onions Option Image: Printf Floating Point Supported Printf Floating Point Supported Scanf Classes Supported Scanf Integer Support Scanf Integer Support Vide Characters Supported Scanf Integer Supported Printf Floating Point Supported	Value Float (modified) int Yes (modified) No No int Yes (modified)	Show Modified Options Only
Debugger GDB Server J-Link Loader Simulator Target Script	Are floating point numbers supported by the printf fun	ction group.	
			OK Cancel

4.1.6. **Preprocess configuration**

Figure 4-9. Preprocess configuration

🗘 🕄 Release 🗸 🗸	Search Options		Show Modified Options Or
Code	Option	Value	
Build Gode Analyzer Code Generation Compiler Compiler Warning External Build File Library Linker Preprocessor Printf/Scanf Runtime Memory Area Section Source Code	Ignore Includes Include Files Assembler Only Include Files C Compiler Only Include Files C++ Compiler Only Include Files C++ Compiler Only Preprocessor Definitions Assembler Only Preprocessor Definitions C Compiler Only Preprocessor Definitions Assembler Only Preprocessor Undefinitions Compiler Only Preprocessor Undefinitions C Compiler Only System Include Directories Undefine All Preprocessor Definitions User Include Directories	No inherits No ¢.\\;\\.\Utilities;\\Firmv	vare\\GD32VW55x_standard_p ^{ive}
User Build Step Debugger GDB Server J-Link Loader Simulator Target Script	User Include Directories Specifies the user include path. This property will have macro e	xpansion applied to it.	



4.1.7. Optimize level configuration

Figure 4-10. Optimize level configuration

r ↓ t _o r Release ▼	optimization	Show Modified Options C			
⊿ Code	Option	Value			
Assembler					
Build	Code Generation				
Code Analyzer	 Disable Function Inlining 	No			
Code Generation	 Keep Link Time Optimization Intermediate Files 	No			
Compiler	 Link Time Optimization 	No			
Compiler Warning	Link Time Optimization Additional Options				
External Build	Machine Outliner [segger-cc]	None			
File	Optimization Level	None (modified)			
Library		None			
Linker	▲ Library	Level U			
Preprocessor	Library Optimization	Level 1			
Printf/Scanf		Level 2 holes and			
Runtime Memory Area	4 Linker	Level 2 balanced			
Section	 Enable Outline Optimization [segger-Id] 	Level 2 for size			
Source Code	Ontimization Lovel	Level 3 for more speed			
User Build Sten	Optimization Level				
 Debug 	Specifies the optimization level to use. The options are:				
Debugger					
GDP Server	 None - don't specify an optimization level Level 0 - no optimization fastest compilation and hest 	None - don't specify an optimization level			
Liek	Level 1 - ontimize minimally.	Level 0 - no optimization, tastest compilation and best debug experience. Level 1 - ortimize minimally:			
J LINK	Level 2 for speed				
Loader	Level 2 balanced				
Simulator	Level 2 for size				
Target Script	 Level 3 for more speed - optimize even more, will take 	longer to compile and may produce much larger code.			

4.1.8. Stack configuration

Figure 4-11. Stack configuration

SEGGER Embedded Studio for RISC	-V V7.32a - Options		×			
Project 'Project ' Options						
↑ ↓ 🕄 Release 🔹 st	ack	Show Modified Op	tions Only			
▲ Code Assembler	Option	Value				
Build Code Analyzer Code Generation	Code Generation Stack Sizes	No	_			
Compiler Compiler Warning External Build	Debugger Starting Stack Pointer Value	_stack_end_ inherits	_			
File Library	Linker Suppress Warning on Executable Stack	No				
Linker Preprocessor Printf/Scanf		2,048 bytes inherits	_			
Runtime Memory Area Section						
User Build Step						
Debugger GDB Server						
Loader Simulator						
Target Script						
		ОК	Cancel			



4.1.9. **Debugger configuration**

Users can choose J-Link or GDB Server to download and debug the project, which refers to Figure 4-12. Debugger configuration.

Figure 4-12. Debugger configuration

SEGGER Embedded Studio for RISC-V V7.32a - Options X						
Project 'Project ' Options						
↑ ↓ 🕄 Release 👻	Search Options		Show Modified Options Only			
⊿ Code	Option	Value	^			
Assembler Build	⊿ ■ Debugger					
Code Analyzer	Target Connection	J-Link (modified)	•			
Code Generation	 Run To Control 	Simulator				
Compiler	Run To	J-Link				
Compiler Warning	 Startup Completion Point 	GDB Server				
External Build	Start From Entry Point Symbol	Yes inherits				
File	Leave Target Running	No				
Library	CPU Register File	\$(StudioDir)/targets/cpu_regist	ters_riscv.xml			
Linker	Register Definition File	\$(PackagesDir)/GD32VW55x/XI	ML/GD32VW553x_Registers.xml			
Preprocessor	Debug Terminal Log File Threads Covint File	None				
Printf/Scanf	Thread Maximum	25				
Runtime Memory Area	Working Directory	S(ProjectDir)				
Section	Command Arguments	S(ProjectName)S(EXE)	×			
Section Sector		Sin foreca tame, steres				
Source Code	Target Connection					
User Build Step	Specifies the target to connect to for debugging actio	ins.				
⊿ Debug						
Debugger						
GDB Server						
J-Link						
Loader						
Simulator						
Target Script						
			UK Cancel .:			

When choosing J-Link mode for project development, J-Link settings refers to Figure 4-13. J-link configuration.

Figure 4-13. J-link configuration

roject 'Project ' Oj	ptions		
🔶 🛟 Release 👻	Search Options		Show Modified Options O
Code	Option	Value	
Assembler			
Build	🔺 🔳 J-Link		
Code Analyzer	Host Connection	USB	
Code Generation	 Target Interface Type 	JTAG (inherits)	-
Compiler	 JTAG Instruction Register Size Before Target 	Auto Detect	
Compiler Warning	 JTAG Number Of Devices Before Target 	Auto Detect	
External Build	 Enable Adaptive Clocking 	No	
File	Speed	4,000 kHz	
Librany	Supply Power	No	
Linker	 Show Log Messages In Output Window 	Yes	
Linker	Log File	None	
Preprocessor	Script File	None	
Printf/Scanf	Exclude Flash Cache Range	None	
Runtime Memory Area	Additional J-Link Options		
Section	Target Has Cycle Counter	No	
Source Code	Target Interface Type		
User Build Step			
Debug	Specifies the type of interface the target has. The options are		
Debugger	ITAG - Use ITAG interface		
GDB Server	SWD - Use SWD interface		
J-Link	 cJTAG - Use cJTAG interface 		
Loader			
Simulator	Inherits		
Target Script	"JTAG" from project in Common configuration		
rarger script			

When choosing the GDB Sever method for project development, select the appropriate GDB



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Server according to the requirements, which refers to *Figure 4-14. GDB server configuration*.

Figure 4-14. GDB server configuration

🗼 🕄 Release 👻	Search Options	Show Mo	dified Options
Code	Option	Value	
Assembler			
Code Analyzer	a Hest	le colle oct	
Code Generation	• Host	la link modified	
Compiler	GDB Server Command Line	"\$(II inkDir)/II inkGDBSenverCl "-device "\$(Dev	viceName)" -sil
Compiler Warping	Auto Start GDB Server	Ves modified	riseriariter an
Compiler Warning	Port	2.331 modified	
External Build	Reset and Stop Command	reset modified	
File	Ignore Checksum Errors	No modified	
Library	 Allow Memory Access During Execution 	Yes modified	
Linker	Register Access	Individual Only modified	
Preprocessor	Breakpoint Types	Hardware and Software	
Printf/Scanf	Log File	None	
Runtime Memory Area	Target XML File	None	
Section	Connect Timeout	5 seconds	
User Build Step Debug Debugger GOB Server J-Link Loader Simulator	Specifies the type of GDB server being connected to. U-Link	OpenOCD, ST-LINK and pyOCD gdb server implementatio	ins are currently

4.2. Project build options

By clicking "Build" option in the menu bar, user can clear, compile and recompile the Project / Solution; In addition, the current active project can be run or debug after compilation, which refers to *Figure 4-15. Project build options*.

Figure 4-15. Project build options





4.3. **Project Debug options**

By clicking the "Debug" option in the menu bar, the target chip can be debugged, breakpoint set and other operations, which refers to <u>*Figure 4-16. Project debug options*</u> and <u>*Figure 4-17. Project debug interface*</u>.

Figure 4-16. Project debug options

In Project - SEGGER Embedded Studio for RISC-V V7.32a (64-bit) - Non-Commercial License								
File Edit View Search	Navigate	Project	Build	Del	oug Target	Tools	Window	Help
Project Explorer					Go		F5	
	1			н.	Break		Ctrl+.	
₹ ₀ 2 Release 🔹		0 P	*		Stop		Shift+F5	5
Project Items			Code	+	Restart		Ctrl+Shi	ft+F5
Solution 'Project'			12.54	μħ,	Toggle Breakpo	oint	F9	
 Project Project Application 3 files 			12.JK		Breakpoints			•
Doc 1 file				φ _Ξ	Step Into		F11	
RISCV 20 files				Ç⊒	Step Over		F10	
Script Files 1 file				ςΞ	Step Out		Shift+F1	1
Utilities 1 file				÷ <u>≡</u>	Run To Cursor		Ctrl+F10)
				気画	Auto Step			
					Instruction Step	o Into	Alt+F11	
				₀≣	Show Next Stat	ement	Alt+*	
				ŶĒ	Set Next Statem	nent	Shift+F1	0
					Switch Debug N	Vlode	Ctrl+F11	I
				00	Quick Watch		Shift+F9)
				R	Debug With Oz	one	Alt+F5	
					Options			+

Figure 4-17. Project debug interface





4.4. Target operation options

By clicking the "Target" option in the menu bar, the operations such as connect, disconnect, attach, download and verify can be performed on the target chip, which refers to <u>*Figure 4-18.</u>* <u>*Target operation options.*</u></u>

Figure 4-18. Target operation options

🛩 Project - SEGGEK Embedded Studio for RISC-V V7.32a (64-bit) - Non-Commercial License									
File Edit View Search Navigate Project Build	d Debug	Target Tools Window Hel	р						
Project Explorer		🍫 Connect J-Link	Ctrl+T, C						
		Disconnect	Ctrl+T, D						
t Release ▼ □ 🖬 🔂	*8	🎨 Reconnect	Ctrl+T, E						
Project Items	Code	jj≣ Attach Debugger	Ctrl+T, H						
Solution 'Project'	10.5%	Reset	Ctrl+T_S						
Project Project Application 3 files	12.3K	1 Download GD32VW55x	Ctrl+T I						
Doc 1 file		∠≣ Verify GD32VW55x	Ctrl+T V						
Peripheral 29 files		•							
RISCV 20 files		Erase All	Ctrl+T, K						
Script Files 1 file		Upload Range							
Output Files		Download File	•						
		Verify File	+						
		Start Cycle Counter							
		Pause Cycle Counter							
		Zero Cycle Counter	Ctrl+T, Z						
		Switch Project	•						
		Target Connection Properties							



5. **Revision history**

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jan.15 2024

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