GigaDevice Semiconductor Inc.

在 SEGGER Embedded Studio IDE 中开发 GD32VW553 系列 MCU

应用笔记

AN186

1.0 版本

（2024 年 1 月）

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1. 前言

GD32VW553 系列 MCU 是基于 Nuclei N307 处理器的 32 位通用微控制器，其中 N307 处理器基于 RISC-V 架构指令集。

本应用笔记旨在帮助用户通过 SEGGER Embedded Studio for RISC-V（SES）IDE 进行基于 GD32VW553 系列 MCU 的软件工程构建和开发。

2. 开发环境

- 开发板：GD32VW553H-EVAL-V1.1
- 硬件调试器：J-Link V11 / V12
- IDE：SEGGER Embedded Studio for RISC-V V7.32a
- 操作系统：WIN10 64-bit OS

3. 工程开发

3.1. 设备支持包安装

可通过 SES 实现设备支持包的在线或离线安装（离线包可通过 https://gd32mcu.com 官网获取），参考*图 3-1. 设备支持包安装选项*。打开 SES 软件，通过“Package Manager...”可进行在线包安装，参考*图 3-2. 设备支持包在线安装*；通过“Manually Install Packages...”选择离线包进行安装，参考*图 3-3. 设备支持包离线安装*。

图 3-1.设备支持包安装选项

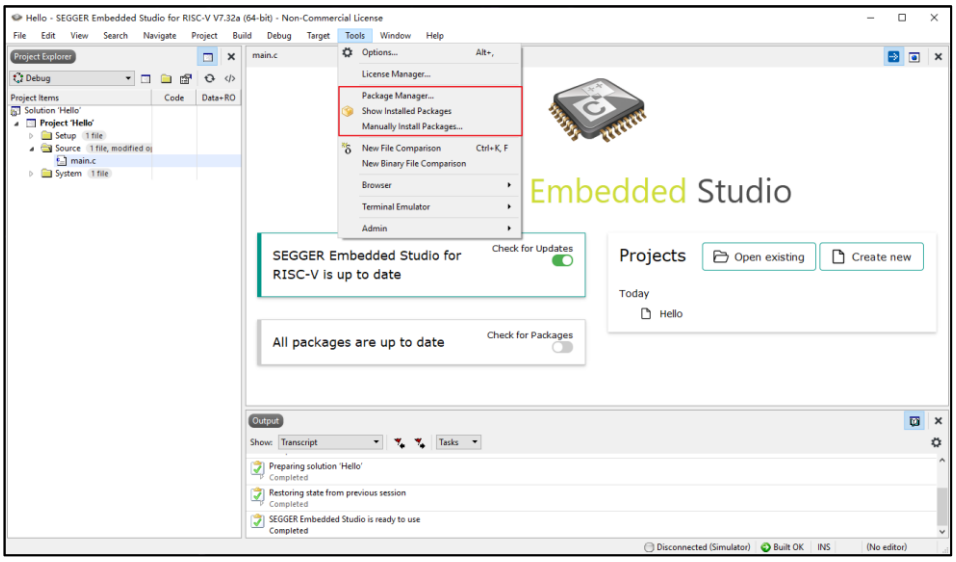


图 3-2.设备支持包在线安装

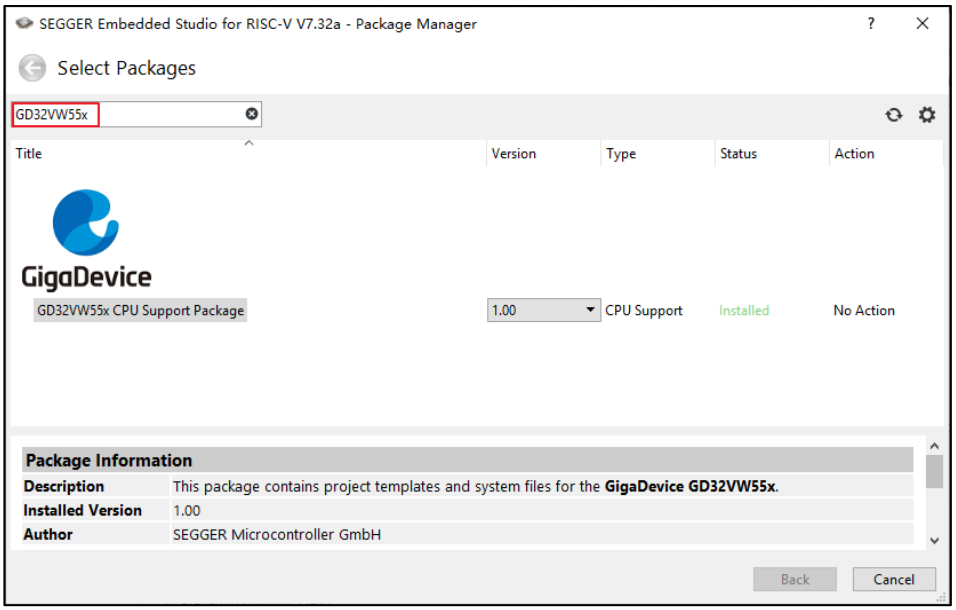
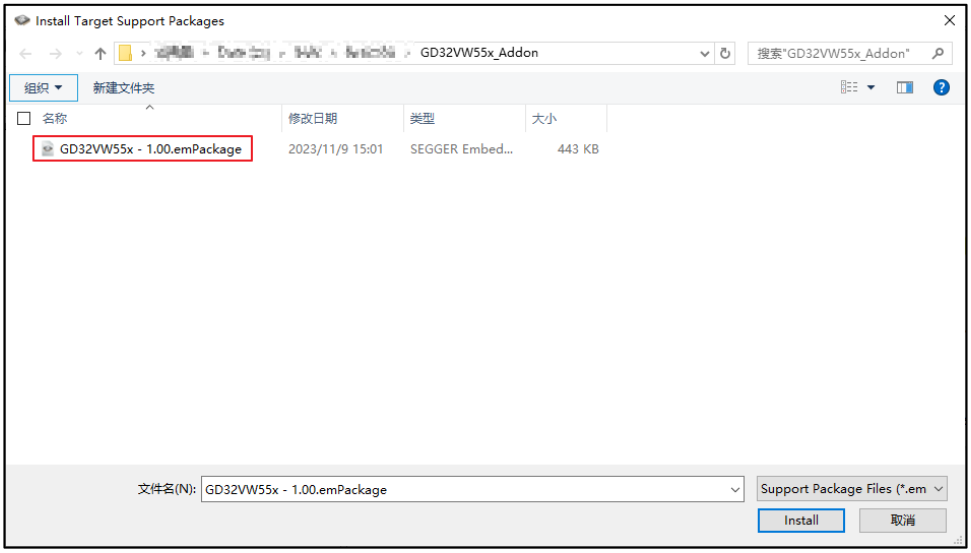


图 3-3.设备支持包离线安装

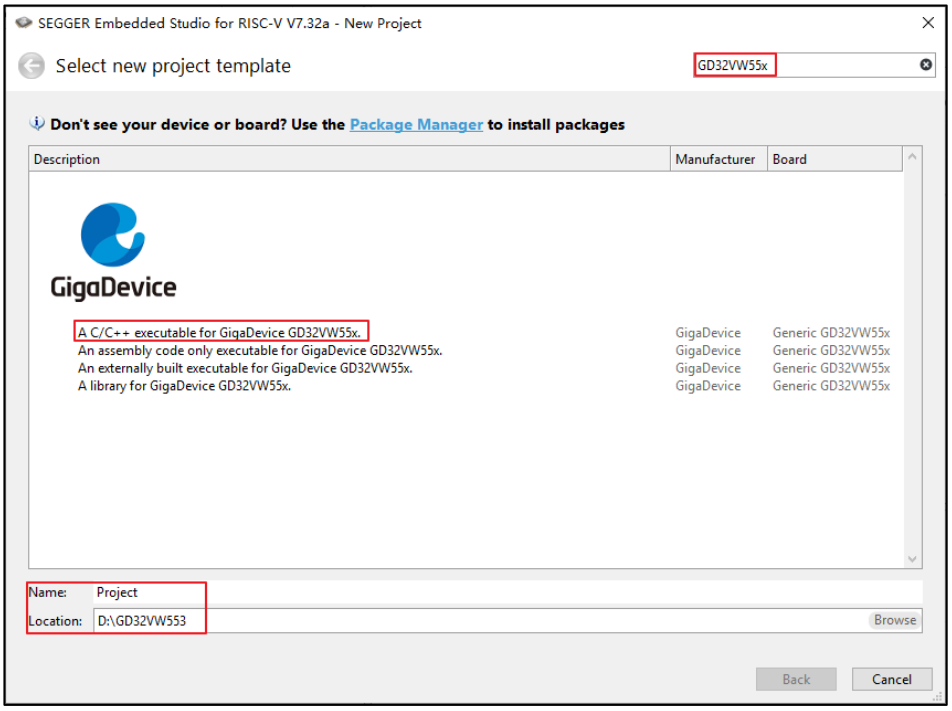


3.2. 基于模板新建工程

基于模板新建工程步骤如下：

步骤 1：打开 SES 软件，在“File->New Project”下通过选择“A C/C++ executable for GigaDevice GD32VW55x”并设置工程名和位置来新建工程，参考*图 3-4. 基于模板新建工程*。

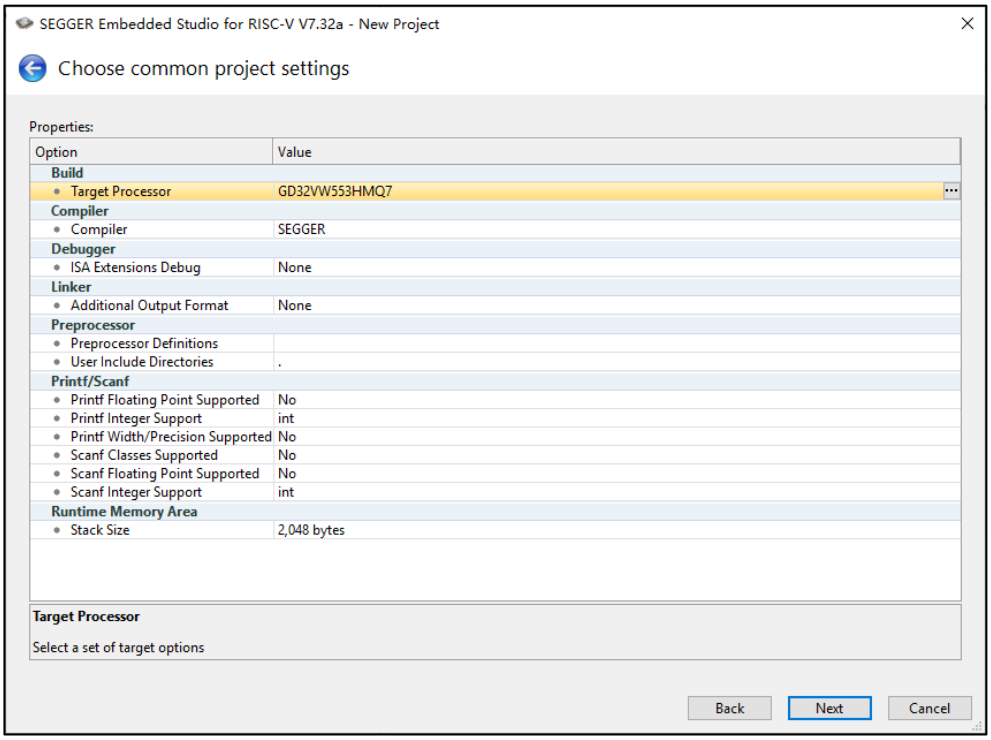
图 3-4. 基于模板新建工程



步骤 2：点击“Next”，进入通用工程设置界面，包括芯片选型，编译器类型选择，链接输出文件类型选择，预定义宏设置，头文件包含路径设置，输入/输出支持选择，栈大小配置，参考*图*

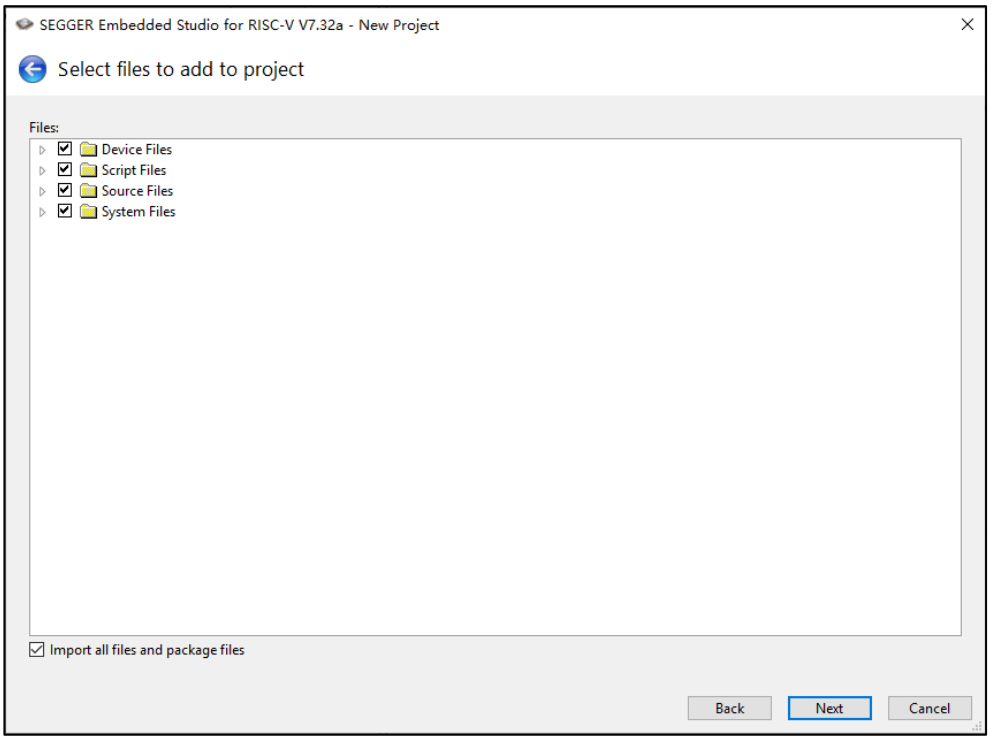
3-5. 基于模板的通用工程设置。

图 3-5. 基于模板的通用工程设置



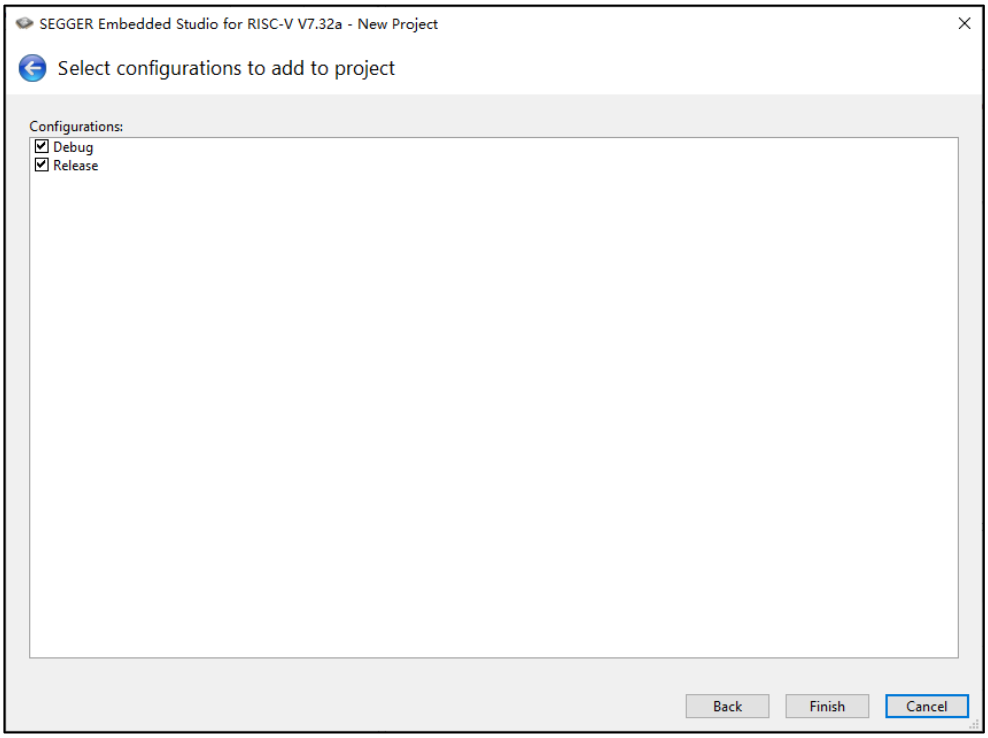
步骤 3：点击“Next”，进入工程文件选择界面，需使用默认选择项，参考*图 3-6. 基于模板的工程文件选择*。

图 3-6. 基于模板的工程文件选择



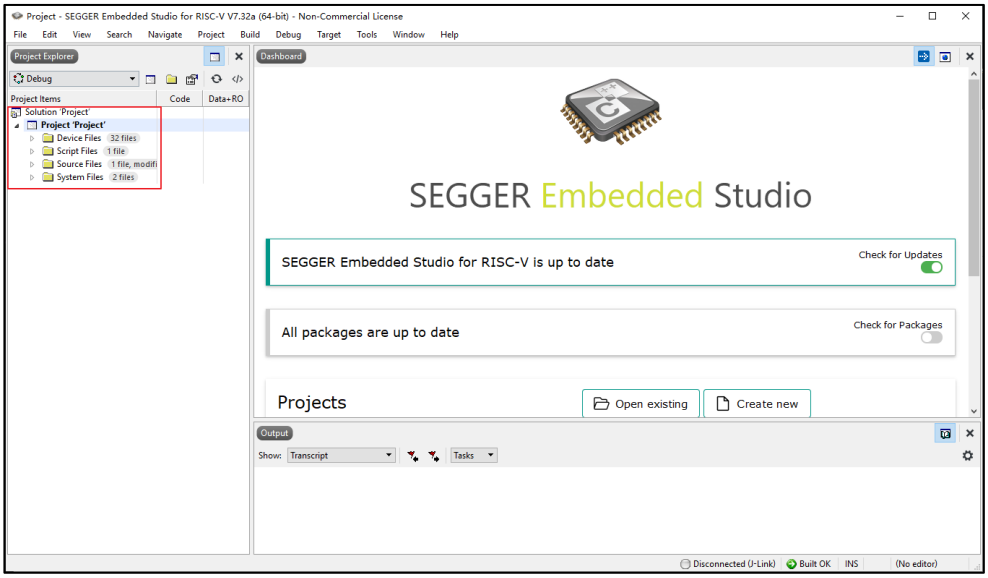
步骤 4：点击“Next”，进入工程配置选择界面，参考*图 3-7. 基于模板的工程配置*。

图 3-7. 基于模板的工程配置



步骤 5：点击“Finish”，进入工程界面，用户可以基于此模板工程进行二次开发，参考*图 3-8. 基于模板的新工程*。

图 3-8. 基于模板的新工程

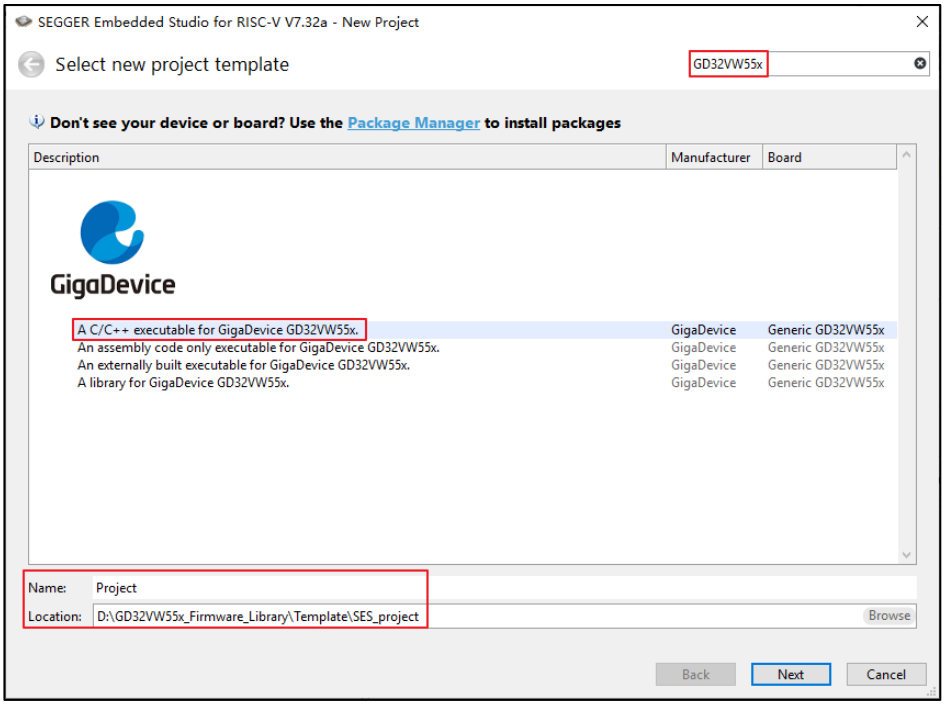


3.3. 基于标准固件库新建工程

基于标准固件库新建工程步骤如下：

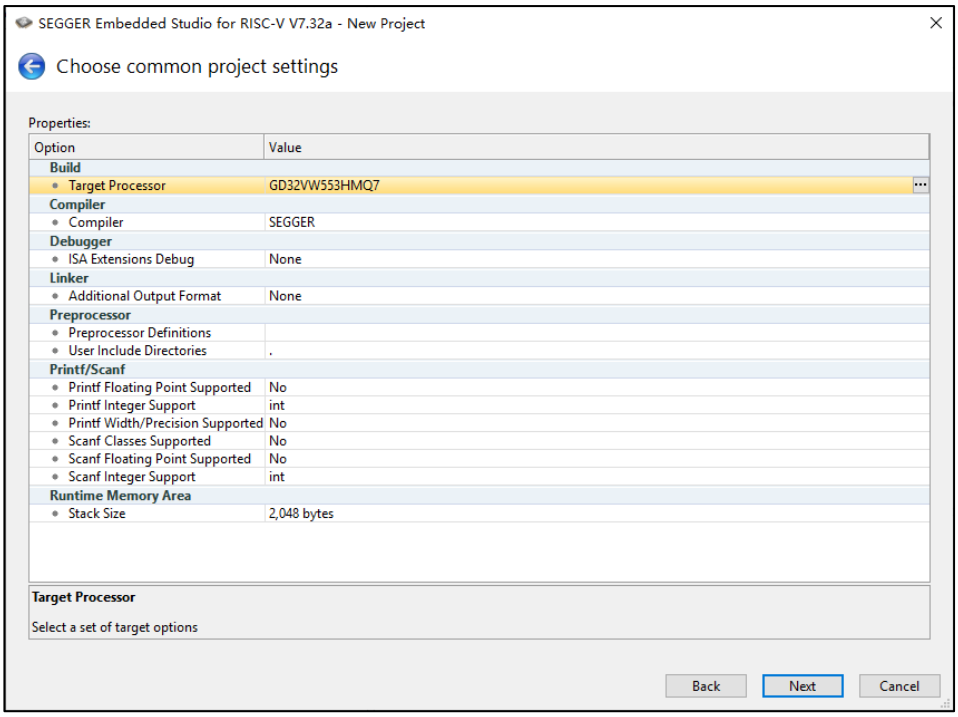
步骤 1：打开 SES 软件，在“File->New Project”下通过选择“A C/C++ executable for GigaDevice GD32VW55x”并设置工程名和位置来新建工程，参考*图 3-9. 基于标准固件库新建工程*。

图 3-9. 基于标准固件库新建工程



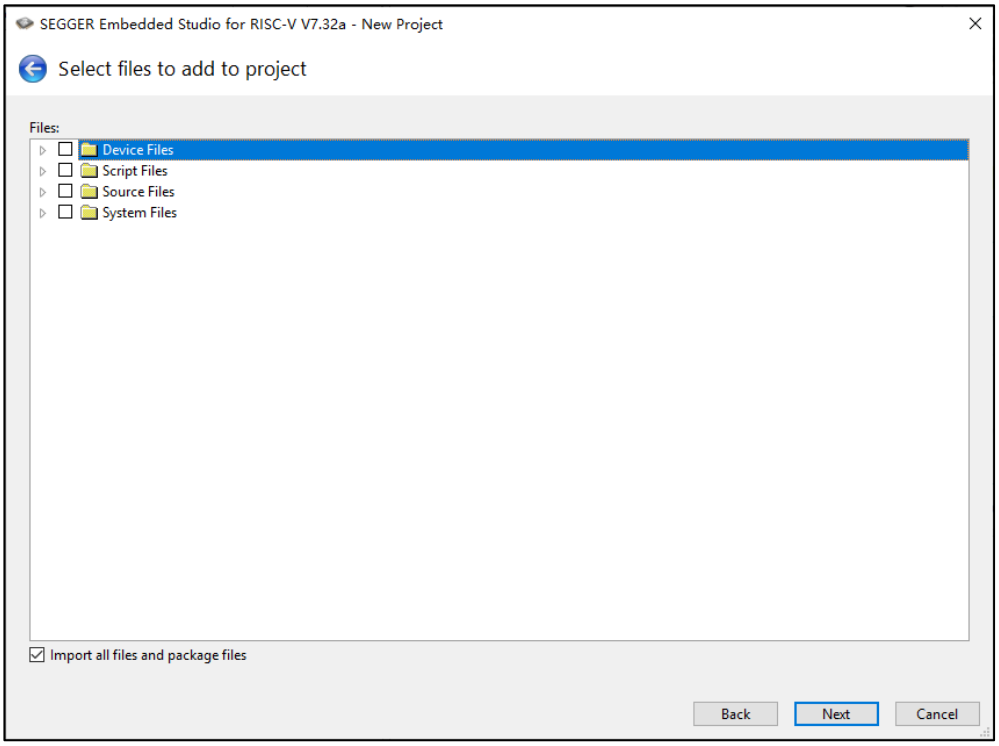
步骤 2：点击“Next”，进入通用工程设置界面，包括芯片选型，编译器类型选择，链接输出文件类型选择，预定义宏设置，头文件包含路径设置，输入/输出支持选择，栈大小配置，参考*图 3-10. 基于标准固件库的通用工程设置*。

图 3-10. 基于标准固件库的通用工程设置



步骤 3：点击“Next”，进入工程文件选择界面，全部取消勾选默认配置项，参考*图 3-11. 基于标准固件库的工程文件选择*。

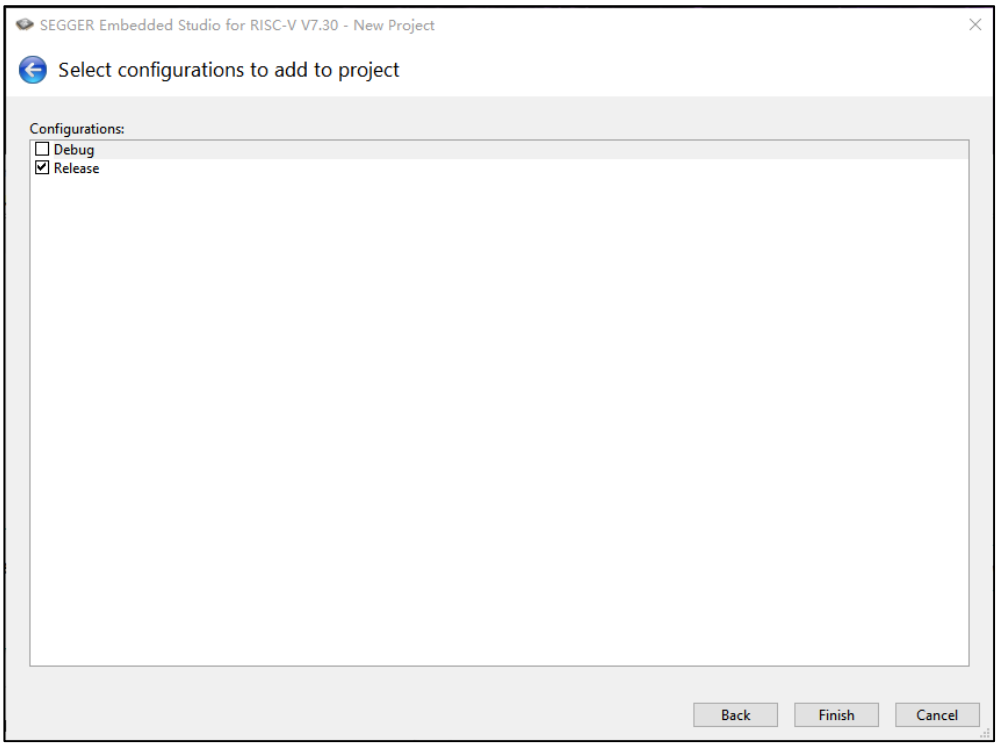
图 3-11.基于标准固件库的工程文件选择



步骤 4：点击“Next”，进入工程配置选择界面，参考*图 3-12. 基于标准固件库的工程配置界*

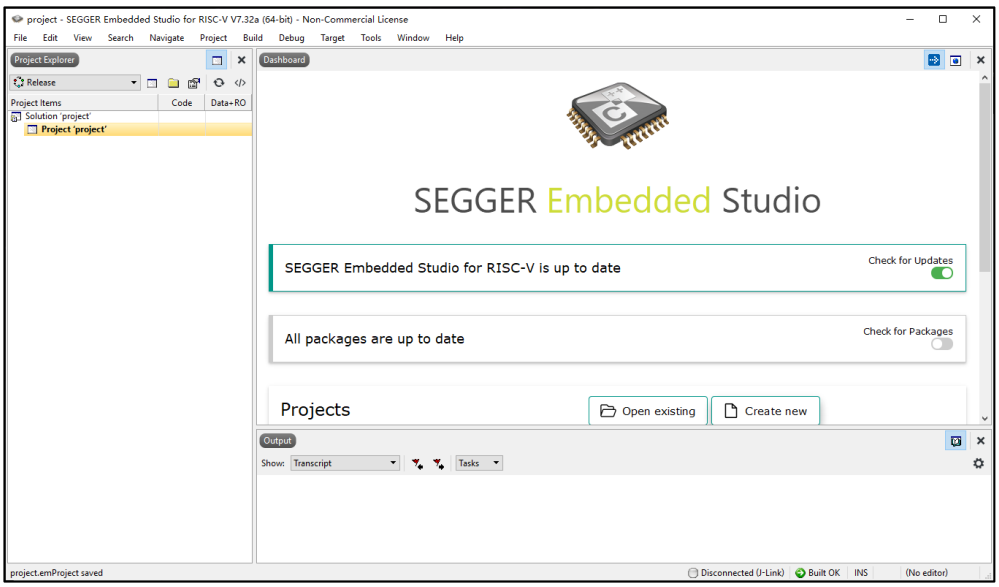
面。

图 3-12. 基于标准固件库的工程配置界面



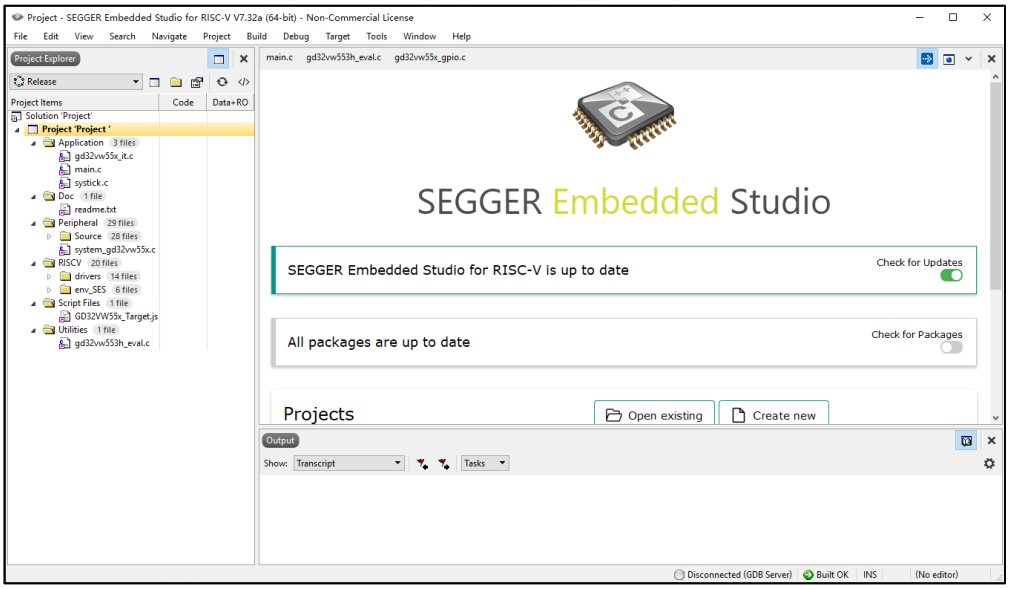
步骤 5：点击“Finish”，进入工程界面，用户可以基于此空工程进行二次开发，参考*图 3-13. 空工程*。

图 3-13. 空工程



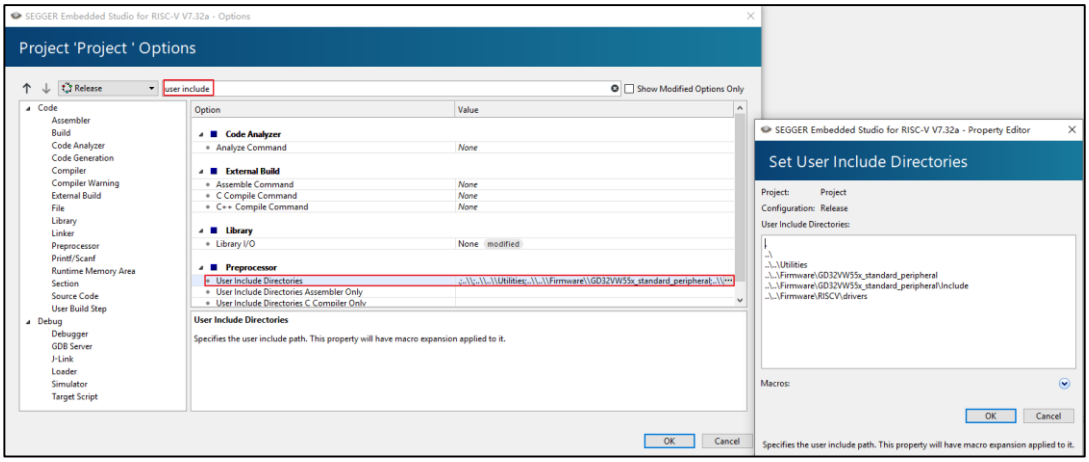
步骤 6：将固件库文件按照如下结构进行组织，参考*图 3-14. 工程文件结构*。具体文件结构，参考固件库模板例程。

图 3-14. 工程文件结构



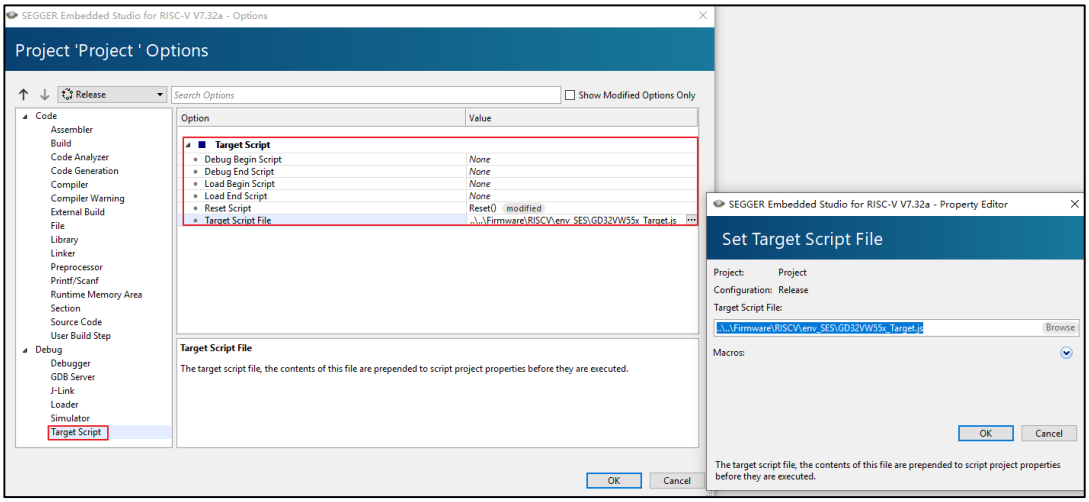
步骤 7：点击“Project->Options”，进入工程配置界面，配置用户头文件包含路径，参考*图 3-15. 用户包含路径配置*。

图 3-15. 用户包含路径配置



步骤 8：点击“Project->Options”，进入工程配置界面，配置脚本文件，参考*图 3-16. 脚本配置*。

图 3-16. 脚本配置

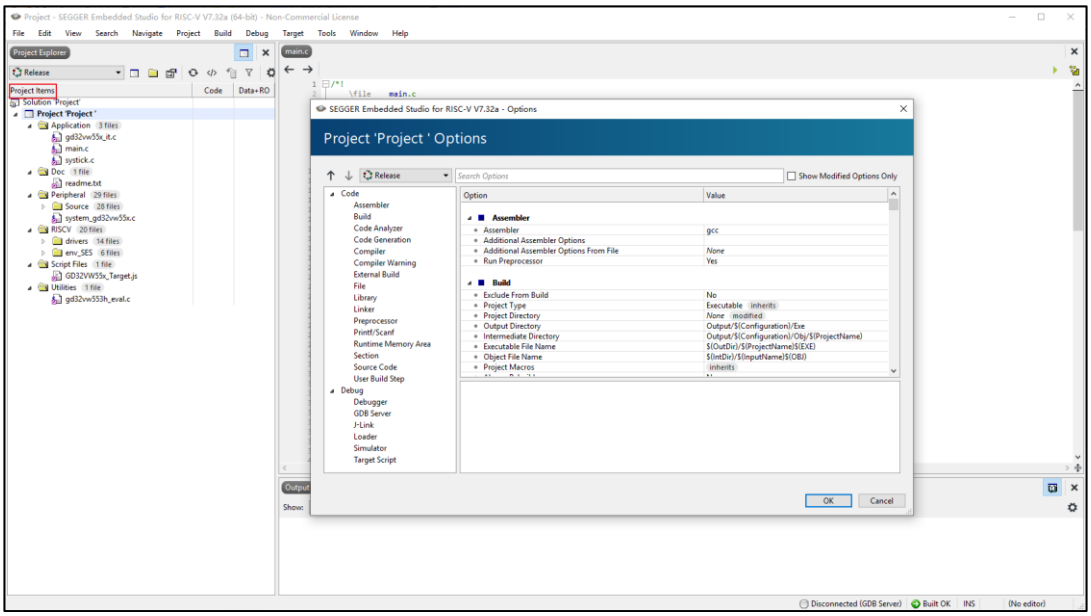

SEGGER Embedded Studio for RISC-V V7.32a - Options
Project 'Project ' Options
Release
Search Options
Show Modified Options Only
Code
Assembler
Build
Code Analyzer
Code Generation
Compiler
Compiler Warning
External Build
File
Library
Linker
Preprocessor
Printf/Scanf
Runtime Memory Area
Section
Source Code
User Build Step
Debug
Debugger
GDB Server
J-Link
Loader
Simulator
Target Script
Option
Value
Target Script
Debug Begin Script
Debug End Script
Load Begin Script
Load End Script
Reset Script
Target Script File
None
Reset()
modified
Target Script File
The target script file, the contents of this file are prepended to script project properties before they are executed.
OK
Cancel
SEGGER Embedded Studio for RISC-V V7.32a - Property Editor
Set Target Script File
Project:
Project
Configuration:
Release
Target Script File:
Browse
Macros:
OK
Cancel
The target script file, the contents of this file are prepended to script project properties before they are executed.

4. IDE 界面介绍

4.1. 工程配置选项

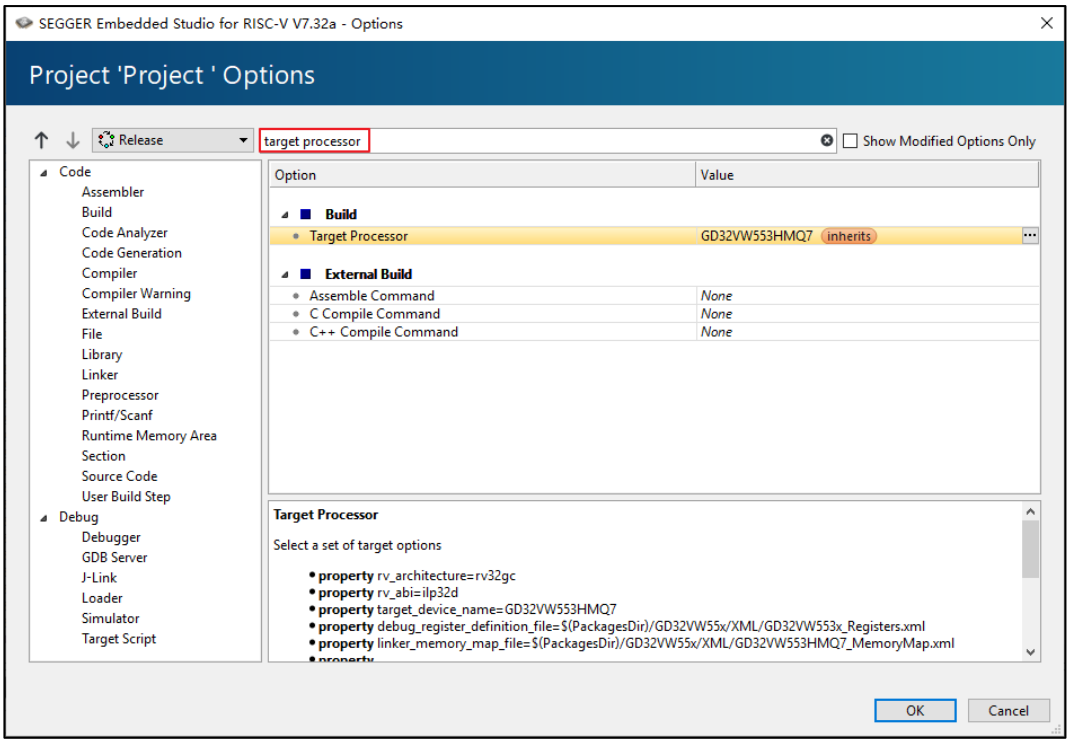
用户可以通过右键点击“Project Items”栏下对应 Solution / Project / 文件夹 / 文件，选择“Options...”进行配置选项设置。

图 4-1. 工程配置选项



4.1.1. 芯片选型

图 4-2. 芯片选型



4.1.2. 汇编器/编译器配置

图 4-3. 汇编器配置

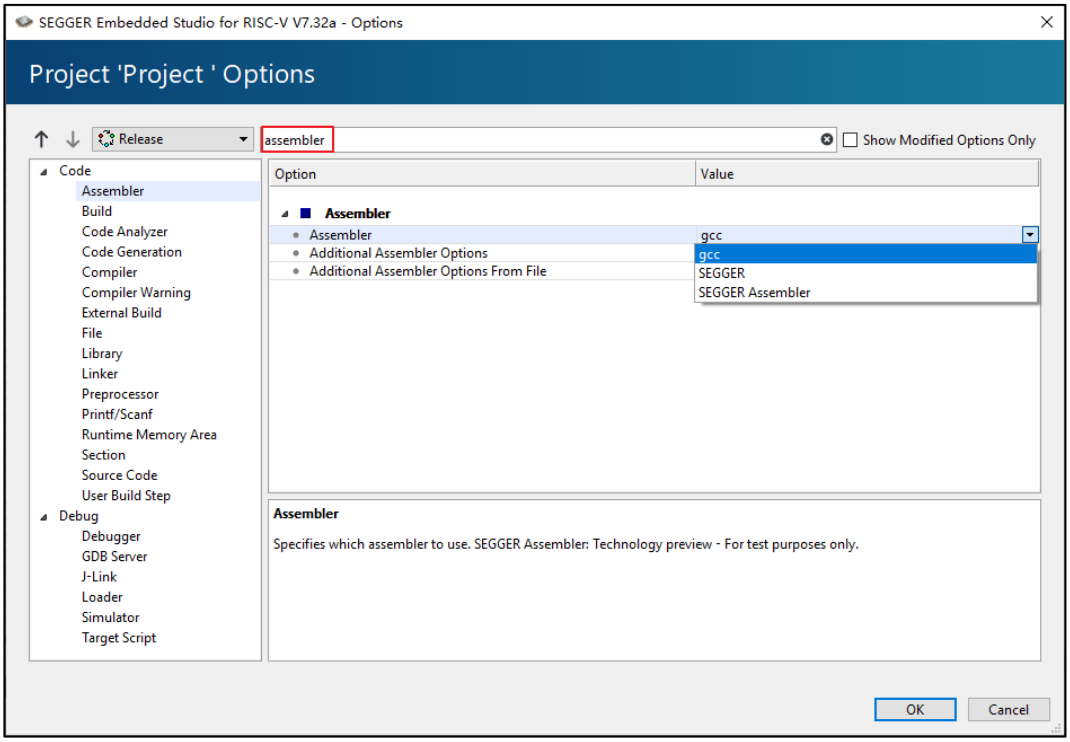
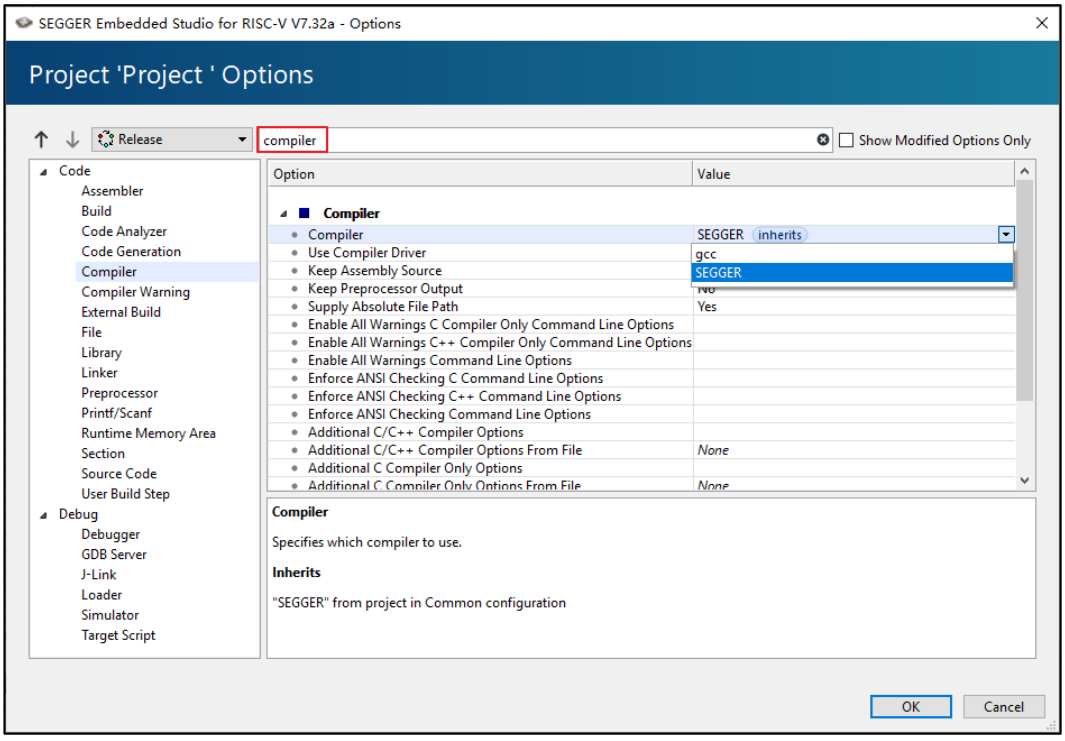
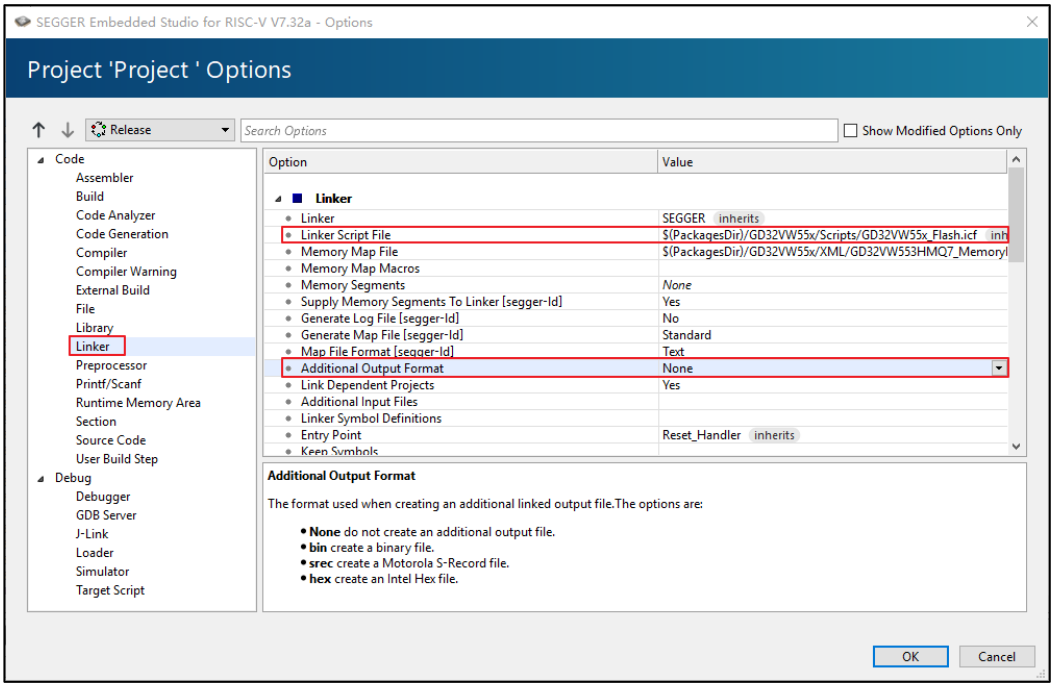


图 4-4. 编译器配置



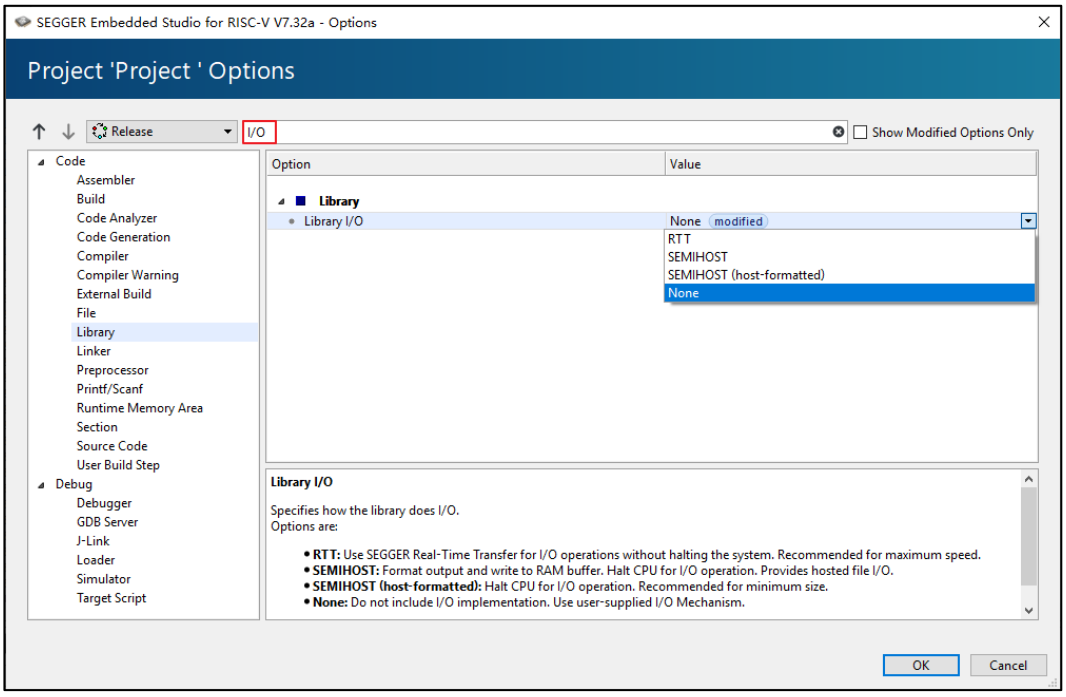
4.1.3. 链接脚本及链接输出格式配置

图 4-5. 链接脚本及输出格式配置



4.1.4. 输入/输出库配置

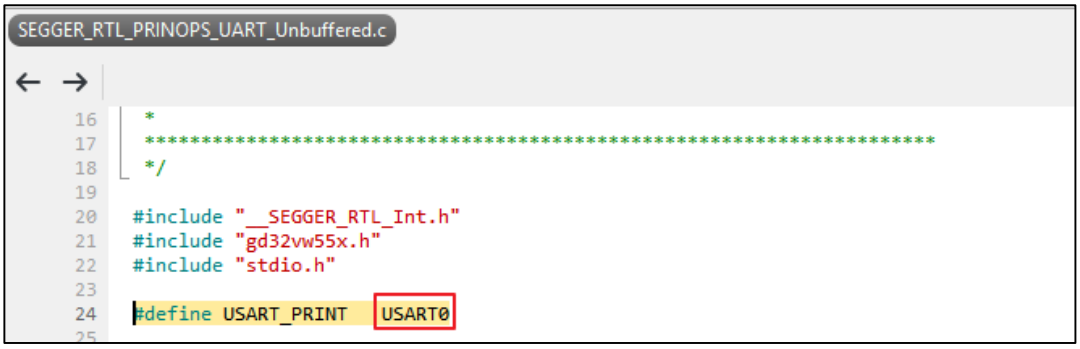
图 4-6. I/O 库配置



当选择为 None 时，用户可通过修改“SEGGER_RTL_PRINOPS_UART_Unbuffered.c”文件

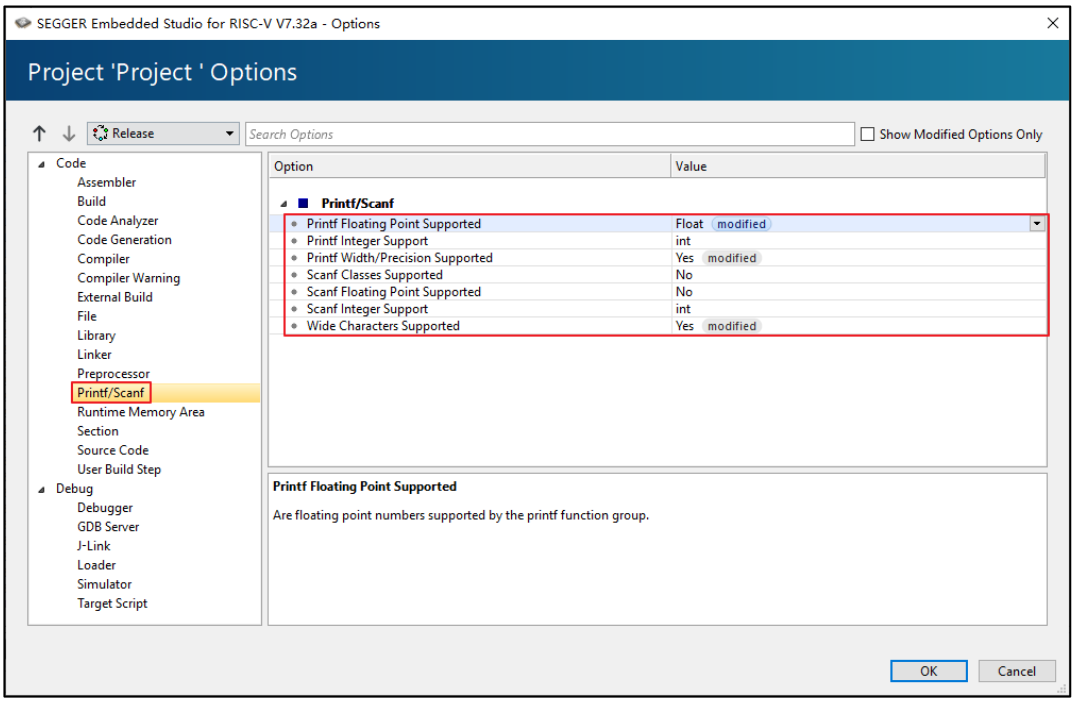
中的宏 USART_PRINT 指定打印串口，参考*图 4-7. 硬件串口配置*。

图 4-7. 硬件串口配置



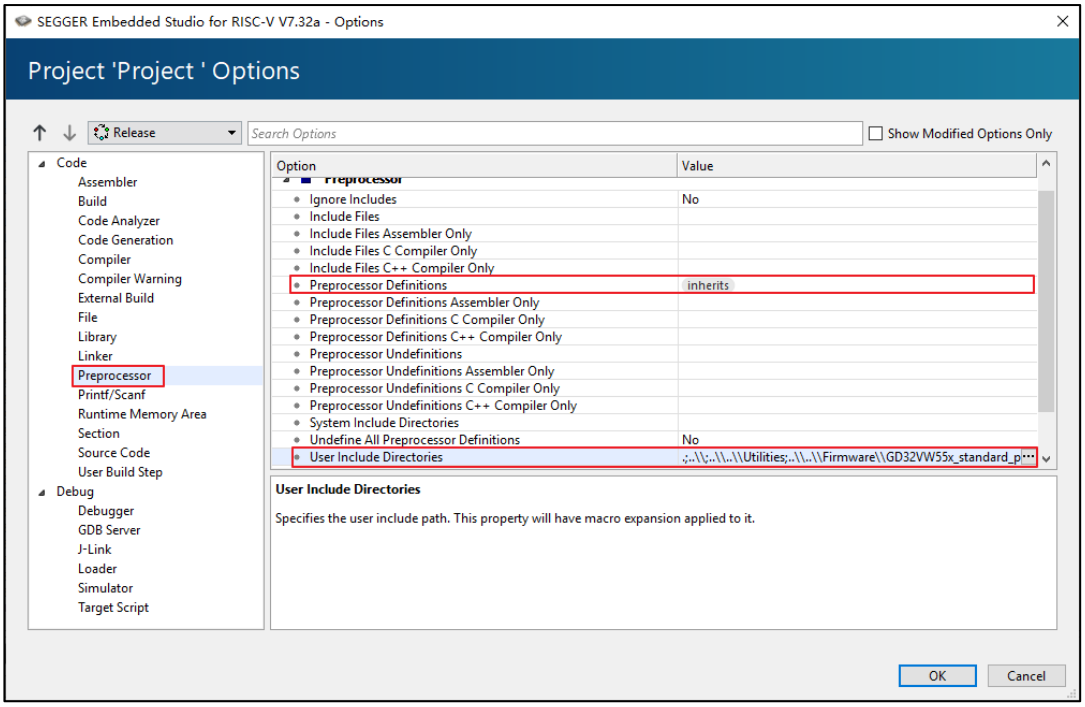
4.1.5. 输入/输出格式支持配置

图 4-8. 输入/输出格式支持配置



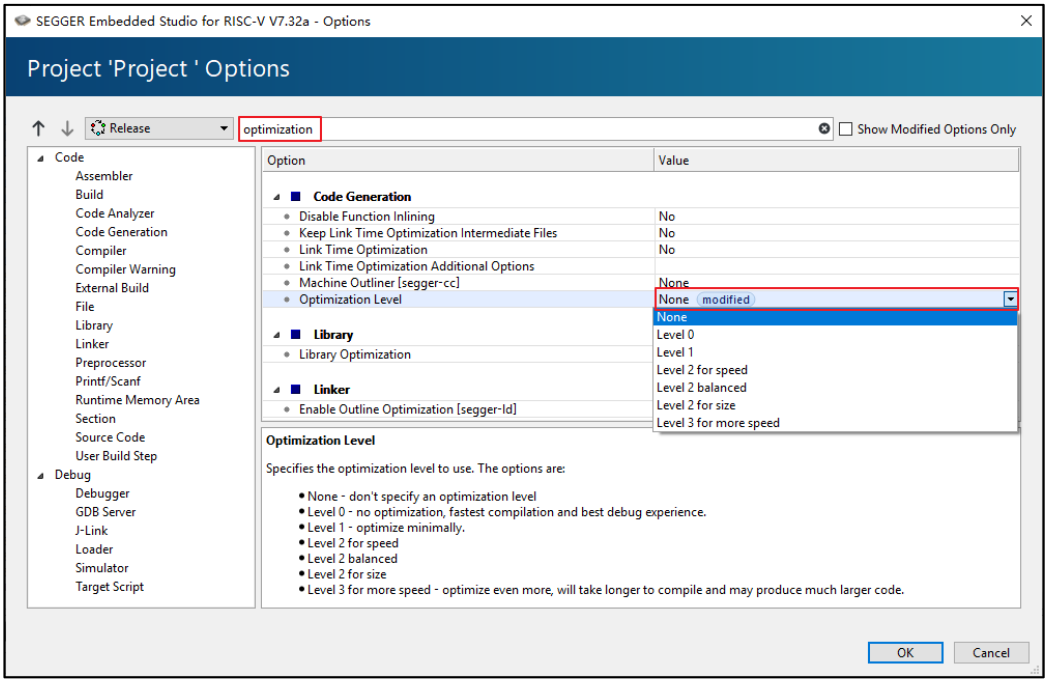
4.1.6. 预处理配置

图 4-9. 预处理配置



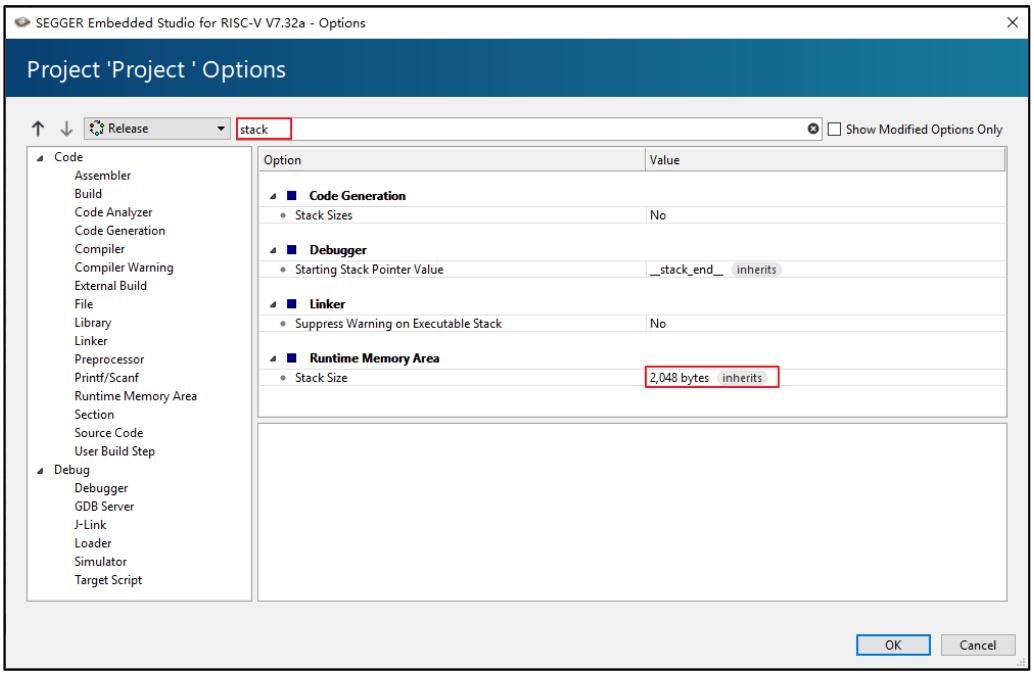
4.1.7. 优化等级配置

图 4-10. 优化等级配置



4.1.8. 栈配置

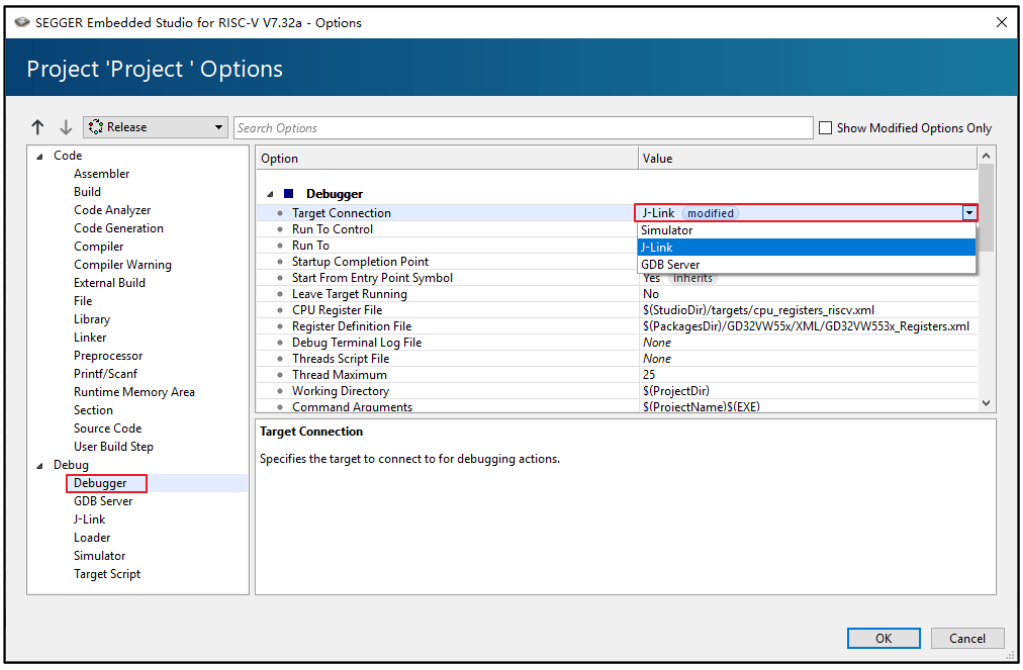
图 4-11. 栈配置



4.1.9. 调试器配置

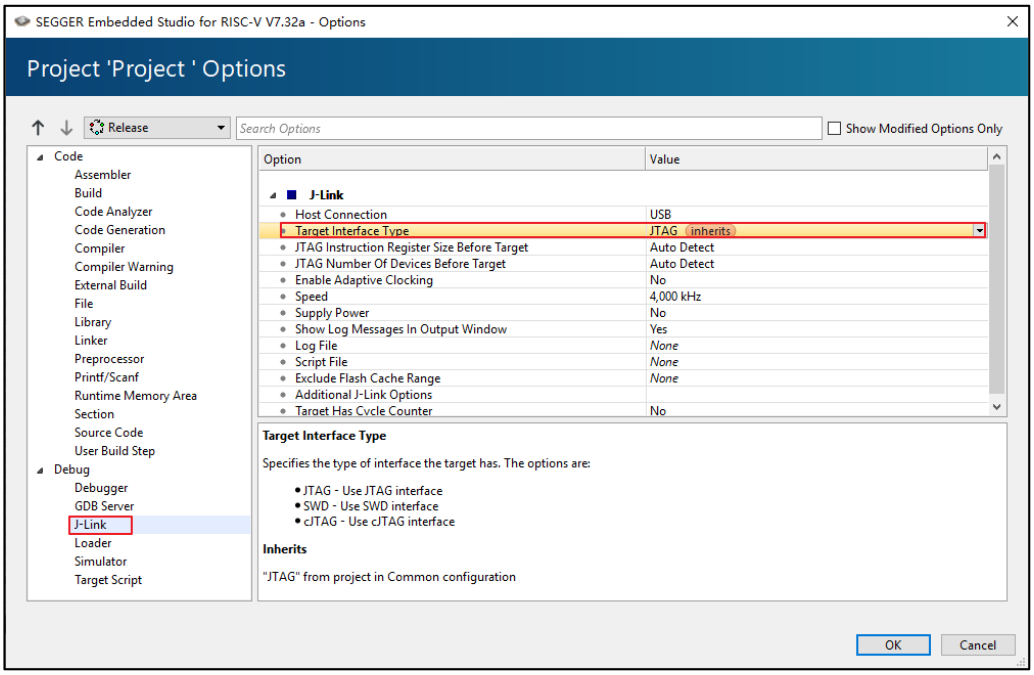
用户可以选择 J-Link 或 GDB Server 的方式进行工程的下载和调试操作，参考*图 4-12. 调试器*。

图 4-12. 调试器配置



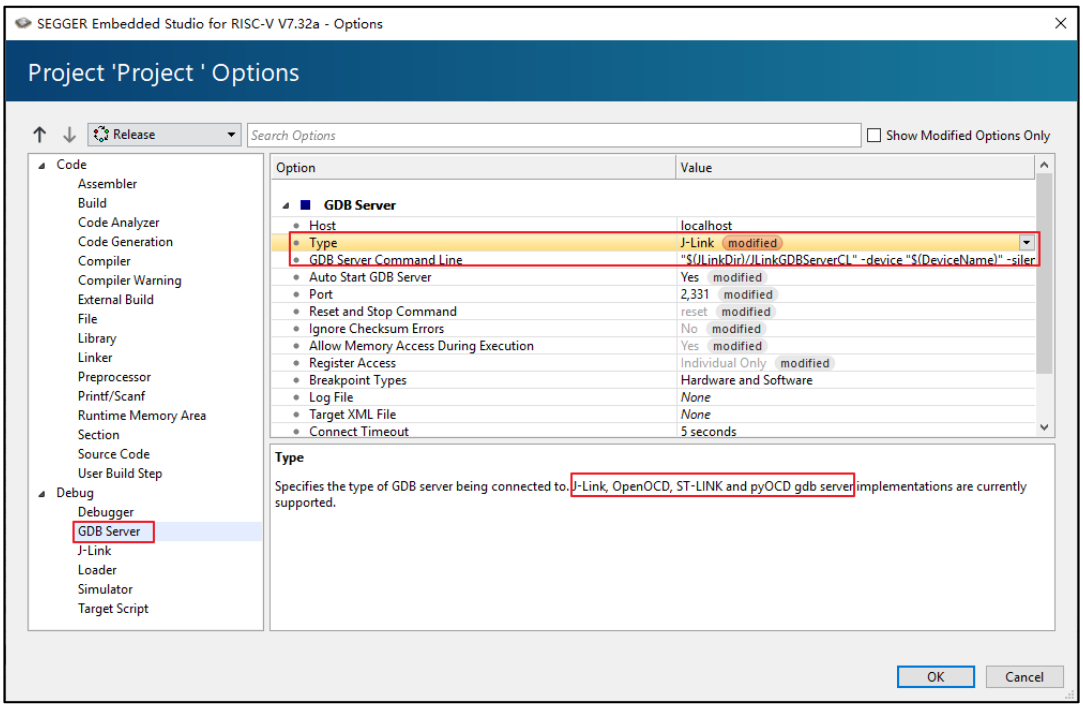
当选择 J-Link 方式进行工程开发时，参考*图 4-13. J-Link 配置*。

图 4-13. J-Link 配置



当选择 GDB Sever 方式进行工程开发时，按照需求选择合适的 GDB Server，参考*图 4-14. GDB Server 配置*。

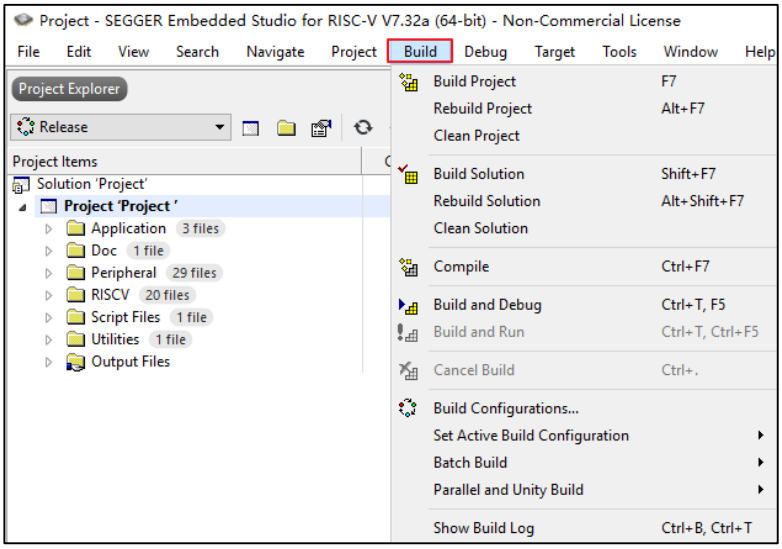
图 4-14. GDB Server 配置



4.2. 工程编译选项

通过点击菜单栏的“Build”选项，可对 Project / Solution 进行清除，编译和重编译操作；并可对当前活跃工程执行编译后运行或调试操作，参考*图 4-15. 工程编译选项*。

图 4-15. 工程编译选项



4.3. 工程调试选项

通过点击菜单栏的“Debug”选项，可对目标芯片进行调试，断点设置等操作，参考*图 4-16. 工程调试选项*和*图 4-17. 工程调试界面*。

图 4-16. 工程调试选项

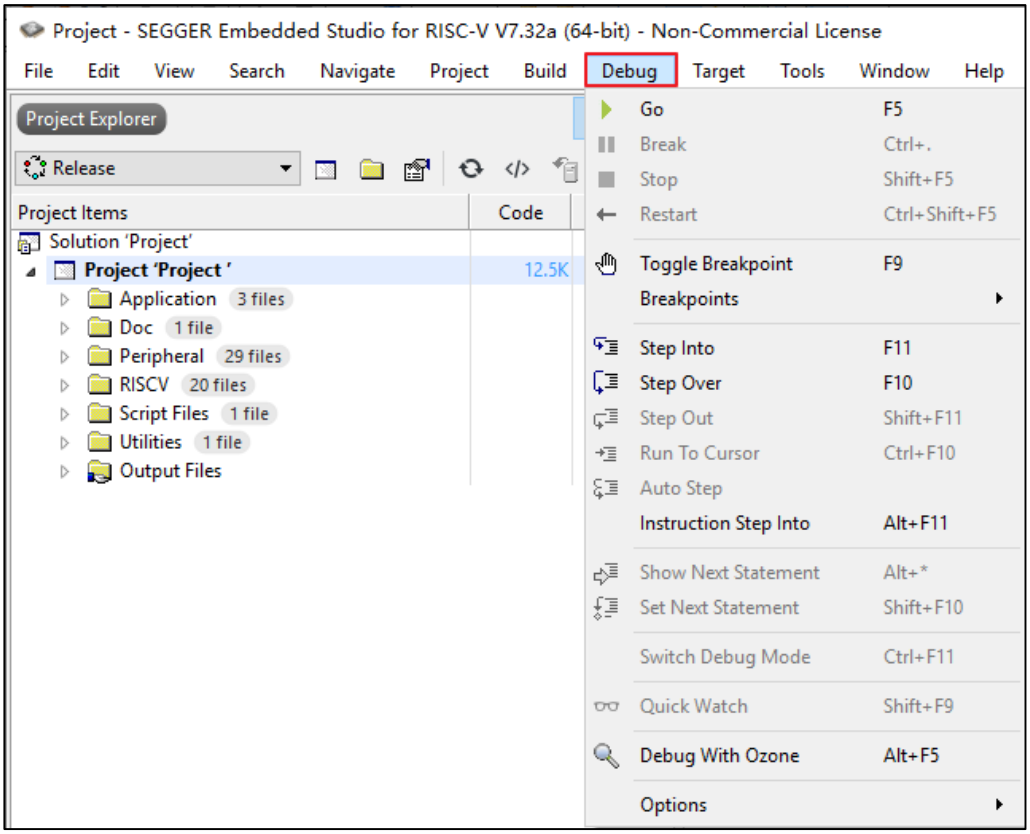
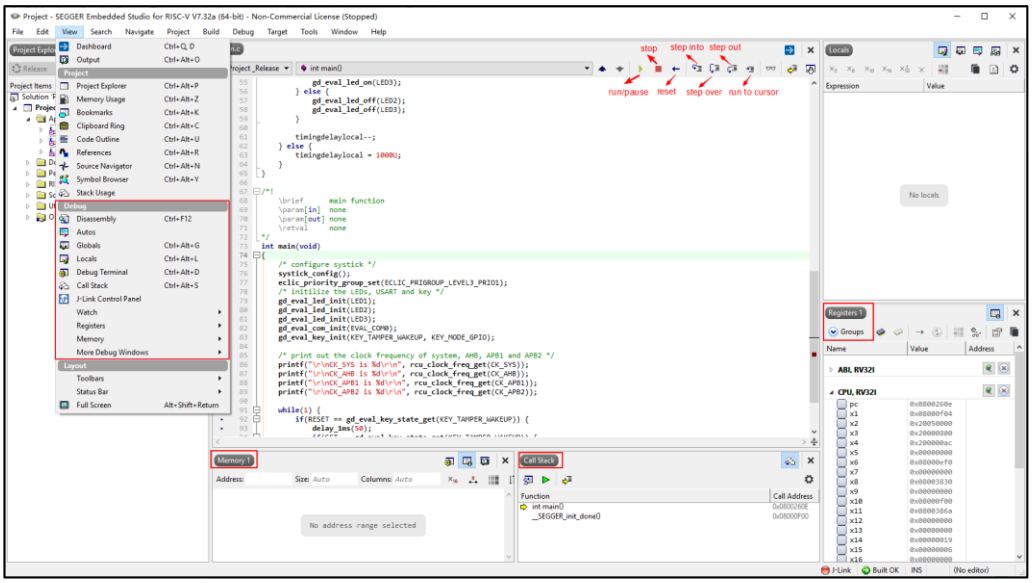

Project - SEGGER Embedded Studio for RISC-V V7.32a (64-bit) - Non-Commercial License
File Edit View Search Navigate Project Build Debug Target Tools Window Help
Project Explorer
Release
Project Items
Code
Solution 'Project'
Project 'Project '
12.5K
Application 3 files
Doc 1 file
Peripheral 29 files
RISCV 20 files
Script Files 1 file
Utilities 1 file
Output Files
Go F5
Break Ctrl+.
Stop Shift+F5
Restart Ctrl+Shift+F5
Toggle Breakpoint F9
Breakpoints
Step Into F11
Step Over F10
Step Out Shift+F11
Run To Cursor Ctrl+F10
Auto Step
Instruction Step Into Alt+F11
Show Next Statement Alt+*
Set Next Statement Shift+F10
Switch Debug Mode Ctrl+F11
Quick Watch Shift+F9
Debug With Ozone Alt+F5
Options

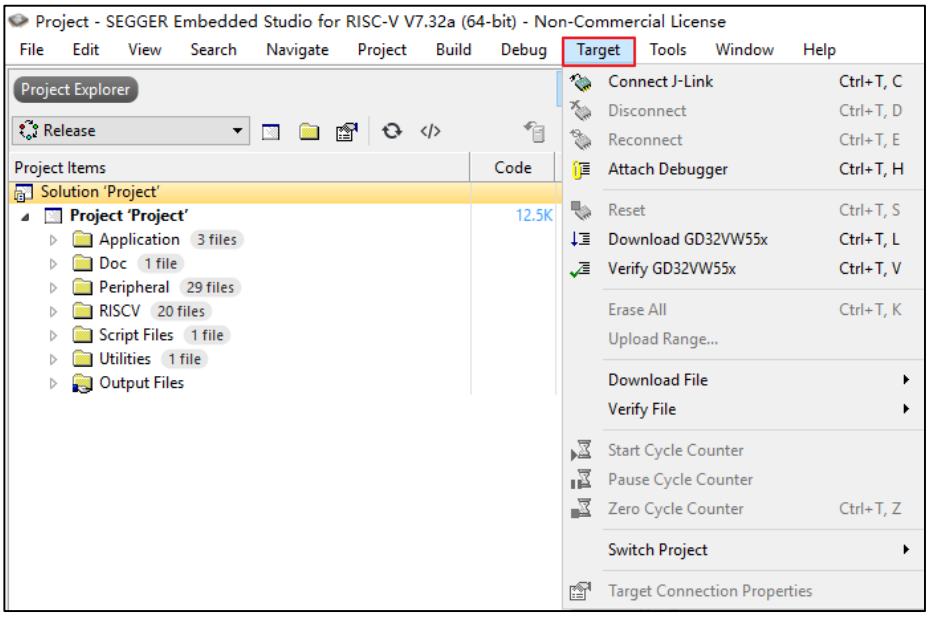
图 4-17. 工程调试界面



4.4. 目标芯片操作选项

通过点击菜单栏的“Target”选项，可对目标芯片执行连接，断开，附着，下载和验证等操作，参考*图 4-18. 目标芯片操作*。

图 4-18. 目标芯片操作



5. 版本历史

表 5-1. 版本历史

版本号.	说明	日期
1.0	首次发布	2024 年 1 月 15 日

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