GigaDevice Semiconductor Inc.

GD32 MCU EMC Hardware Protection Design Reference

Application Notes
AN163

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1. Foreword

As a general control component, MCU has a wide range of applications. In actual electronic products, in addition to the basic software and hardware functions, MCU needs to provide certain EMC performance.

During the use of MCU, the pins of MCU can be roughly divided into Global PIN and Local PIN according to the different pin definitions of GPIO. Local PIN means that the terminal component connected to the MCU pin is inside the PCB and does not need to be led out through the interface, such as an external Flash circuit connected through the SPI interface. Global PIN means that the MCU pin needs to be connected to other PCBs or devices through the interface for signal interaction, such as CAN, USB, UART, Display, SWD, I2C, and test points. The Global PIN interface is generally located at the edge of the PCB, and it allows users to plug and unplug cables in the product. This process increases the possibility of introducing EMS interference through the interface, and surrounding charged objects may also produce electrostatic discharge interference on the interface.

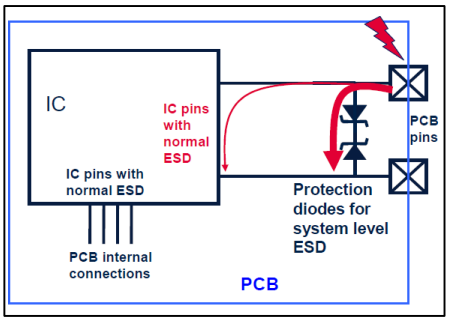
Therefore, factor in EMS during product design. In addition, EMI radiation also needs to be controlled. When some high-speed communication interfaces are used, because the peripheral clock sends square signals, the frequency of multiple harmonics on the rising edge may be higher than that of the peripheral clock of MCU. During PCB design, if a certain low impedance return path and a small return area are not provided for the return of high-frequency signals, EMI radiation is likely to be out of limit. For example, when the MCU reads and writes Flash through the SPI interface, EMI radiation is likely to be out of limit on the SCK wiring and the FPC during display refresh.

This document provides some EMC protection design references for MCU hardware design, aiming to help optimize the EMC performance of MCU in product applications.

2. Global PIN ESD protection design

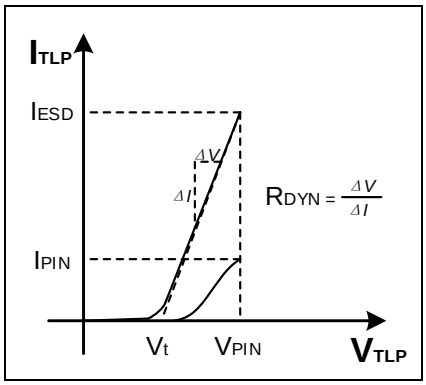
In the application process of MCU, special attention should be given to EMC protection design for the Global PIN. Common interfaces include SWD, UART, I2C, enable control pins, test points, etc. During the implementation of basic functions, transient overvoltage or electrostatic interference may occur on load terminals connected to the pins due to changes in inductive loads, resulting in malfunction and damage. TVS can be used to suppress the transient overvoltage or electrostatic interference on the pins to a certain extent. As shown in ***Figure 2-1. Schematic diagram of TVS protection***, the protection of TVS for the pins is to discharge most of the interference to the GND, so that the interference on the GPIO interface is minimized. Reasonable TVS selection is crucial for the protection effect. For more details on TVS selection, refer to ***AN051 ESD Protective Components - Selection and Use of TVS***.

Figure 2-1. Schematic diagram of TVS protection



When the TVS provides protection, it works in the reverse breakdown status. In this status, the TVS has a small on-resistance so that a large current can flow. The instantaneous discharge of a large current can reduce the level of interference voltage on the GPIO interface, achieving a clamping action on overvoltage. The key parameters for the use of TVS are the clamping voltage and current discharge capability. For TVS with the same clamping voltage, the overcurrent capability of TVS can be evaluated through the power parameters provided in the data book. During large current discharge, the on-resistance of TVS is small and dynamically changing. The on-resistance value is related to the magnitude of discharge current. As shown in ***Figure 2-2. PIN&TVS TLP curve chart***, reasonable TVS selection must meet the following conditions: The clamping voltage of TVS is lower than the failure voltage of IC, and the discharge current of TVS is higher than the failure current of GPIO under the premise that the clamping voltage of TVS is lower than the failure voltage of GPIO, so that TVS can provide sufficient protection for GPIO.

Figure 2-2. PIN&TVS TLP curve chart



During the use of TVS, the case as shown in ***Figure 2-3. PIN&TVS TLP curve chart*** also occurs. The clamping voltage of TVS is close to or higher than the failure voltage of IC, as shown in ***Figure 2-4. Schematic diagram of enhanced ESD protection by a series resistor***. In this case, an additional resistor can be connected in series to increase the difference between the above two voltages to improve the problem. When the clamping voltage of TVS is higher than the failure voltage of IC, the series resistance is calculated according to the formula as shown in ***Figure 2-5. Calculation method of series resistance between TVS and PIN***. The failure voltage and failure current of MCU GPIO can be measured through TLP. The chip-level IV results of TLP testing can be co-designed with system-level ESD protection.

Figure 2-3. PIN&TVS TLP curve chart

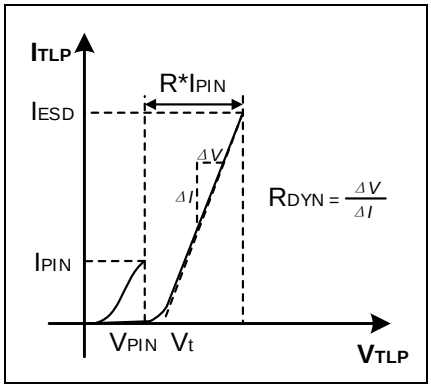


Figure 2-4. Schematic diagram of enhanced ESD protection by a series resistor

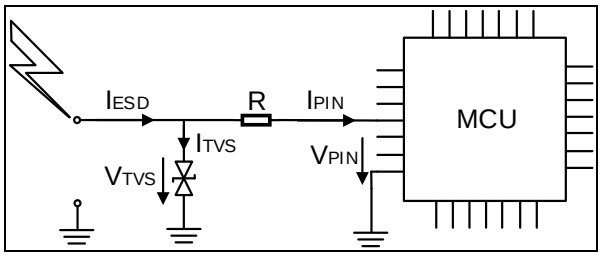


Figure 2-5. Calculation method of series resistance between TVS and PIN

$$R \geqslant \frac{(I_{ESD} - I_{PIN}) \cdot R_{DYN} + V_t - V_{PIN}}{I_{PIN}}$$

The selection of series resistors varies with the pin functions. For the approximate value ranges based on different function types, see ***Table 1-1. ESD protection resistor reference***.

Table 1-1. ESD protection resistor reference

Function type	Recommended resistance
Enable control pin	Several hundred to 1K ohms
SWD	Less than 100 ohms
Test point	Several hundred to 1K (it is generally recommended to add resistors to the test probe end)
UART	Less than 100 ohms
I2C	Less than 100 ohms

Another factor that has a key influence on TVS protection is the layout of TVS on the PCB, as shown in ***Figure 2-6. TVS layout***. To ensure the ESD protection capacity of TVS, the TVS must be close to the source of interference to discharge the interference, and secondly, the return path of the interference discharged by the TVS must have a minimal impact on other components on the PCB. The TVS usually discharges ESD energy by drilling via holes directly near the TVS pads to release the ESD energy to the GND. As shown in ***Figure 2-7. Placement of TVS via holes***, an appropriate number of via holes can be selected. Generally, one via hole needs to be drilled on each side of the pads. Because the ESD energy contains rich high-frequency components, expanding the via hole surface area by increasing the via hole diameter properly can reduce the influence of kelvin effect to a certain extent, thus reducing the impedance.

Figure 2-6. TVS layout

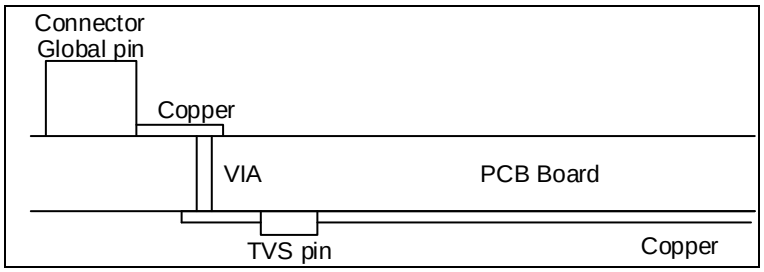
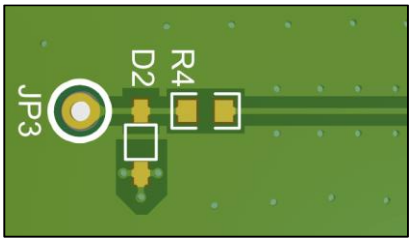


Figure 2-7. Placement of TVS via holes

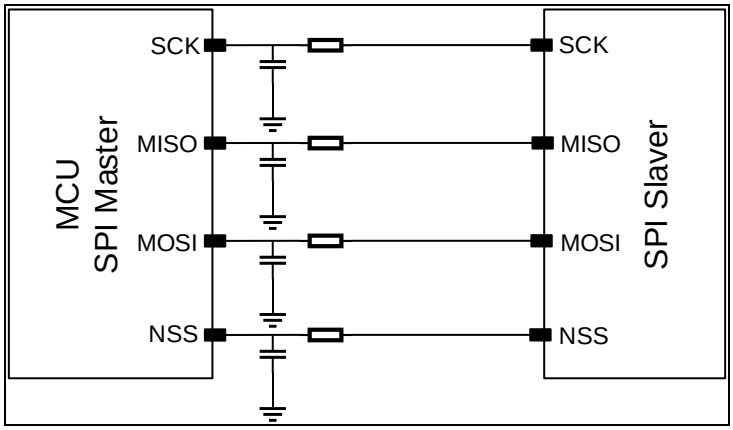


3. SPI interface protection design

The SPI bus is a serial peripheral communication bus, which generally forms a serial communication channel between on-board chips on the PCB. The bus is rarely connected to other PCBs through long cables. A common application is that the MCU is connected to peripherals such as Flash, ADC, and DAC through the SPI interfaces to implement specific functions. The communication rate of the MCU SPI bus can reach up to tens of MHz. When the SPI bus is used for communication, reasonable filter and layout designs are required to control the energy radiated by the EMI.

For the SPI bus of MCU, control measures can be implemented from both the software and hardware aspects. In terms of hardware, the amount of radiation can be reduced by adding filters. Commonly employed filter methods consist of RC filters, LC filters, and magnetic bead filters. Optimal results are achieved by positioning the filters in proximity to the radiation source, typically located at the driver end, as illustrated in ***Figure 3-1. Schematic diagram of SPI interface filtering***. Radiation sources on the PCB can also be located by using near-field probes. Common sources of radiation from the SPI bus are the SPI clock line or the power supply network of MCU. When the clock frequency on the SPI clock line is tens of MHz, its multiple harmonics can reach hundreds of MHz or more. If the return path of the SPI clock line is large and forms an obvious loop antenna effect, the EMI radiation is likely to be out of limit. In addition, the quick high and low flips of the SPI clock and signal lines can cause transient current fluctuations on the power supply network. At this point, if the return path formed by the power supply network is large, the EMI radiation may also be out of limit.

Figure 3-1. Schematic diagram of SPI interface filtering



The layout of the SPI bus also helps improve EMI radiation. The clock frequency of the SPI bus is relatively high, and PCB wiring should be designed according to the wiring rules of high-speed PCB. Pay attention to the following key points:

- Try to meet the 3W wiring rules, as shown in ***Figure 3-2. Schematic diagram of 3W wiring rules***. The distance between the clock line and the signal line needs to be more than three times the line width to reduce the crosstalk effect of the clock line on signals.

- Try to route the SPI clock lines or data lines on the same layer to reduce the use of via holes. As shown in ***Figure 3-3. Schematic diagram of wiring of signal line***, try to minimize the path of the wiring to avoid U-shaped wiring that is folded back and forth. During wiring, avoid 90° fold lines at corners and use 45° fold lines or curved wiring. The SPI SCK signals can be controlled with characteristic impedance based on project cost considerations. The wiring should be designed with 50Ω characteristic impedance to reduce overshoot due to signal reflection effects, thus reducing EMI radiation to a certain extent. The filters of the SPI bus can be placed as close to the MCU pins as possible, so that the excessive frequency bands can be filtered in advance at the driver end.
- When designing a multi-layer PCB, aim to establish a complete return path for the SPI bus wiring. Multi-layer PCBs with more than two layers usually feature a complete ground plane. For wiring the SPI bus, consider placing it on an inner layer to benefit from the shielding effect provided by the copper layers on the top and bottom surfaces.

Figure 3-2. Schematic diagram of 3W wiring rules

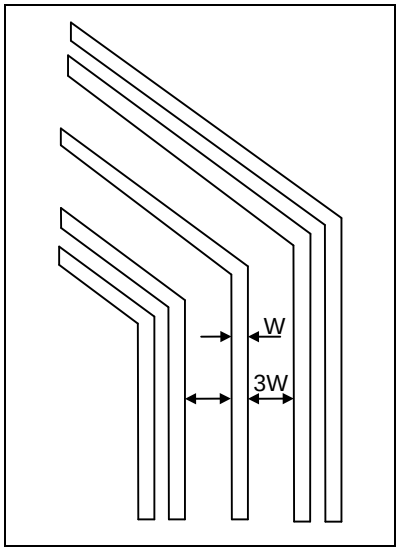
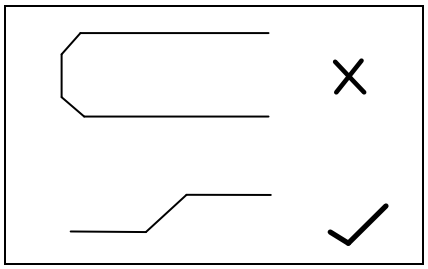


Figure 3-3. Schematic diagram of wiring of signal line



The relatively low-cost EMI suppression method is to make adjustment through software. The GPIO of MCU provides the function of adjusting the drive capability defaulting to 50 MHz. As shown in ***Figure 3-4. SPI SCK waveform - 50 MHz drive***, the rising edge of the waveform at 50 MHz is steep with a certain overshoot, and the drive capability can be set to 10 MHz or 2 MHz through software during initialization. As shown in ***Figure 3-5. SPI SCK waveform - 2 MHz drive***, the adjustment of drive capability of the GPIO interface is reflected in the waveform of the GPIO signal flip. When the drive speed of GPIO is adjusted from 50 MHz to 2 MHz, it can be clearly observed from the waveform that the rising edge of the waveform

after the adjustment becomes less steep, and the overshoot decreases. Such changes indicate that some high-frequency components in the waveform are attenuated to reduce EMI radiation. This method has a relatively low cost but present certain disadvantages. For applications with a relatively high SPI SCK frequency, a longer rising edge of the clock waveform shortens the sampling and holding time in the digital signal, which may affect the communication function. Therefore, when this method is used, the waveform parameters need to be confirmed to make sure that the normal functions are not affected.

Figure 3-4. SPI SCK waveform - 50 MHz drive

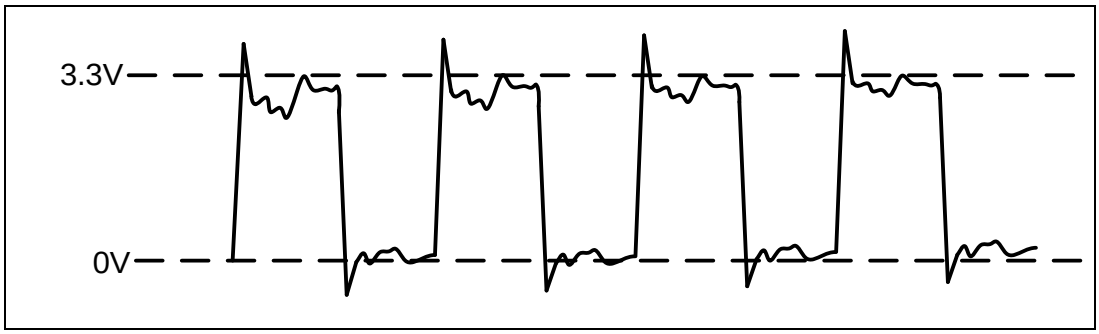
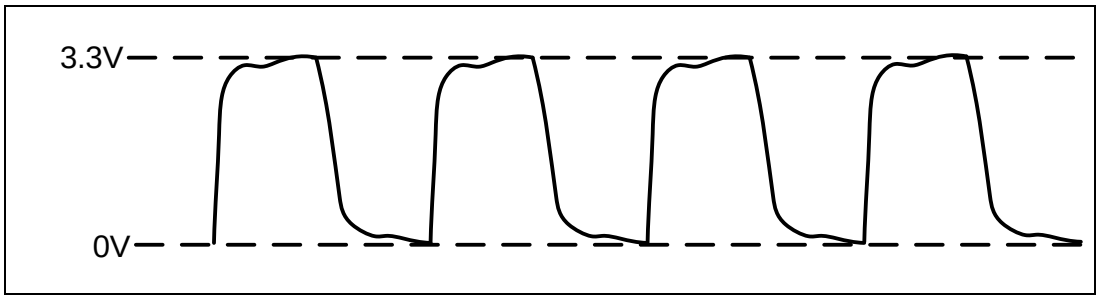


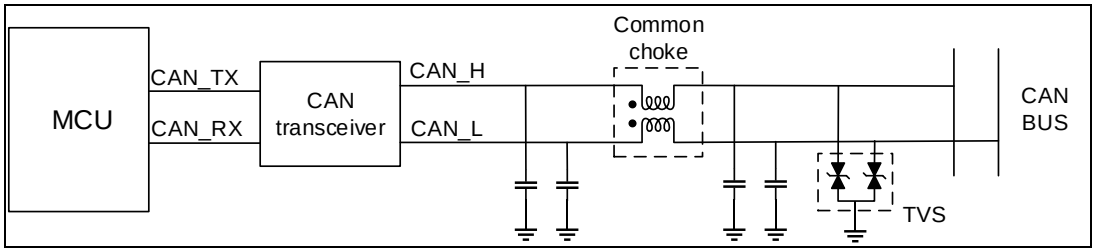
Figure 3-5. SPI SCK waveform - 2 MHz drive



4. CAN interface protection design

The CAN communication protocol has been widely used since its inception. Because the application environment of the CAN communication protocol is relatively complex, such as in complex industrial environments and high-reliability automobiles, sufficient anti-interference capabilities are required for the CAN bus. Some models of GD32 MCU support two-wire CAN communication interfaces. The currently supported CAN communication protocol is CAN2.0B/CAN FD. The MCU with CAN communication functions integrates the CAN controller internally, and realizes the conversion between the differential signal and the logic level of MCU through the external CAN transceiver to realize the most basic CAN communication functions, as shown in ***Figure 4-1. MCU CAN communication circuit diagram***.

Figure 4-1. MCU CAN communication circuit diagram

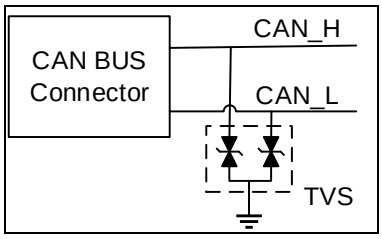


4.1. ESD protection of CAN communication

CAN communication is an interconnection communication protocol for LAN. Various electronic functional modules with CAN communication are mounted on the same bus to communicate with each other. CAN communication interfaces are usually designed at the edge of the PCB so that communication cables can be easily connected. However, the interfaces located at the edge of the PCB are more likely to be subject to electrostatic interference than the circuit function modules inside the PCB. Because electrostatic interferences introduced by the interfaces at the edge of the PCB enter the inside of the PCB through the propagation path, severe interferences may occur and cause system malfunctions. The common method for ESD protection of CAN communication is to connect electrostatic interference suppression components in parallel at the interfaces. Discrete TVS or TVS arrays are usually used to form a protection circuit.

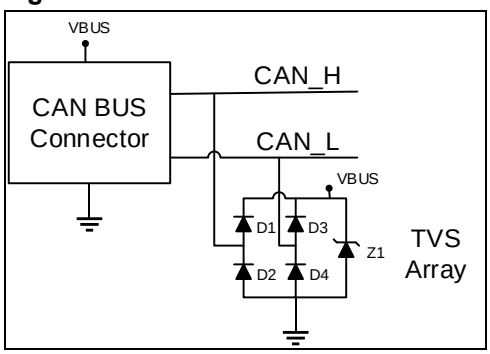
TVS protects the transceiver by clamping the transient high voltage to a safe level. TVS has a high impedance at a voltage below the breakdown voltage and a low impedance at a voltage above the breakdown voltage. As shown in ***Figure 4-2. CAN communication TVS protection circuit diagram***, discrete TVS tubes are used to form a protection circuit. Two uni-directional diodes can be combined into a bi-directional TVS. The clamping voltage of the composite component is equal to the breakdown voltage of the reverse-biased diode plus the forward voltage drop of the forward-biased diode.

Figure 4-2. CAN communication TVS protection circuit diagram



As shown in ***Figure 4-3. CAN communication diode array protection circuit diagram***, a diode array integrating multiple diodes and Zener TVS is used to form a protection circuit. The array consists of four standard diodes and a uni-directional TVS. The CAN bus lines are protected by clamping the signal lines to a forward diode voltage drop above the power supply voltage or to a forward diode voltage drop below the ground voltage. One advantage of this circuit is that the diode array clamps to a voltage closer to the normal amplitude of the waveform. The diodes can be used to eliminate overshoot or ringing on the signal line. Another advantage of this configuration is that the capacitive load on the signal lines is usually smaller than that of the bi-directional TVS circuit, as shown in ***Figure 4-2. CAN communication TVS protection circuit diagram***. Diodes D1, D2, D3, and D4 have a low capacitance and are designed to have a short conduction time. Diode Z1 of TVS is used to dissipate most of the energy when an overvoltage occurs. Because the capacitive load of the component is on the power line rather than the data line, Z1 can be a component with large junction capacity and higher power. The main disadvantage of the diode array circuit is that the CAN_L and CAN_H waveforms may be clamped if common mode or bias voltages are present. Diode array circuits should only be used in systems that ensure that the offset voltage between the ground references of the CAN module is relatively low and less than the on-state voltage of the diodes.

Figure 4-3. CAN communication diode array protection circuit diagram



The CAN bus controller in the MCU is based on the power rails of the MCU. Most CAN transceivers require a 3.3 V or 5.0 V supply voltage generated by a 12 V or 24 V power supply. The RX and TX pins of the CAN transceivers are connected to the CAN controller pins of the MCU. The CAN_H and CAN_L signal pins of most CAN transceivers are designed to withstand DC voltages of ±40 V or higher on the signal lines. The maximum supply voltage of the system connected to CAN_H and CAN_L in the CAN transceiver is an important factor in selecting TVS components. TVS components should be selected such that the minimum breakdown voltage of the diodes is higher than the maximum system supply voltage. TVS

components are designed to dissipate peak power in the case of transient events, and should not be used to regulate the steady-state voltage.

4.2. CAN communication noise suppression

Common mode chokes are often used to attenuate noise common to both transceiver buses, as shown in ***Figure 4-4. CAN communication common mode noise suppression circuit diagram***. The function of chokes is to provide high impedance for common mode signals and low impedance for differential signals, thus improving the common mode rejection ratio (CMRR) of the transceivers. Chokes enable filtering on high-speed data lines without increasing a large number of distortions. Common mode chokes limit the magnitude of overvoltage surges on data lines by serving as filters. Therefore, it is recommended to add TVS components to the circuit to provide clamping protection. Chokes have several disadvantages, one of which is that the inductors of the components, the PCB, and the capacitors of the transceivers form a resonant circuit, which produces oscillations. Oscillations on the CAN signal lines can cause the transceiver to detect false bits. Another problem with choke filters is that any mismatch in the inductors of two coils will cause signal waveform distortion.

Figure 4-4. CAN communication common mode noise suppression circuit diagram

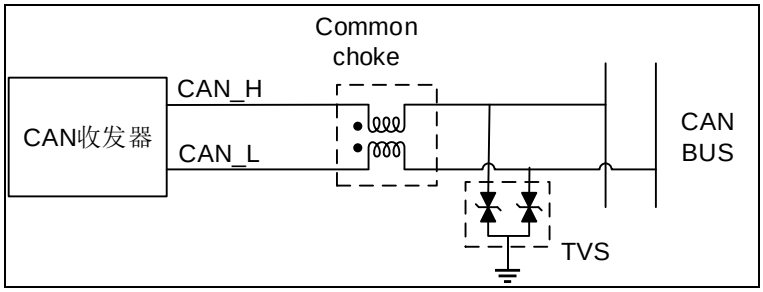
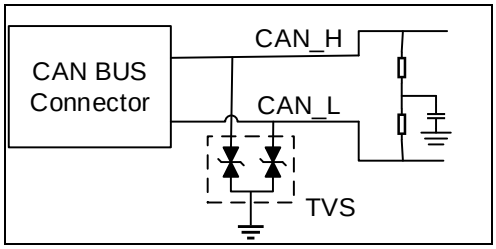


Figure 4-5. CAN communication terminal RC filter circuit diagram shows a separate terminating circuit that can be used to provide noise protection for CAN transceivers. The terminating circuit serves as a low-pass filter and consists of two resistors with equivalent resistance and a capacitor. The common-mode signal is terminated through a capacitor that shunts the high-frequency noise signal to the ground. The difference in resistance of terminating resistors should be as small as possible (R tol ≤ 1%) to maintain waveform symmetry between CAN_H and CAN_L signals.

Figure 4-5. CAN communication terminal RC filter circuit diagram

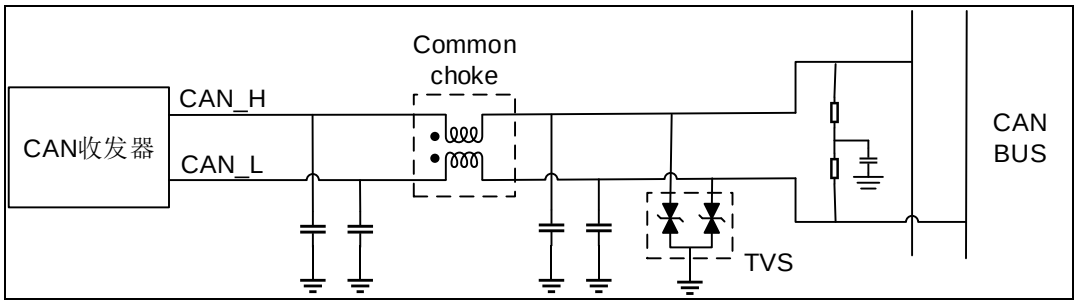


Shunt terminating circuits can be used in combination with TVS diodes. Resistance-capacitance (RC) circuits provide protection by serving as low-pass filters and limiting the slew rate of ESD or transient overvoltage signals. A TVS clamping device should be added to the shunt terminating circuit to make sure that the bus line voltage is not higher than the maximum rated voltage of the transceivers and capacitors.

Generally, the terminating resistors of the high-speed CAN bus are located at both ends of the network. If the CAN node is at the end of the bus, use two 60 Ω resistors instead of one 120 Ω resistor. If the transceiver is located at a CAN node without terminating resistor, resistors with higher resistance are required to keep the resistance of the terminating resistors connected in parallel at 60 Ω.

The combination of common mode chokes, capacitors, and TVS can be used to meet the EMI radiation and immunity requirements. As shown in ***Figure 4-6. CAN communication protection circuit diagram***, the noise entering the CAN node is attenuated by the second-order filters formed by the inductors and capacitors CH1 and CL1 of the choke filters. In contrast, capacitors CH2 and CL2 provide a filter to reduce the radiation or noise from the transceiver. The function of the bi-directional TVS is to clamp the transient voltage interference on the CAN bus to a safe value.

Figure 4-6. CAN communication protection circuit diagram



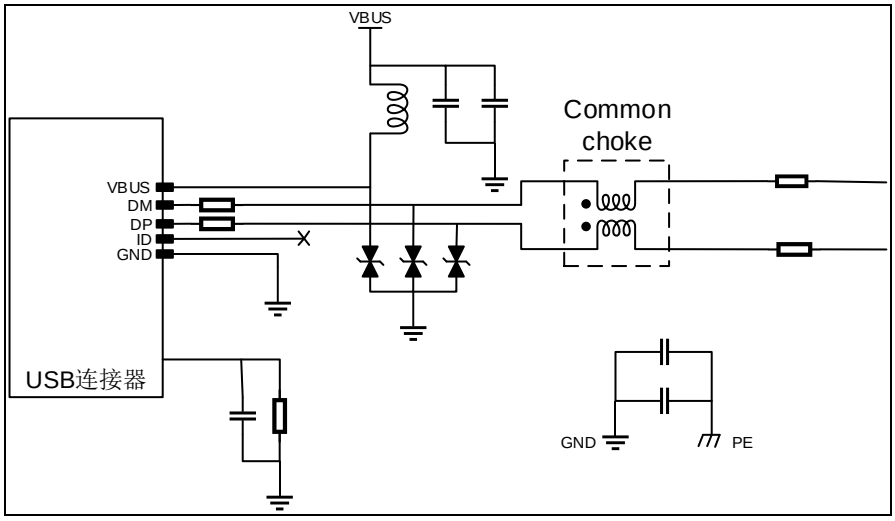
5. USB interface protection design

The USB interface is widely used in various external devices, which is characterized by high transmission speed, support for hot swapping, and multi-device connection. Some models of GD MCU support the USB function. The currently supported version of the USB function is USB 2.0, which is divided into Full Speed and High Speed types according to different transmission speeds. USB interfaces are usually used for data transmission between external devices and the host, and are often located on the edge of the PCB. USB interfaces are also reserved on the housing of the whole device. USB interfaces are likely to be subject to electrostatic interference due to their application characteristics. In many cases, electrostatic interference problems are introduced into the PCB through the USB interfaces, resulting in product resets, crashes, or other functional abnormalities. Therefore, the anti-static design of USB interfaces needs to be introduced in the circuit design stage of the product to improve its anti-static interference capability.

5.1. USB interface circuit design

USB 2.0 interfaces usually include four lines: VBUS, DM, DP, and GND, and those that support the OTG protocol also include the ID signal line. The four lines VUSB, DM, DP, and GND in common product designs are sufficient to meet most application scenarios. The reference circuit design of USB interfaces is as shown in ***Figure 5-1. USB communication interface circuit diagram***.

Figure 5-1. USB communication interface circuit diagram

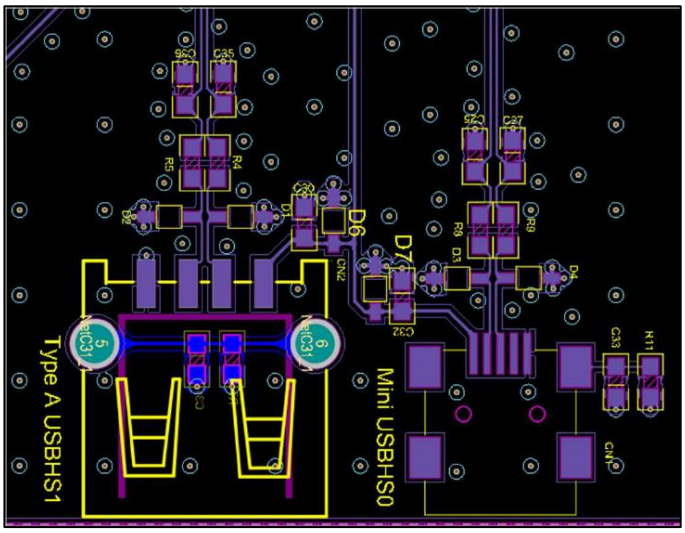


The ESD protection of USB interfaces is mainly designed into two parts: the power and signal lines of USB interfaces, and the grounding and protection of the metal housing. For the anti-static design of DP, DM, and VBUS, the key point is to add suitable TVS components, whose transient high-voltage pulse suppression capability can discharge the ESD interference to the GND circuit as early as possible. For USB circuits, users can also refer to the ESD protection by using diode arrays in the CAN protection circuit.

USB interfaces are usually located at the edge of the PCB and are susceptible to electrostatic interference. During the use of TVS, try to place the TVS as close to the interfaces as possible, so that the electrostatic interference can be discharged to the GND in the minimum circuit area, as a too large discharge circuit area can affect more components. When a PCB is affected by electrostatic interference, it not only carries energy through its wiring, but also emits waveforms with rise times in the nanosecond range during ESD events. Additionally, the impedance of PCB components and wiring often undergoes sudden changes, leading to the release of some energy in the form of radiation across a broad frequency spectrum. This may cause more complex problems. For the PCB layout of USB circuits and TVS, refer to ***Figure 5-2. USB interface circuit layout*** for the design. There are some key points that require special attention.

- When selecting a TVS model, in addition to considering the clamping voltage of the TVS, pay attention to the capacitance of the TVS junction capacitor, which is generally required to be less than 4 pF.
- It is essential to design differential pairs with equal lengths to ensure matching line lengths during PCB wiring. Failure to do so can result in timing offset, reduced signal quality, and increased EMI.
- The spacing between differential pairs should be as short as possible to maintain tight coupling. Usually, the spacing needs to be less than 10 mm. In addition, the wiring distance between other signal lines and differential pairs should be increased, and the VBUS wiring also needs to be kept as far away from the differential pairs as possible.
- The coupling between differential signal lines affects the external impedance of the signal lines, and terminating resistors must be used to achieve maximum matching of the differential transmission lines.
- Differential line wiring should steer clear of 90° angles and arcs. It is recommended to use 45° wide-angle bends or curved wiring to minimize impedance variations in the wiring and reduce signal reflections.
- In the HS mode, a characteristic impedance of 90 ohm is recommended to be designed for the PCB wiring of differential pairs to improve signal integrity. Secondly, the differential pairs should be routed on the same layer whenever possible to avoid layer changes through via holes.

Figure 5-2. USB interface circuit layout



5.2. Grounding of USB interface housing

Regarding USB interface housings, our primary concern is whether they shall be grounded. In most cases, direct grounding works very well. However, when the interference is large, it is recommended to ground the housing through a resistor-capacitor network. There are three main grounding methods: ungrounded and suspended, directly grounded, and grounded through a 100 k to 1 M resistor and a 0.1 uF or 1 uF capacitor.

Without ESD interference, all three methods can function properly. However, our primary concern is identifying the most suitable method in the presence of ESD interference.

It is generally not advisable to leave the USB interface housing directly ungrounded and suspended. For SMD-packaged USB connectors, relying solely on the welding of four pins for grounding without grounding the housing positioning pins may result in an insecure connection that could lead to detachment during use. In contrast, through-hole packaged USB connectors are less likely to detach. When USB interfaces in this form are subject to ESD interference, flashover can occur in the network near the housing grounding pad, resulting in secondary ESD interference.

The second and third grounding methods are commonly used during interface design, and the third method is generally recommended. The third grounding method has a certain buffering effect on ESD, thus reducing the level fluctuation of GND. For devices connected to the ground, the second grounding method can be employed. In the design phase, it is crucial to keep the ESD discharge path after USB grounding as close to the ground as possible. To prevent ESD energy from permeating the entire PCB and causing an expanded interference range, it is advisable to avoid positioning the power ground and USB ground on opposite sides of the PCB. The ideal design method is that the ESD discharge GND of the USB housing and the power ground interface of the PCB are on the same side of the PCB or close to each other.

The third method is recommended for battery-powered floating devices. Battery-powered floating devices discharge ESD much slower than grounded devices. The electrostatic energy injected into the devices by ESD will remain on the PCB for a period of time and then slowly dissipate. The accumulation of charges causes potential shift and secondary discharge problems. Issues such as MCU resets or crashes are often caused by rapid transient voltage fluctuations. Using the third method can serve as a buffer. In this method, users have the option to exclude capacitors and retain only resistors. If capacitors are used, it is advisable to opt for high-voltage tolerant capacitors. Secondly, the secondary discharge of charges accumulated on the PCB also causes MCU reset and crash problems. During the test, when the device under test is placed on the horizontal coupling plate, excessive charge accumulation can cause the PCB to discharge to the horizontal coupling plate, resulting in secondary discharge. Therefore, appropriate protection measures are necessary for areas with a high risk of secondary discharge. If the testing requirements are met, after each ESD event during testing, discharge the charged PCB using a grounding brush, and then proceed to the second round of testing.

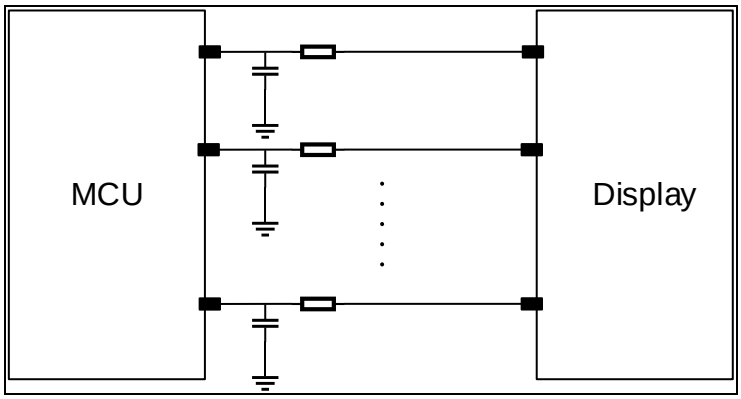
6. Display protection design

The application of LCD display in embedded systems provides users with an interactive interface. MCU, as a commonly used control IC in embedded systems, is often used as a display controller. There are various types of LCD screens. Currently, the commonly used LCD screens have integrated drive circuits. The external MCU is used as a controller to control the data refresh of the display to realize the display and switching of the screen. LCD screens and MCUs are connected through pin headers or FPCs. The interfaces of LCD screens usually include data lines, address lines, control signal lines, etc., and transmit signals through I2C, SPI, and other methods. Some LCD screens realize time division multiplexing of control signals and data directly through I2C and SPI serial ports to provide the display function. Because the LCD screen needs to refresh data at a certain refresh rate during normal operation, as the amount of data increases, the refresh rate is also constantly increasing, thus causing EMI radiation, posing a significant concern in product applications.

The EMI radiation sources of LCD screen are usually display screen FPCs, PCB wiring, etc. Take protective measures including filtering and shielding to address the out-of-limit EMI radiation problem of the display screens. RC filter or magnetic bead filter is usually used, as shown in ***Figure 6-1. LCD interface filter circuit diagram***. Because the frequency point where EMI radiation is out of limit is unpredictable at the beginning of the design, the design of filters generally needs to be adjusted based on the specific product requirements. It is recommended to reserve a position for RC filter in advance. During PCB mounting, it is recommended that the cut-off frequency of the RC filter be not lower than 5 times the actual signal frequency, so as to prevent the low-frequency harmonics that constitute the signal from excessive attenuation due to a too low cut-off frequency, which may affect the actual communication function. The preset cut-off frequency may not be suitable for the final test effect. In this case, it needs to be adjusted based on the test results.

The bandwidth of the RC filter is determined by the cut-off frequency and is a wide-band filter. When EMI radiation is out of limit at certain frequency points, users can retain the filter capacitors only, and match the resonance points of the capacitors and the out-of-limit frequency points to achieve narrow-band filtering. The filtering effectiveness of capacitors is closely linked to the signal return impedance of the capacitors. In actual product manufacturing, cost considerations often lead to the use of two-layer boards. Maintaining a solid ground connection can be challenging when components and wires are densely packed. In such scenarios, using RC filters or single-capacitor filters may result in the filtered frequency components causing high impedance on the ground return path, thereby failing to achieve the desired filtering outcome. In this case, magnetic bead filters can be used to occupy the original resistor positions for filtering. Magnetic bead filters are also narrow-band filters. Different from capacitive filters, the high impedance of magnetic bead filters at a specific frequency point can convert the internal field energy of the magnetic bead filters into heat for dissipation.

Figure 6-1. LCD interface filter circuit diagram



Generally speaking, the filters can reduce the radiation energy. However, when the radiation energy is high, the filtering method alone does not have a good effect. In this case, the shielding method can be used to reduce the radiation of the product. A commonly used radiation shielding method is to paste conductive tapes on the FPC of the LCD display screen, and connect the conductive tapes to the GND of the PCB to form a shield, as shown in ***Figure 6-2. Shielding of FPC radiation by conductive tapes***. For an LCD display screen with a metal backplate, the metal plate of the backplate can overlapped with the GND of the PCB through conductive foam, as shown in ***Figure 6-3. Shielding structure of LCD metal plate***. Through such a structural design, a shielding effect can be achieved with the help of the LCD metal backplate to shield the components and wiring within the LCD display screen coverage.

Figure 6-2. Shielding of FPC radiation by conductive tapes

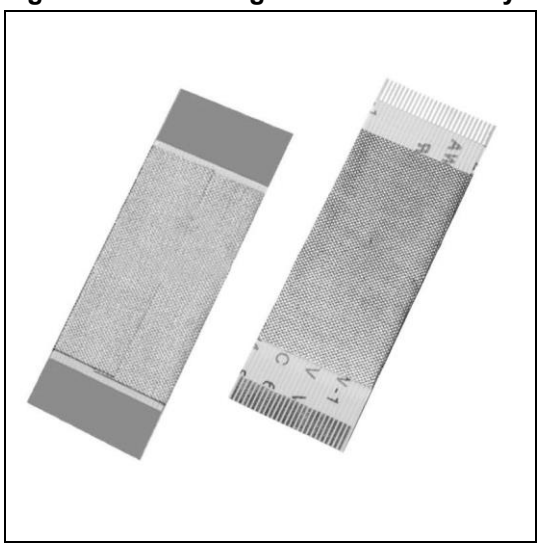
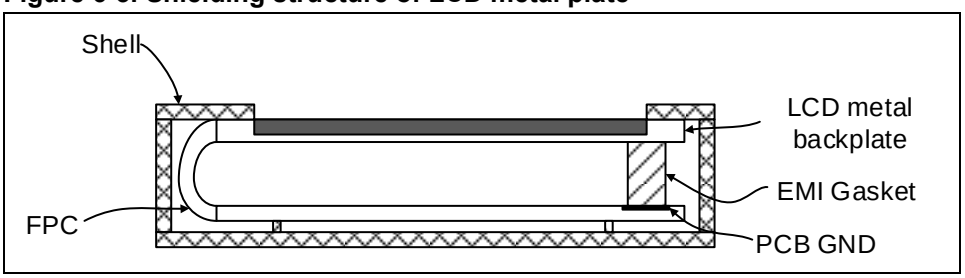
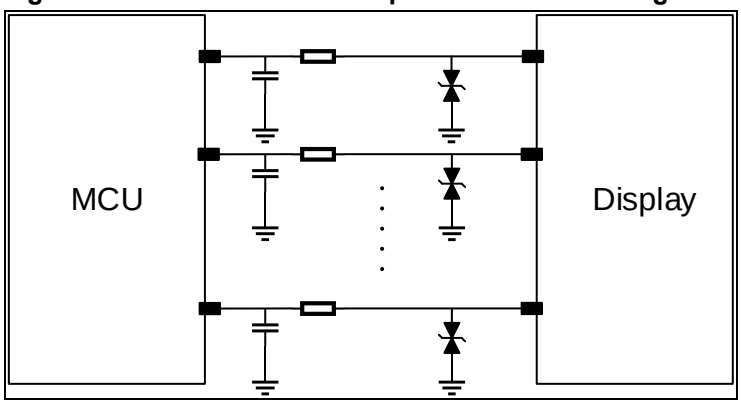


Figure 6-3. Shielding structure of LCD metal plate



During actual EMC testing, in addition to RE radiation testing, ESD immunity testing is also very important. Because the formed product has a complete package, the discharge points during ESD testing are usually the function buttons, display screen body, and frame that match the display screen. Various types of LCD screens are used based on factors such as the positioning and cost of the product. Common types include plastic casing, metal frame, and all-metal backplate, etc. During ESD testing, static electricity can build up on the casing of the LCD display screen with a plastic backplate, leading to secondary discharge issues. This can potentially interfere with the FPC of the display and the wiring on the PCB. Therefore, ESD protection is required for the display screen interface wiring, including the addition of TVS for transient high voltage suppression, as illustrated in ***Figure 6-4. LCD interface ESD protection circuit diagram***.

Figure 6-4. LCD interface ESD protection circuit diagram



During ESD testing, in addition to the above problems, LCD screens with metal frame and backplate can cause radiation problems. The metal frame and backplate radiate part of the electrostatic energy during the electrostatic injection. In this case, if the wiring on the PCB and the radiated electromagnetic frequency band generate an antenna receiving effect, it will also cause abnormal system functions. In this case, users can connect the metal frame or backplate to the GND of the PCB to reduce the radiation effect. At the same time, pay attention to the location of the connection point, and try to choose a location near the GND of the power supply port to reduce the impedance during the interference discharge. Secondly, the wiring on the PCB needs to be optimized to minimize the signal return path. If it is difficult to optimize the wiring on the PCB, capacitors can be connected in parallel on the wiring that generates the antenna effect to improve this problem.

7. HXTAL anti-interference design

When the MCU uses an external high-speed passive crystal oscillator as the clock signal source, there are two main aspects to consider for the anti-interference performance of the clock. The first aspect is to choose a suitable passive crystal so that it can oscillate in a suitable amplitude range after working with the MCU; the second aspect is that if the wiring in the PCB layout of the crystal oscillator circuit is not handled properly, it is susceptible to external interference.

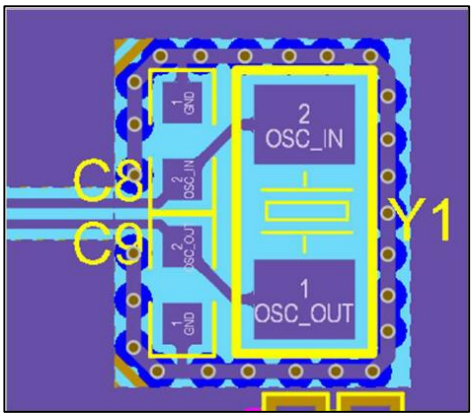
7.1. HXTAL amplitude range

For passive crystal oscillators, the amplitude of oscillation is related to the drive capability of the drive circuit inside the MCU, while the drive capability of the MCU for HXTAL is fixed and cannot be adjusted. Secondly, the amplitude in the passive crystal oscillator mode also depends on the parameters of the crystal oscillator itself (ESR), the capacitance on the board, and whether there are amplitude limiting resistors, etc. Usually, when the oscillation can start and reach a certain amplitude, the chip amplifies and shapes the waveform on the OSCIN/OUT pin into a full-amplitude square wave. In practice, oscillators exhibit higher stability when the amplitude exceeds 0.5V.

7.2. Notes on HXTAL layout

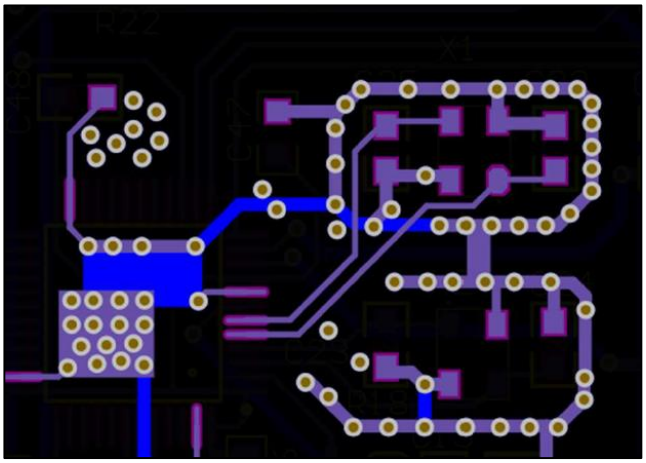
For the PCB layout design of HXTAL, the general rule is that the OSCIN and OSCOUT wirings of the crystal oscillators should be as short as possible and keep the same length; secondly, appropriate shielding with ground wires can shield interference for HXTAL. When shielding with ground wires, be careful not to connect the ground loop directly to the GND of the MCU and try not to form a closed loop. ***Figure 7-1. Recommended crystal oscillator layout*** shows a recommended HXTAL layout method. In this layout design, the shielding loop of HXTAL is connected to the bottom layer through via holes, and the top layer is segmented to import interference signals that may be generated during HXTAL oscillation into the bottom GND through the ground loop, thereby minimizing the impact of interference on the top GND.

Figure 7-1. Recommended crystal oscillator layout



As shown in ***Figure 7-2. Crystal oscillator layout not recommended***, in the wrong layout design, the ground loop of the crystal oscillators and the analog ground VSSA of the MCU are connected to form a closed loop. This processing method is susceptible to interference signals during the EMC anti-interference test. For example, in the RS test, it is susceptible to RF interference signals, thus causing fluctuations in VSSA. Therefore, this phenomenon needs to be avoided in the design. For details on the selection of passive crystal oscillators and circuit design, please refer to the released application note ***AN052 GD32 MCU Resonator-Based Clock Circuit***.

Figure 7-2. Crystal oscillator layout not recommended



8. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial release	February 4, 2024

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