GigaDevice Semiconductor Inc.

Device Limitations of GD32E235

Errata Sheet

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1. Introduction

This document applies to GD32E235 product series, as shown in ***Table 1-1. Applicable products***. It offers technical guidance for using GD32MCU and provides workaround to current device limitations.

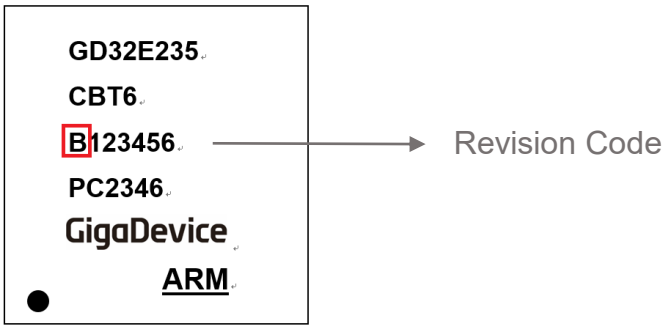
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32E235xx series

1.1. Revision identification

The device revision can be identified according to the mark on the top of the package. The 1st code on Line 3 of the mark is the product revision code, as shown in ***Figure 1-1. Device revision code of GD32E235***.

Figure 1-1. Device revision code of GD32E235



1.2. Summary of device limitations

The device limitations of GD32E235 are shown in ***Table 1-2. Device limitations***, please refer to Section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code B
RCU	*System operation fails due to system clock switching from high clock frequency to low clock frequency*	Y

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. RCU

2.1.1. System operation fails due to system clock switching from high clock frequency to low clock frequency

Description & impact

System operation fails when system clock switching from high clock frequency to low clock frequency.

Workarounds

Firstly, reduce the system frequency (such as HCLK / 2 or HCLK / 4); secondly, delay more than 20 HCLK clock; finally, switch to the low clock frequency. For reference, see the RCU_MODIFY macro in the system_gd32e23x.c file of the firmware library. The RCU_MODIFY reference code is as follow:

```
#define RCU_MODIFY(__delay)     do{                                         \
                                    volatile uint32_t i;                    \
                                    if(0 != __delay){                       \
                                        RCU_CFG0 |= RCU_AHB_CKSYS_DIV2; \
                                        for(i=0; i<__delay; i++){           \
                                        }                                   \
                                        RCU_CFG0 |= RCU_AHB_CKSYS_DIV4; \
                                        for(i=0; i<__delay; i++){           \
                                        }                                   \
                                    }                                       \
                                }while(0)
```

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.27, 2024
1.1	Update the workarounds of RCU limitation, refer to ***System operation fails due to system clock switching from high clock frequency to low clock frequency***	Sep.1, 2024

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