GigaDevice Semiconductor Inc.

Migration from GD32F4xx series to GD32F5xx series

Application Notes
AN194

Revision 1.0

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1. Foreword

Designers working with GD32 series MCUs often need to replace one microcontroller with another to meet the requirements of their products. To accelerate the launch of new products, designers often need to port applications to new MCUs.

This application note aims to help you port your applications from GD32F4xx MCU to GD32F5xx MCU.

The GD32F5xx series, a new Cortex®-M33 series introduced by GD in 2024, is highly compatible with the GD32F4xx series, which belongs to GD's Cortex®-M4 series. If there are requirements for porting from GD32F4 series to GD32F5xx series during use, this document introduces in detail how to port the existing code of GD32F4xx series to the GD32F5xx series.

To make better use of the information in the application notes, you need to have a deep understanding of GD32 MCUs. You can download the data of various series of GD32 MCUs, such as Datasheet, user manual, Firmware Library, and various development tools from GigaDevice's data website: https://www.gd32mcu.com/ or network disk: https://pan.baidu.com/s/1mhQsNpu.

2. Pin compatibility

The package types of the GD32F5xx series currently include: LQFP64, LQFP100, LQFP144, LQFP176, and BGA208.

The package types of the GD32F4xx series include: LQFP64, LQFP100, LQFP144, BGA100, and BGA176.

The pin packaging function of GD32F5xx can completely cover the product pin functions of GD32F4xx series.

3. Internal resource compatibility

The following table provides an overview of the resource comparison between GD32F4xx and GD32F5xx

(taking the comparison between GD32F470IK and GD32F527IS as an example):

Table 3-1. Overview of internal resource comparison between GD32F470IK and GD32F527IS series

On-chip resources	GD32F470IK	GD32F527IS	Compatibility description
Clock frequency	240MHz	200MHz	\
Core	M4 core	M33 core	Compatible and enhanced
Flash	3M	6M	Compatible and enhanced
Code	1M	2M	Compatible and enhanced
RAM	256K	512K	Compatible and enhanced
GPTM	8+2	8+2	Compatible
Advanced TM	2	2	Compatible and enhanced
Basic TM	2	2	Compatible
Systick	1	1	Compatible
Watch dog	2	2	Compatible
RTC	1	1	Compatible
USART	4	4	Compatible
UART	4	4	Compatible
I2C	3	6	Compatible and new
SPI/IIS	6/2	6/2	Compatible
SDIO	1	1	Compatible
CAN	2	2*CAN FD	Compatible and enhanced
USB	FS+HS	FS+HS	Compatible
ENET	1	1	Compatible
TLI	1	1	Compatible
DCI	1	1	Compatible
SAI	\	1	New
EXMC/SDRAM	1/1	1/1	Compatible
IAP	\	1	New
CAU	\	1	New
HAU	\	1	New

On-chip resources	GD32F470IK	GD32F527IS	Compatibility description
TRNG	\	1	New
PKCAU	\	1	New
ADC(CH)	3(24)	3(24)	Compatible
DAC	2	2	Compatible
GPIO	140	140	Compatible

4. Program porting

According to the previous section, GD32F5xx and GD32F4xx are compatible in basic functions, and the main functional differences lie in some new peripheral functions in GD32F5xx and the enhancement of some functions.

Note: GD32F5xx adopts the Cortex®-M33 core architecture, which requires Keil 5.25 or newer versions (V6 compiler) and IAR 8.1 or newer versions during development.

Table 4-1. IDE support for GD32F5xx

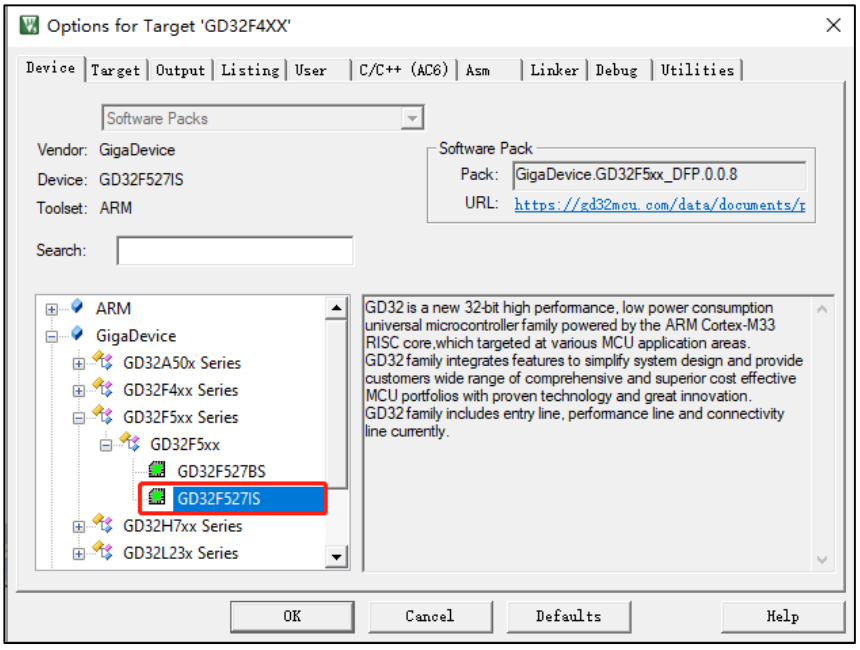
Chip series	GD32F4xx	GD32F5xx
Keil	Keil4 and Keil5	Keil 5.25 or newer versions
IAR	IAR 6.3 or newer versions	IAR 8.1 or newer versions

4.1. Direct replacement

If you do not add functions (the original library does not involve Flash operations), you can continue using the firmware library of GD32F4xx for modification and development. To download, you can call the download algorithm file of GD32F5xx for simulation download and increase the size of the project FLASH file in the configuration:

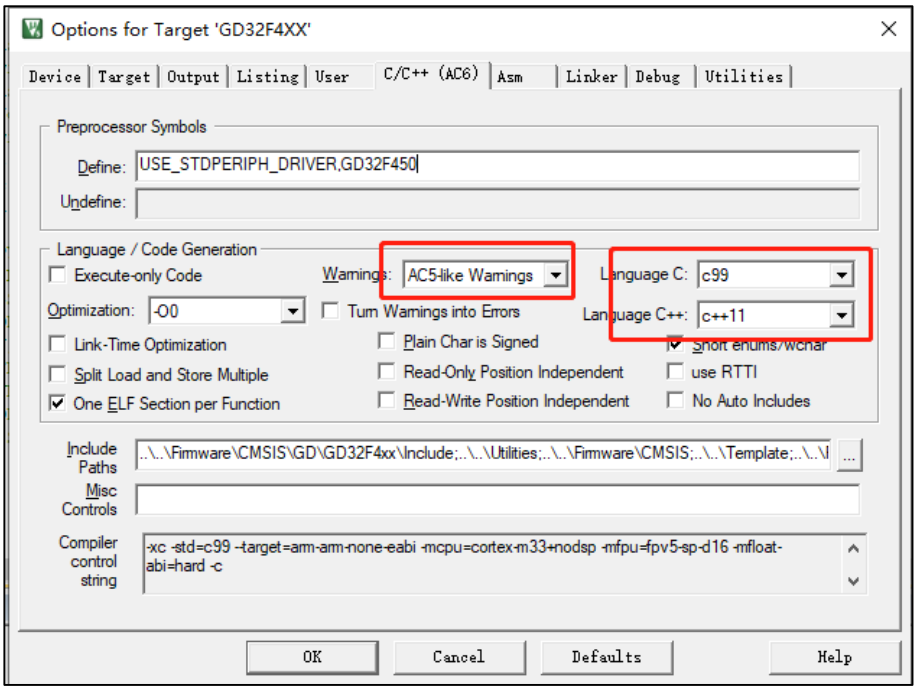
- Open the Option for Target, and change the Device to the model corresponding to GD32F5xx.

Figure 4-1. Device configuration



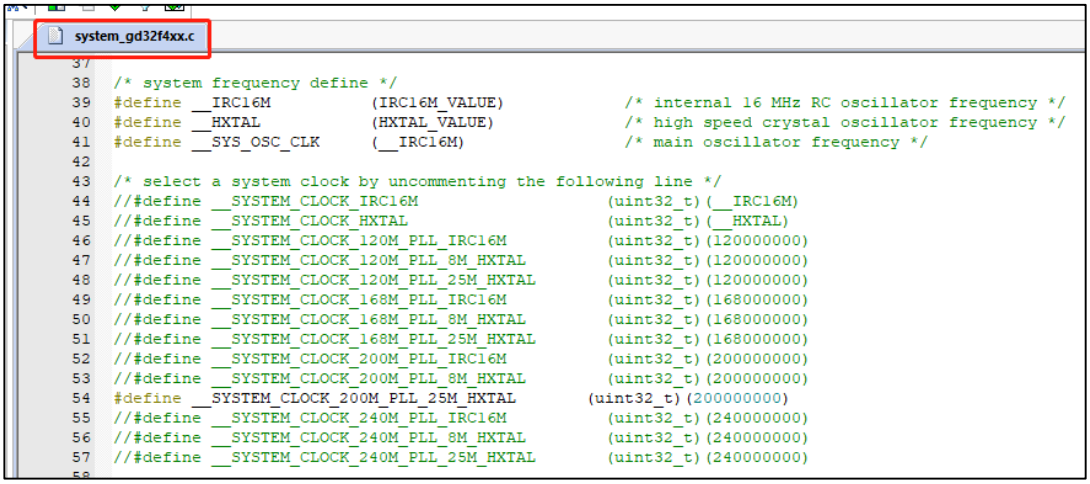
- On the C/C++ tab, modify the C99 version and C++11 version, and modify AC5-like Warnings.

Figure 4-2. C/C++ tab



- Modify the maximum clock frequency (up to 200M) and the configuration of timer and other clocks in the program to perform compilation, simulation, and operation.

Figure 4-3. Modification of the maximum clock frequency



- If the Flash operation is used, modify "Flash erase" in the program to "page erase".

Figure 4-4. Flash page erase function

```
/*!
    \brief      FMC erase page
    \param[in]  page_addr: the page address to be erased.
    \param[out] none
    \retval     state of FMC
      \arg        FMC_READY: the operation has been completed
      \arg        FMC_BUSY: the operation is in progress
      \arg        FMC_RDDERR: read D-bus protection error
      \arg        FMC_PGSERR: program sequence error
      \arg        FMC_PGMERR: program size not match error
      \arg        FMC_WPERR: erase/program protection error
      \arg        FMC_OPERR: operation error
      \arg        FMC_TOERR: timeout error
*/
fmc_state_enum fmc_page_erase(uint32_t page_addr)
{
    fmc_state_enum fmc_state = FMC_READY;

    /* wait for the FMC ready */
    fmc_state = fmc_ready_wait(FMC_TIMEOUT_COUNT);

    if(FMC_READY == fmc_state) {
        /* unlock page erase operation */
        FMC_PEKEY = UNLOCK_PE_KEY;

        /* start page erase */
        FMC_PECFG = FMC_PE_EN | page_addr;
        FMC_CTL &= ~FMC_CTL_SN;
        FMC_CTL |= FMC_CTL_SER;
        FMC_CTL |= FMC_CTL_START;
```

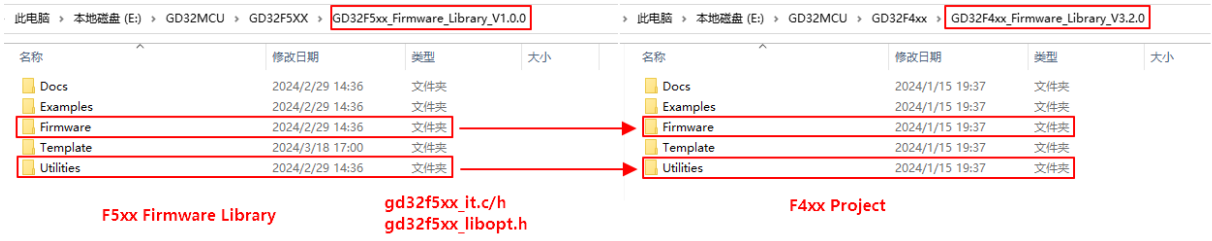
4.2. Library replacement

To make better use of the functional applications of GD32F5xx and add new functions to the program, the underlying driver library needs to be replaced. Because the underlying driver function APIs of the GD32 compatible series are basically the same, you can directly download the latest GD32F5xx firmware library from the official website (http://www.gd32mcu.com/cn/download?kw=), and replace the old one with it in the original GD32F4xx project directory. As shown in the figure below, move all the content in the Firmware folder of the GD32F5xx firmware library to the target project directory.

At the same time, add the interruption service function and gd32f5xx_libopt.h (header file inclusion file) of the original GD32F4xx project to the gd32f5xx_it.c/.h file for replacement.

Note: There are differences in clock frequency of chip, vector table offset, and some macros.

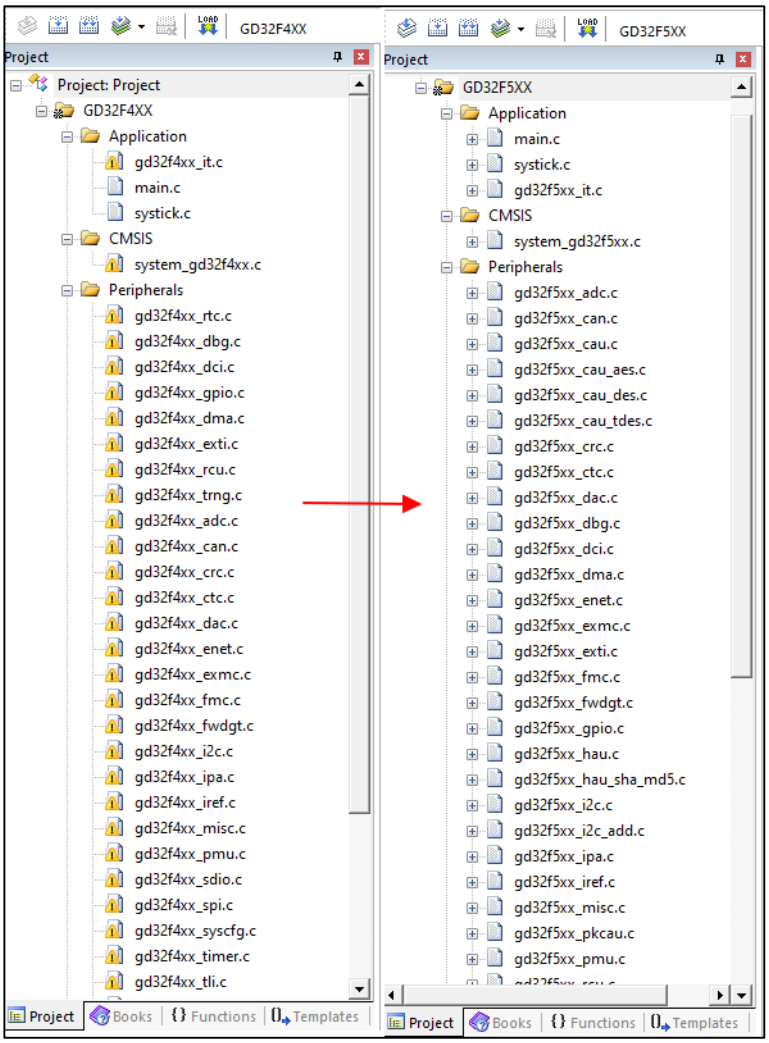
Figure 4-5. Replacement of underlying firmware



After replacement, reopen the project, delete the corresponding warning file, and add the new

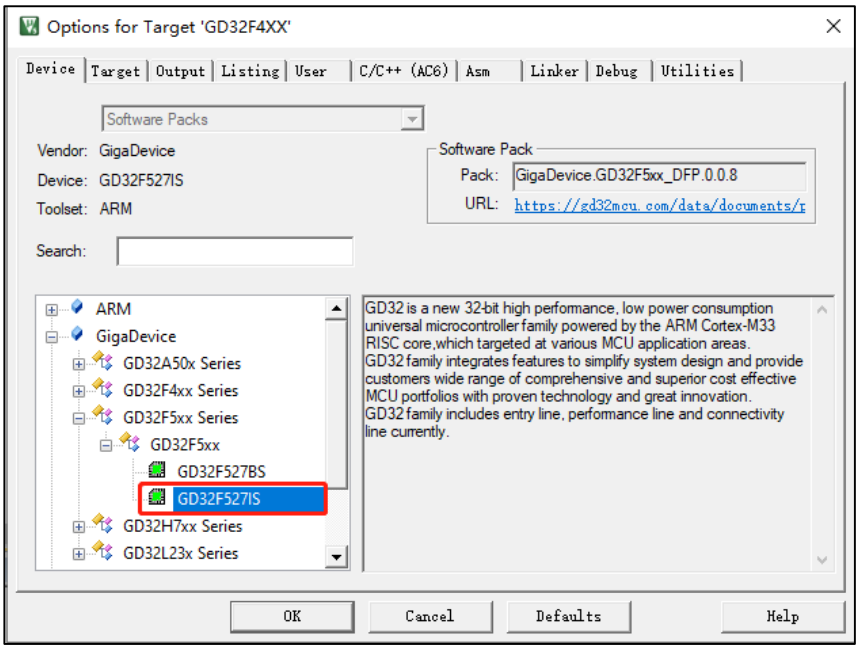
GD32F5xx underlying firmware content under the replaced firmware library. Including: clock initialization.c, firmware content.c, startup file.s, interrupt service function.c, etc.

Figure 4-6. Replacement of files in the IDE



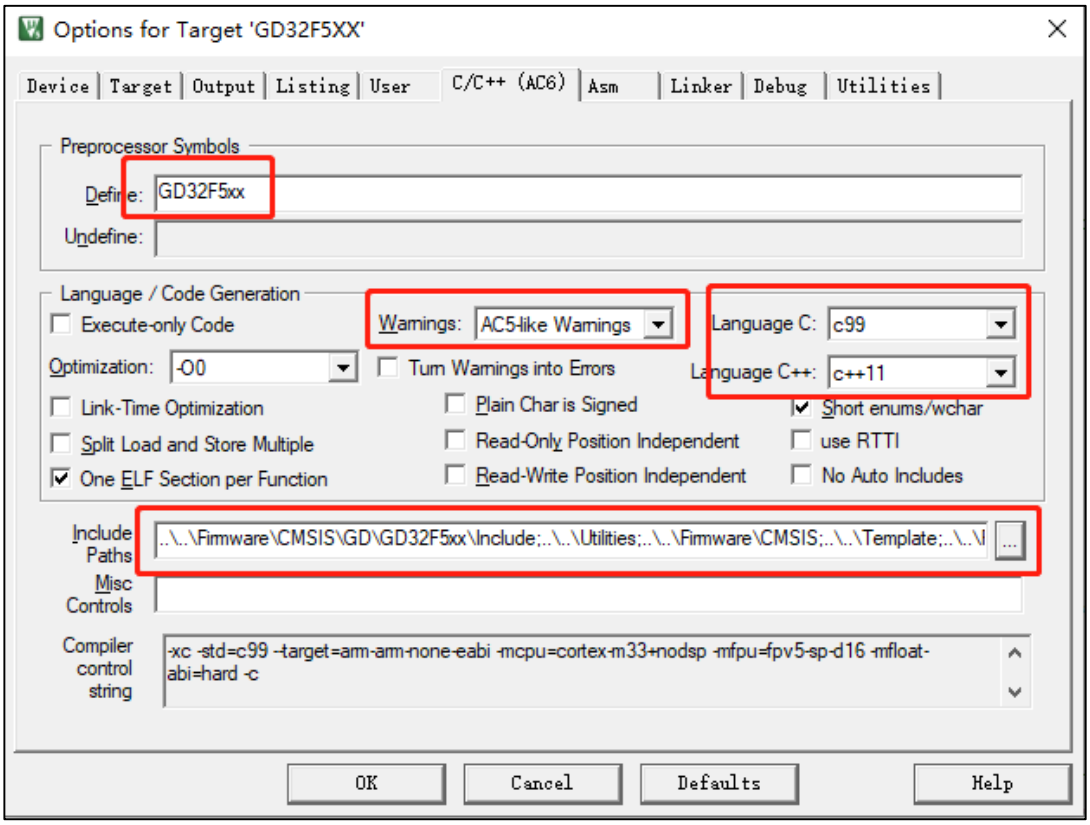
Open the Option for Target, and change the Device to the model corresponding to GD32F5xx.

Figure 4-7. Modification of Device model



On the C/C++ tab, modify the corresponding macros, and add the corresponding header file path again. Modify the C99 version and C++11 version, and modify AC5-like Warnings.

Figure 4-8. Modification of C/C++ tab



Finally, search for the header file inclusion names of GD32F4xx in the project, and modify all of them to the header files of GD32F5xx. Adjust the corresponding clock frequency in the system_gd32f5xx.c code. The compilation can be performed normally, and downloading and

debugging can be carried out later.

If some macros cannot be found, GD32F5xx may be named or used differently. You can find the corresponding macros or similar application macros and modify them.

Figure 4-9. Replacement of corresponding header files

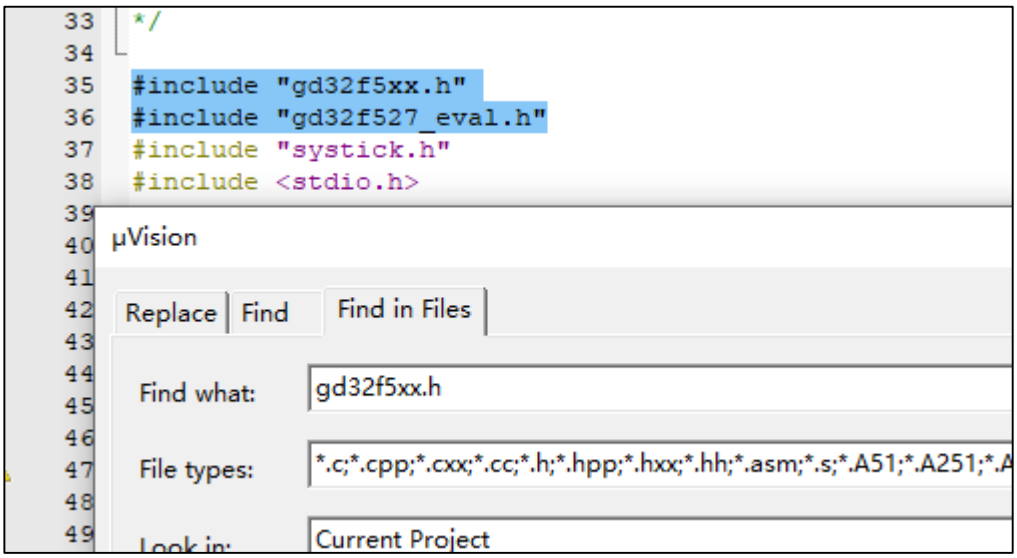
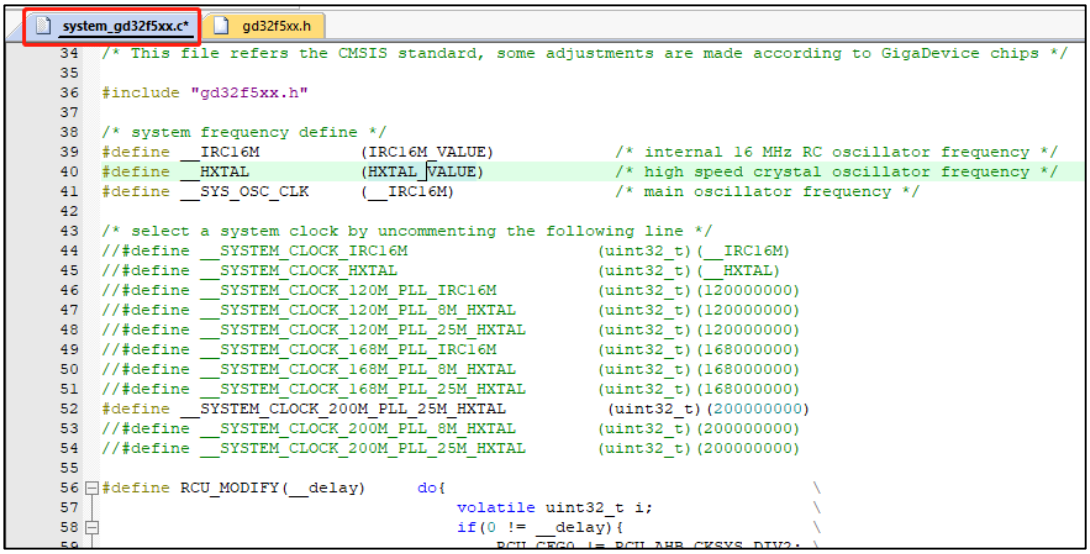


Figure 4-10. Modification of clock frequency



5. Differences of peripheral devices

GD32F5xx and GD32F4xx are mostly compatible in terms of peripherals, but as a more advanced MCU, GD32F5xx has many more new functions in terms of functional safety than GD32F4xx.

The following lists the new peripheral functions of GD32F5xx.

5.1. FMC

There are big differences in FMC between GD32F5xx and GD32F4xx, mainly around function expansion and new functions:

- TCMSRAM: 64 KB;
- SRAM ECC: 512 KB - 1 MB;
- CodeFlash ECC: 1 MB - 2 MB;
- DFlash ECC: Up to 5.5 MB;

GD32F5xx whose main flash memory capacity is no more than 7680 KB contains up to eight 16 KB sectors, two 64 KB sectors, thirty 128 KB sectors, and fourteen 256 KB sectors. Each sector of the main flash memory can be erased separately. The flash memory structure is divided into 4 MB dual blocks, 2 MB dual blocks, 1 MB single block, and 512 KB single block. Each structure has Bank1 extended flash memory (Bank1_Ex).

Note: The extended flash memory address of Bank1_Ex always starts from 0x08400000. For small-capacity GD32F5xx, the Bank1_Ex address may be discontinuous.

- ECC supports single-bit error correction and double-bit error detection.
- Add support for 64-bit double-word programming.
- Provide 64-byte OTP0 blocks for storing user data, and add 128 KB OTP1 and 128 KB OTP2.

The OTP1 area can be used for secure boot of the program, and with the key stored in OTP2, the execution redirects to the APP code.

- For one-time programmable non-volatile EFUSE memory cells, no bits can be rolled back from 1 to 0.

EFUSE can work with OTP1&OTP2 to perform secure boot of the fixed address.

- Code area loading

FMC_CTL register BIT29 NWLDE can be modified: Enable and disable the loading of zero wait area after system resetting (reset values are restored only after power supply reset).

- Option byte.

Add USER BIT1 ECCEN to enable or disable ECC.

Add WP0 BIT 5 NWA and select the zero wait area. You can select Bank0 or Bank1 as the zero wait code area (this bit only takes effect after power supply reset for the 4 MB dual-block series).

5.2. System security

GD32F5xx is enhanced in security levels:

- Multi-level code and data protection (OTP0/1/2)

OTP1 128 KB, user-trusted root code area. Block Read/Write Lock: After the trusted root code is read by the CPU and redirection is executed, the area is locked and cannot be read or executed by the APP.
OTP2 512 Byte, key protection area, and Area Read/Write Lock: Some data is locked and cannot be read by the APP after the trusted code is executed, while certain data can be read by the App.

- User secure storage

Read protection: None/Low Level/High Level.

Write and erase protection: The option bytes are configured with Sector erase and write protection.

The core comes with MPU User/Priv mode to control resource access.

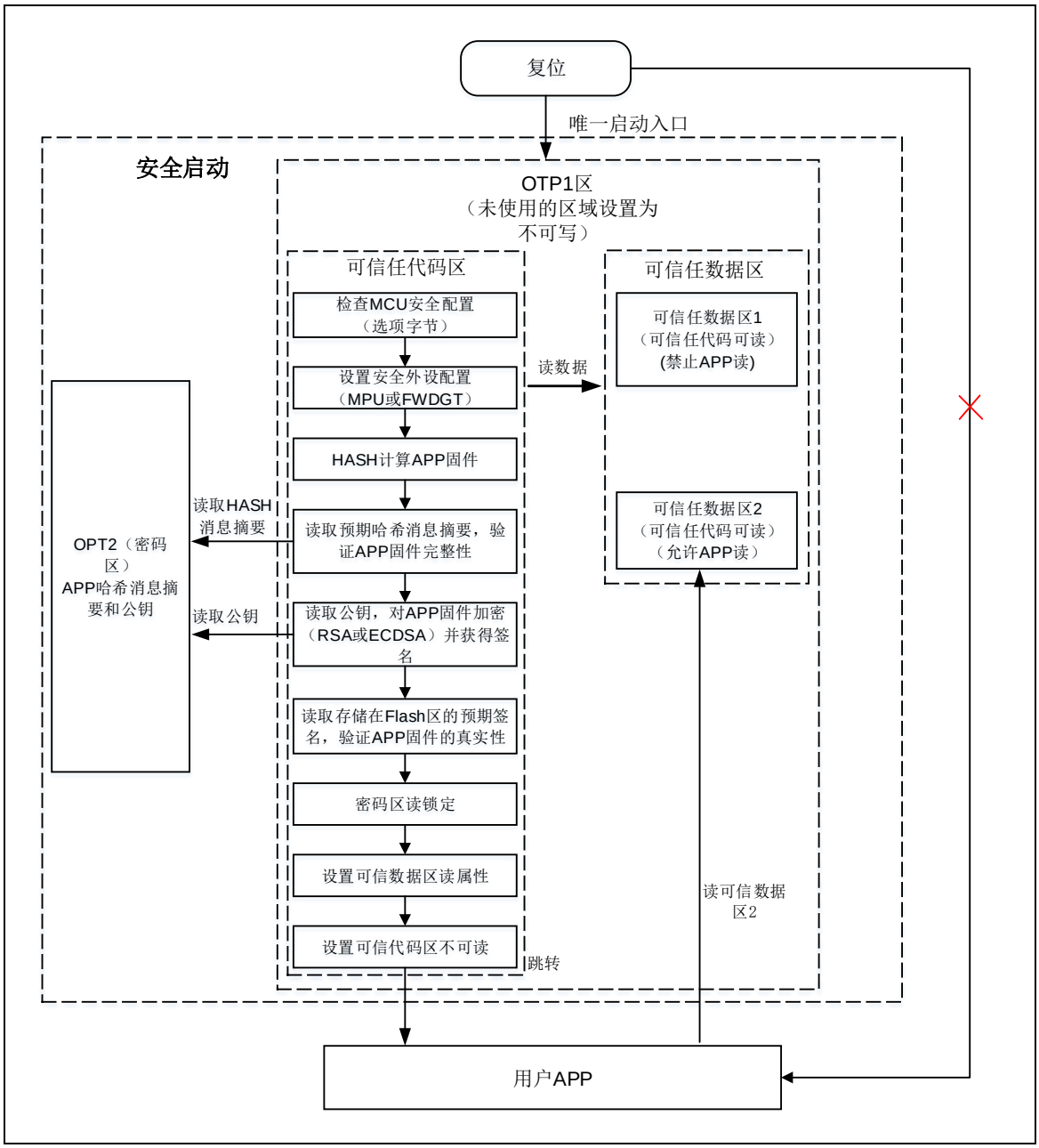
- Boot protection

Unique entrance protection, EFUSE configuration, and Flash/OTP1 trusted root code area boot.

In the OTP1 secure and trusted root code area, check the correctness of system configuration and verify the integrity and legality of subsequent Apps. (SHA1/224/256, ECC640, and RSA3136) Hash summary information, shared key OTP2 area, and APP firmware signature are stored in Flash after each update.

Secure boot is executed before the user App firmware when the MCU is reset, and it provides the security functions in the initial stage. You can store user-level secure boot in the OTP1 area, and then set the OTP1 area as the unique boot entry for the MCU. Every time the MCU is reset, it must boot in the secure boot mode.

Figure 5-1. Secure boot flow chart



- Secure debugging

SPC sets the security level. The code area can only be executed, and the code cannot be accessed through the debug interface. However, the registers can still be accessed through the debugger.

EFUSE BIT permanently disables the debug interface.

- Security upgrades

OTA: A bank is executed, B bank is upgraded, written in, and swapped after successful verification. Verify the firmware version to prevent rollback.

- Hardware encryption algorithm & random number;

SHA-1, SHA-224, and SHA256 supported.

AES128 and 256 supported.

TRNG supported - NIST sp800-22 satisfied

- UID: Each chip has an independent UID.

5.3. Enhanced Safety

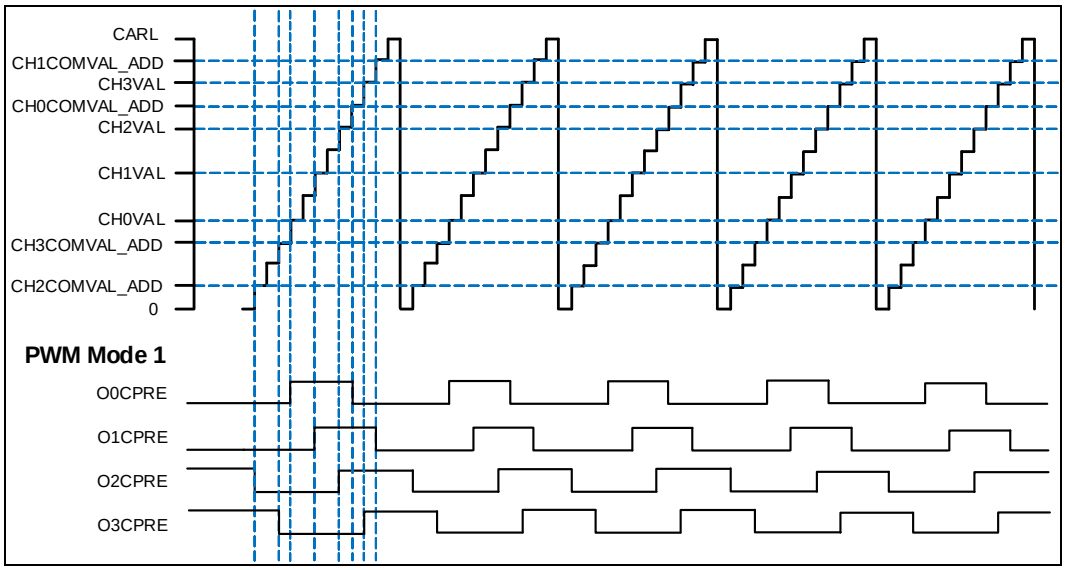
IEC61508 SIL2 supported;

Flash/SRAM ECC supported.

5.4. TIMER

GD32F5xx adds the composite PWM mode to the advanced TIMER, and adds two comparison points for frequency conversion and phase shift to change the duty cycle. Four pairs of complementary outputs are added to enhance the flexibility of control.

Figure 5-2. Composite PWM output



5.5. CAN

The GD32F4xx series provides the CAN2.0 function. The GD32F5xx series provides the 2*CAN-FD function and is compatible with the CAN2.0 function. The maximum baud rate for CAN-FD frame communication is 6 Mbit/s, and it supports a transmission delay compensation mechanism. For detailed information about its specific functions and register configurations, please refer to the GD32F5xx User Manual.

5.6. I2C

GD32F5xx introduces new I2C interfaces, namely I2C3, I2C4, and I2C5. These interfaces have the same basic features as I2C0, I2C1, and I2C2, with additional functionalities. Some of the key features include support for multiple 7-bit slave addresses, programmable setup time and holding time, compatibility with SMBus 3.0 and PMBus 1.3 standards, optional PEC (message error check) production and verification, the ability to wake up from sleep mode and deep sleep mode when an address is matched, and an independent clock source separate from PCLK.

6. Revision history

Table 6-1. Revision history

Revision No.	Description	Date
1.0	Initial release	April 10, 2024

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