GigaDevice Semiconductor Inc.

GD32A503/A513 Series Two-bit ECC Error Description

Application Note
AN175

Revision 1.0

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Table of Contents

List of Figures

List of Tables

1. Introduction

During the write operation, the encoder generates an ECC code that is written to the storage unit along with the data. During the read operation, the decoder parses and verifies the original data of the storage unit and the ECC code. ECC can realize the function of 1 bit error correction and two-bit error detection, and can not judge the error of more than 2 bits.

This application note introduces the common handling methods when SRAM / flash two-bit ECC error occurs.

2. NMI interrupt caused by an ECC two-bit error

After an two-bit ECC error occurs in the SRAM / Main flash / OTP, the program enters NMI interrupt. If the NMI interrupt handler does not clear the ECC flag, the NMI interrupt will continue to be triggered, which affects the debugger connection.

Suggestion: After the NMI interrupt is generated, record the ECC information, set the query flag, and clear the flag bit. In the main program, the query flag is used to determine whether an ECC error is generated, and if an error is generated, further processing will be done.

3. Scenes of two-bit ECC error

3.1. SRAM two-bit ECC error

Reading an uninitialized SRAM address may produce an two-bit ECC error due to a mismatch between the SRAM raw data and the ECC code.

Solution: The SRAM addresses that may be accessed need to be initialized before the SRAM read operation. It is recommended to initialize all the SRAM addresses in the startup file.

Figure 3-1. SRAM initialization

```
Reset_Handler   PROC
                EXPORT  Reset_Handler                   [WEAK]

                LDR     r0, =0x1FFFF7E0
                LDR     r2, [r0]
                LDR     r0, = 0xFFFF0000
                AND     r2, r2, r0
                LSR     r2, r2, #16
                LSL     r2, r2, #10
                LDR     r1, =0x20000000
                MOV     r0, #0x00
SRAM_INIT       STM     r1!, {r0}
                SUBS    r2, r2, #4
                CMP     r2, #0x00
                BNE     SRAM_INIT

                IMPORT  SystemInit
                IMPORT  __main
                LDR     R0, =SystemInit
                BLX     R0
                LDR     R0, =__main
                BX      R0
                ENDP
```

In practical applications, if not all the SRAM areas are expected to be initialized after reset, but only the addresses that the application may access. Note that the IDE software may access the SRAM when debuging, and when the IDE accesses the uninitialized SRAM address, it will trigger an ECC error.

3.2. Flash two-bit ECC error

In most cases, ECC errors are caused by low power supply, power down, or reset during operation, and there is no substantial damage to the physical storage unit. The ECCADDR[14:0] in the FMC ECCCS register records the error address. After the error address is erased, it can be used again and the original data is lost.

Table 3-1. Description of ECC error address

Error area	Error flag	Error address
Bank0	ECCDET	0x08000000 + ECCADDR[14:0] * 8
Bank1	ECCDET/BK1_ECC	0x08040000 + ECCADDR[14:0] * 8
Data flash	ECCDET/DF_ECC	0x08800000 + ECCADDR[14:0] * 8

Error area	Error flag	Error address
System area	ECCDET/SYS_ECC	0x1FFFB000 + ECCADDR[14:0] * 8
Option bytes 0 (read 0x1FFFF80x)	ECCDET/OB0_ECC	0x1FFFF800 + ECCADDR[14:0] * 8
OTP	ECCDET/OTP_ECC	0x1FFF7000 + ECCADDR[14:0] * 8
EEPROM SRAM	EPECCDET	0x08C00000 + ECCADDR[14:0] * 8
Option bytes 0	OB0ECCDET	/
Option bytes 1	OB1ECCDET	/

Note: If an two-bit ECC error occurs when loading the option byte 0 or option byte 1, ECCADDR[14:0] will not record the error address.

If the Flash is used for a long time, considering the aging failure, after erasing, programming and then read, the error is likely to be reported again, such an error address should not be used.

3.2.1. Main flash / OTP two-bit ECC error

If the ECC error occurs in the main flash / OTP, the data in the error address is returned to all F, the program will enter the NMI interrupt and process according to the NMI interrupt handling suggestion.

Note: OTP has non-erasable properties, and it is necessary to ensure the working environment to be stable when programming.

3.2.2. EEPROM two-bit ECC error

If the ECC error occurs in the EEPROM, the data in the error address is returned to all F, and the program will not enter the NMI interrupt.

The EEPROM two-bit ECC error is usually caused by power down or reset during EEPROM operation. When the EEPROM two-bit ECC error occurs, the EPECCDET will be set. When an two-bit ECC error occurs, the data in EEPROM is not reliable and needed to be reconfigured before use.

The EPECCDET flag is cleared after the system is reset and may also be set again during EEPROM data reconstruction after the reset. No matter whether the value is 0 after resetting, if the EPECCDET has been set, the EEPROM needs to be reconfigured.

The FMC ECC two-bit error interrupt should be enabled in order to capture the asserting of EPECCDET in a timely manner. The library function fmc_interrupt_enable(FMC_INT_ECCDET) can be called to enable a two-bit error interrupt. Do not operate the register such as FMC ECCCS |= FMC ECCCS ECCDETIE;. Because if there is an EEPROM ECC error before the interrupt is enabled, then the OR operation will write 1 to the error flag bit, and the error flag will be cleared.

After enabling the interrupt, the EEPROM must be reconfigured in the FMC interrupt.

Table 3-2. EEPORM two-bit ECC error handling

```
if(RESET != fmc_interrupt_flag_get(FMC_INT_FLAG_EPECCDET))
{
    fmc_interrupt_flag_clear(FMC_INT_FLAG_EPECCDET);
    fmc_unlock();
    ob_unlock();
    ob1_eeprom_parameter_config(OB1CS_DF_32K_EF_32K, OB1CS_EPSIZE_4K);
    ob_reset();
}
```

3.3. Two-bit ECC error caused by loading OB0 / OB1

If an two-bit ECC error occurs when loading OB0 / OB1. The data in the error address is returned to all F, and the program will not enter the NMI interrupt.

Because it is few opportunities to rewrite OB0 / OB1, the two-bit ECC error can be concluded to be caused by abnormal operations, and OB0 / OB1 needs to be reconfigured.

3.4. Two-bit ECC error caused when bus reads OB0 from 0x1FFFF80x

If an two-bit ECC error occurs, the data in the error address is returned to all F, and the program will not enter the NMI interrupt. Because it is few opportunities to rewrite OB0, the two-bit ECC error can be concluded to be caused by abnormal operations, and OB0 needs to be reconfigured.

4. Revision history

Table 4-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov.30 2023

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