GigaDevice Semiconductor Inc.

GD32L23x Series Software Development Guide

Application Note
AN197

Revision 1.0

(Jun. 2024)

Table of Contents

List of Figures

List of Tables

1. Overview

This document is intended for GD32L23x MCU, introducing how to build and debug GD32L23x chip based projects and how to use each module. This application note aims to give an exemplary introduction to peripheral resources on GD32L23x MCU so that users can know how to develop software rapidly with GD32L23x chips.

For more information on deepsleep1 mode and deepsleep2 mode, please refer to the ***AN094 Wakeup methods from deepsleep1 mode for GD32L233 series*** and the ***AN167 Use methods of deepsleep2 mode for GD32L233***.

For more information on the low power consumption solution for SLCD display, please refer to the ***AN087 Low Power Consumption Solution for SLCD Display Based on GD32L233***.

For the differences between the GD32L235 and GD32L233 series, please refer to ***AN179 Differences between GD32L235 and GD32L233 products***. For the method of porting from GD32L233 to GD32L235, please refer to ***AN184 Porting from GD32L233 series to GD32L235 series***.

For information on simulating EEPROM with the GD32L23x FLASH, please refer to ***AN201 FLASH emulate EEPROM for GD32L23x series***.

The Embedded Builder software supports the GD32L23x series. For usage, please refer to the <Embedded Builder User Manual>.

Table 1-1. Applicable Products

Type	Model
MCU	GD32L23x Series

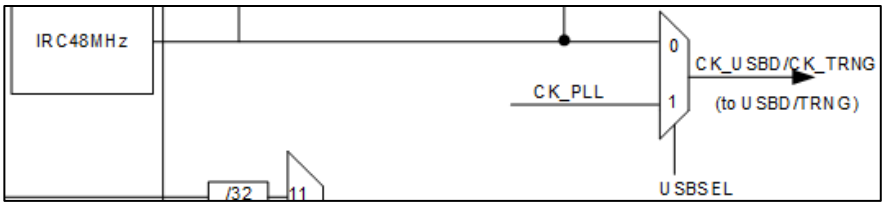
2. Software feature development

2.1. Precautions for using UBSD

2.1.1. USBD Clock Configuration

The USBD module clock tree is shown in ***Figure 2-1. USBD Peripheral Clock Tree***.

Figure 2-1. USBD Peripheral Clock Tree



The internal IRC48M clock or the external CK_PLL clock can be selected through the USBSEL selector, with CK_PLL configured through PLL frequency division and multiplication. The startup clock for USBD is 48MHz.

To use the internal IRC48M clock or the external PLL clock, the RCU control register (RCU_CTL) needs to be used to enable the IRC48M or PLL.

The USBSEL selector can choose between two clock sources as follows:

- CK_PLL: Configured by PLL frequency division and multiplication.
- CK_IRC48M: Provided by the internal 48M clock (requires calibration with an accuracy of ±500ppm).

USBD Clock Configuration Code, as shown in ***Figure 2-2. USBD Peripheral Clock Configuration Code***.

Figure 2-2. USBD Peripheral Clock Configuration Code

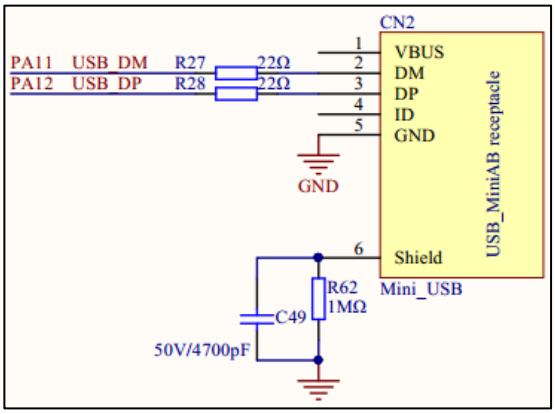
```
void rcu_config(void)
{
    rcu_usbd_clock_config(RCU_USBDSRC_PLL);

    /* enable USB APB1 clock */
    rcu_periph_clock_enable(RCU_USBD);
}
```

2.1.2. USBD-related GPIO Configuration

The DP/DM pins of USBD are dedicated pins. Once the USBD clock is enabled, the DM (PA11) and DP (PA12) pins are the default data transmission pins for USBD, and no separate configuration is needed. It is worth noting that before enabling USBD, the DP must be pulled

up. There are three ways to pull up the DP: first, by enabling the internal register (DPC); second, by controlling the pull-up through the GPIO pin output; third, by externally connecting a 3.3V pull-up. The control circuit of USBD is shown in *Figure 2-3. USBD Control Circuit*.

Figure 2-3. USBD Control Circuit



2.1.3. USBD Array and Endpoint Configuration

The GD32L23x series chips use the M23 core, and when defining array variables, they need to be aligned at even addresses, either 2-byte or 4-byte alignment, otherwise the device may not be able to enumerate normally. The array variables defined are 2-byte aligned, as shown in *Figure 2-4. Definition of Device Descriptor Array*.

Figure 2-4. Definition of Device Descriptor Array

```
__ALIGNED(2) usb_desc_dev cdc_dev_desc =
{
    .header =
    {
        .bLength          = USB_DEV_DESC_LEN,
        .bDescriptorType  = USB_DESCTYPE_DEV,
    },
    .bcdUSB               = 0x0200U,
    .bDeviceClass         = USB_CLASS_CDC,
    .bDeviceSubClass      = 0x00U,
    .bDeviceProtocol      = 0x00U,
    .bMaxPacketSize0      = USBD_EP0_MAX_SIZE,
    .idVendor             = USBD_VID,
    .idProduct            = USBD_PID,
    .bcdDevice            = 0x0100U,
    .iManufacturer        = STR_IDX_MFC,
    .iProduct             = STR_IDX_PRODUCT,
    .iSerialNumber        = STR_IDX_SERIAL,
    .bNumberConfigurations = USBD_CFG_MAX_NUM,
};
```

The USBD of the GD32L23x series supports up to 8 endpoints (including endpoint 0), with the endpoint configuration address range being 0x00-0x1FF, and the endpoint address should be 16-bit aligned.

2.1.4. Other notes

- USBD is a full-speed device interface, which can only act as a USB device and cannot act as a USB host.

- The data transmission of USBD supports the USB 2.0 protocol and is a half-duplex transmission.
- When USBD is working normally, the digital signal is a differential signal in the form of a square wave.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jun.17, 2024

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