GigaDevice Semiconductor Inc.

Device limitations of GD32F50x

Errata Sheet

Revision 1.1

(Nov. 2025)

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1. Introduction

This document applies to GD32F50x product series, as shown in ***Table 1-1. Applicable products***. It offers technical guidance for using GD32 MCU and provides workaround to current device limitations.

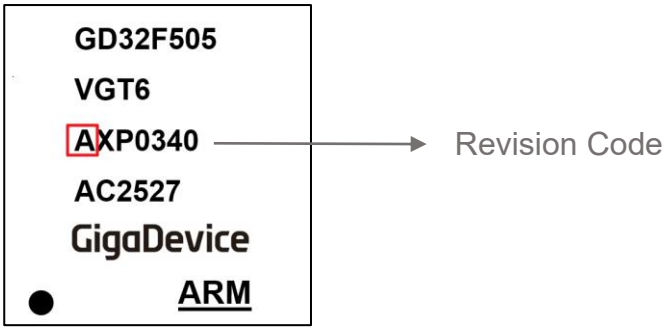
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32F503xx series
	GD32F505xx series

1.1. Revision identification

The device revision can be identified according to the mark on the top of the package. The 1st code on Line 3 of the mark is the product revision code, as shown in ***Figure 1-1. Device revision code of GD32F50x***.

Figure 1-1. Device revision code of GD32F50x



1.2. Summary of device limitations

The device limitations of GD32F50X are shown in ***Table 1-2. Device limitations***, please refer to Section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code A
I2C	***When the I2C slave is configured in 10-bit address mode, if the external master does not send a STOP signal after transmitting a frame of data, the I2C slave will be unable to match the slave address in subsequent operations***	Y
CAN	***When TFO bit is set and mailbox 0/1/2 are enabled for simultaneous transmission, aborting the transmission of mailbox 2 will also abort mailbox 1***	Y

Module	Limitations	Workaround
		Rev. Code A
	When TFO is cleared and the identifiers of transmission mailbox 1 or 2 are configured as 0x1FFFFFFF, the data in transmission mailbox 1 or 2 cannot be sent	Y
Core	***Access permission faults are prioritized over unaligned Device memory faults***	N

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. I2C

2.1.1. When the I2C slave is configured in 10-bit address mode, if the external master does not send a STOP signal after transmitting a frame of data, the I2C slave will be unable to match the slave address in subsequent operations

Description & impact

When the I2C slave is configured in 10-bit address mode, if the external master does not send a STOP signal after transmitting a frame of data and instead sends a START signal to initiate the transmission of a second frame, the I2C slave will misinterpret the second byte of the slave address (the lower 8 bits of the 10-bit address) as data, and the address match flag (ADDSEND) will not be set. For example, if the slave is in address polling mode, it will continuously wait for an address match and remain stuck in a loop. Similarly, if the slave is in interrupt or DMA mode, it will fail to process subsequent data due to the inability to match the slave address.

Workarounds

When the I2C slave is operating in 10-bit address mode, the external I2C master must send the corresponding STOP signal at the end of each frame transmission.

2.2. CAN

2.2.1. When TFO bit is set and mailbox 0/1/2 are enabled for simultaneous transmission, aborting the transmission of mailbox 2 will also abort mailbox 1

Description & impact

When TFO bit is set and mailbox 0/1/2 are enabled for simultaneous transmission, aborting the transmission of mailbox 2 will also abort mailbox 1, meaning the data in mailbox 1 will not be transmitted.

Workarounds

Use one of the following solutions:

1) Before aborting the transmission of mailbox 2, confirm whether mailbox 1 is in the pending state.
2) After aborting the transmission of mailbox 2, reconfigure mailbox 1/2 for transmission and resend.

2.2.2. When TFO is cleared and the identifiers of transmission mailbox 1 or 2 are configured as 0x1FFFFFFF, the data in transmission mailbox 1 or 2 cannot be sent

Description & impact

When TFO is cleared and the identifiers of transmission mailbox 1 or 2 are configured as 0x1FFFFFFF, the data in transmission mailbox 1 or 2 cannot be sent. For example, when TFO is set to 0 and the ID of transmission mailbox 1 is configured as 0x1FFFFFFF, the data in transmission mailbox 1 cannot be sent.

Workarounds

Use one of the following solutions:

1) When the identifier is 0x1FFFFFF, use transmission mailbox 0 for data frame transmission.
2) Use first-in-first-out (FIFO) transmission order, i.e., set TFO = 1.

2.3. Core

About Cortex-M33 limitations, please refer to “Cortex-M33 AT623 and Cortex-M33 with FPU AT624 Software Developer Errata Notice”. This document can be downloaded on ARM official wbesite.

2.3.1. Access permission faults are prioritized over unaligned Device memory faults

This limitation refers to Arm ID number 1080541 in “Cortex-M33 AT623 and Cortex-M33 with FPU AT624 Software Developer Errata Notice”.

Description & impact

A load or store which causes an unaligned access to Device memory will result in an UNALIGNED UsageFault exception. However, if the region is not accessible because of the MPU access permissions (as specified in MPU_RBAR.AP), then the resulting MemManage fault will be prioritized over the UsageFault.

This erratum affects all configurations of the Cortex-M33 processor with the MPU enabled.

The failure occurring conditions are as follows:

The MPU is enabled and:

- A load/store access occurs to an address which is not aligned to the data type specified in the instruction.
- The memory access hits one region only.
- The region attributes (specified in the MAIR register) mark the location as Device memory.
- The region access permissions prevent the access (that is, unprivileged or write not allowed).

The implications of this limitation is that the MemManage fault caused by the access permission violation will be prioritized over the UNALIGNED UsageFault exception because of the memory attributes.

Workarounds

Not available. However, it is expected that no existing software is relying on this behavior since it was permitted in Armv7-M.(The CM33 is Armv8-M).

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Aug.8 2025
1.1	1. Add limitations of CAN, refer to ***When TFO bit is set and mailbox 0/1/2 are enabled for simultaneous transmission, aborting the transmission of mailbox 2 will also abort mailbox 1*** 2. Add limitations of CAN, refer to ***When TFO is cleared and the identifiers of transmission mailbox 1 or 2 are configured as 0x1FFFFFFF, the data in transmission mailbox 1 or 2 cannot be sent***	Nov.5 2025

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