GigaDevice Semiconductor Inc.

Device limitations of GD32E51x

Errata Sheet

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1. Introduction

This document applies to GD32E51x product series, as shown in ***Table 1-1. Applicable products***. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

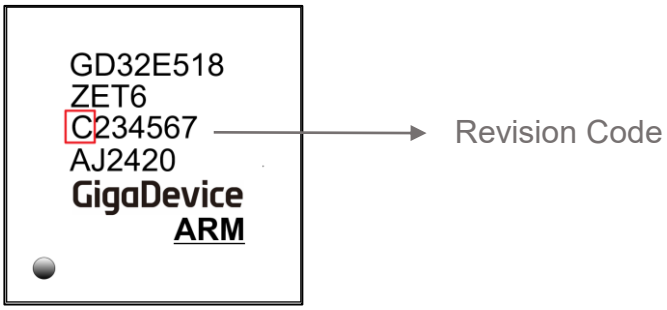
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32E513xx series
	GD32E517xx series
	GD32E518xx series
	GD32EPRTxxA series

1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in ***Figure 1-1. Device revision code of GD32E51x***.

Figure 1-1. Device revision code of GD32E51x



1.2. Summary of device limitations

The device limitations of GD32E51x are shown in ***Table 1-2. Device limitations***, please refer to section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code C
RCU	*MCU cannot be waked up from Deepsleep mode when DSLP_HOLD bit is set*	Y
	The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly	Y
ADC	*ADC data acquisition error occurs when the ADC clock is much*	Y

Module	Limitations	Workaround
		Rev. Code C
	slower than the PCLK clock	
DAC	***In the DAC noise mode, when the value (DH+DWBW) is configured more than 4095, the DAC output voltage will have an abnormal break point***	Y
I2C	***Read one more data because the BTC flag was not cleared***	Y
	When SDA line interference causes garbled data on the I2C bus, it can lead to a stuck in the I2C2 slave device	N
EXMC	***NE timing can not satisfy the requirement when using NAND pre-waiting function***	Y
USB	***When USBHS device uses an internal PHY and is suspended by the host, its suspension interrupt flag and wakeup interrupt flag are frequently set***	N

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. RCU

2.1.1. MCU cannot be waked up from Deepsleep mode when DSLP_HOLD bit is set

Description & impact

When the DSLP_HOLD bit in the DBG_CTL register is set, the MCU cannot be waked up after the MCU enters deepsleep mode.

Workarounds

When the DSLP_HOLD bit is set to enable low power debugging, the application programme need switch the system clock to IRC8M before entering the deepsleep mode.

2.1.2. The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly

Description & impact

When LXTAL stops unexpectedly, the LXTALSTB bit cannot be cleared by disabling the LXTAL, which prevents the LXTAL from restarting.

Workarounds

By repeatedly setting and resetting the LXTALBPS more than ten times to clear the LXTALSTB bit, and then reconfiguring the LXTAL. The reference code for clearing LXTALSTB bits is as follows:

```
void lxtal_stb_clear(void)
{
    volatile   uint32_t i = 0U;
    /* close LXTAL clock */
    rcu_osci_off(RCU_LXTAL);
    for(i = 0; i < 10; i++) {
        /* enable the LXTAL bypass mode */
        rcu_osci_bypass_mode_enable(RCU_LXTAL);
        /* disable the LXTAL bypass mode */
        rcu_osci_bypass_mode_disable(RCU_LXTAL);
    }
}
```

2.2. ADC

2.2.1. ADC data acquisition error occurs when the ADC clock is much slower than the PCLK clock

Description & impact

When the ADC clock is much slower than the PCLK clock, the ADC_RDATA register is read immediately after the EOC is set and a data acquisition error occurs.

Workarounds

When the delay between reading EOC flag and reading ADC_RDATA is no more than two ADC clocks, after the EOC flag is set, software need to delay two ADC clocks before reading the ADC_RDATA register.

2.3. DAC

2.3.1. In the DAC noise mode, when the value (DH+DWBW) is configured more than 4095, the DAC output voltage will have an abnormal break point

Description & impact

When the DAC is configured in noise mode and the DAC output value is set to a large value, the superimposed value (DH+DWBW) will exceed the maximum value of 4095, resulting in an abnormal break point of zero voltage in the DAC output signal.

Workarounds

When the DAC output value and the noise wave peak value are configured, avoid the superimposed value (DH+DWBW) overflow.

2.4. I2C

2.4.1. Read one more data because the BTC flag was not cleared

Description & impact

If an interrupt occurs before reading I2C_DATA register when RBNE flag is set and BTC flag is reset, I2C will read an additional data if BTC flag is set during the interrupt processing because the read data operation cannot clear the BTC flag.

Workarounds

Use one of the following solutions:

1) Using interrupt method to read the I2C_DATA register (need higher interrupt priority).
2) Using DMA method to read the I2C_DATA register (recommend).

2.4.2. When SDA line interference causes garbled data on the I2C bus, it can lead to a stuck in the I2C2 slave device

Description & impact

When I2C2 operates as a slave and is configured in 10-bit addressing mode, and if there is a mismatch in the 10-bit address header or the lower 8 bits of the 10-bit address during the I2C2 slave addressing phase, interference on the SCL / SDA line that causes the next RESTART / STOP signal to be sent early can result in the I2C2 slave pulling the SDA line low, ultimately leading to the I2C2 slave stuck.

Note: This limitation applies to I2C2.

Workarounds

Not available.

2.5. EXMC

2.5.1. NE timing can not satisfy the requirement when using NAND pre-waiting function

Description & impact

For some EXMC_NCE-sensitive NAND Flash, NE timing can not satisfy the requirement when using NAND pre-waiting function. NE signal keeps the low level when EXMC_INTx is active.

Workarounds

Using general I/O port to simulate the NE timing to finish the NAND reading and writing, NE signal keeps the low level after starting reading or writing.

2.6. USB

2.6.1. When USBHS device uses an internal PHY and is suspended by the host, its suspension interrupt flag and wakeup interrupt flag are frequently set

Description & impact

When a USBHS device uses an internal PHY and is suspended by the host, its suspension interrupt flag (SP) and wakeup interrupt flag (WKUPIF) are frequently set.

Workarounds

Not available. But it does not affect the normal use of USBHS.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Aug.22, 2024

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