GigaDevice Semiconductor Inc.

Device Limitations of GD32E230

Errata Sheet

Table of Contents

List of Figures

List of Tables

1. Introduction

This document applies to GD32E230 product series, as shown in ***Table 1-1. Applicable products***. It offers technical guidance for using GD32MCU and provides workaround to current device limitations.

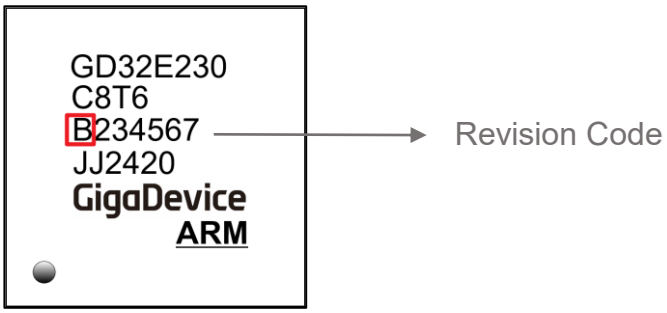
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32E230xx series

1.1. Revision identification

The device revision can be identified according to the mark on the top of the package. The 1st code on Line 3 of the mark is the product revision code, as shown in ***Figure 1-1. Device revision code of GD32E230***.

Figure 1-1. Device revision code of GD32E230



1.2. Summary of device limitations

The device limitations of GD32E230 are shown in ***Table 1-2. Device limitations***, please refer to Section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround	
		Rev. Code A	Rev. Code B
System	*DMA transmission is blocked when the CPU performs flash memory erase / program operations in the flash*	Y	Y
FMC	*The PGERR bit will not be set when performing two word programming operations on the same address*	Y	Y
PMU	*Power consumption is higher in standby mode in some case*	N	N
	Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode	N	N

Module	Limitations	Workaround	
		Rev. Code A	Rev. Code B
RCU	*MCU cannot be waked up after entering deep-sleep mode when DSLP_HOLD bit is set*	Y	Y
	The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly	Y	Y
ADC	*ADC data acquisition error occurs when the ADC clock is much slower than the PCLK clock*	Y	Y
RTC	*When FACTOR_A is set to 0 and the A1S bit is set to 1, it will cause an reload value*	Y	Y
	During the AM 11 o'clock time slot, the add 1 hour function	Y	Y
	Calibrate abnormally when using both smooth digital calibration and FREQI calibration	Y	Y
TIMER	*Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function*	Y	Y
	When the BRKP bit is set to 0, if the CMP output signal is used to trigger the braking of TIMER0, then the brake of TIMER0 will remain continuously active	Y	Y
I2C	*Read one more data because the BTC flag was not cleared*	Y	Y
	Due to the timing difference of START signal between I2C0 and I2C1, the master that wins the arbitration cannot receive ACK, and the bus is blocked	N	N
	The 90ms timeout interrupt cannot be entered in SAM_V mode	Y	Y
	Switching I2CEN from the disabled state to the enabled state may cause the I2C to send a start signal	N	N
	The I2C master cannot initiate a new access when arbitration is lost	N	N
	When SCL is pulled low, the timeout period for the first transaction is 25ms, and for all subsequent transactions, the timeout period is 130ms	Y	Y

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. System

2.1.1. DMA transmission is blocked when the CPU performs flash memory erase / program operations in the flash

Description & impact

When the CPU performs flash memory erase / program operations in the flash, DMA transmission is blocked due to bus being locked by flash operation.

Workarounds

During project linking, scatter load the the interrupt vector table, all interrupt service routines, and flash erase / program operation function to SRAM. This means the interrupt handlers and programs related to flash erase / program will be executed in SRAM.

2.2. FMC

2.2.1. The PGERR bit will not be set when performing two word programming operations on the same address

Description & impact

When the programming width is 64 bits and the address area to be programmed is empty, performing two word programming operations on the same address will not set the PGERR bit, and the data programmed in the second operation will be incorrect.

Workarounds

Ensure that the data at the address is empty before programming.Before programming the same address, programme need to perform an erase operation on that address area.

2.3. PMU

2.3.1. Power consumption is higher in standby mode in some case

Description & impact

In some case, power consumption is higher in standby mode, due to HXTALSTB bit is not cleard.

Workarounds

Application programme can turn off HXTAL and waite for HXTAL_STB cleard before entering standby mode to reduce the power consumption.

2.3.2. Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode

Description & impact

When reset the internal signal STBY_CTL to enter to standby mode, if the Tglitch is smaller than 100ns, which will cause the mcu cannot be waked up. The narrow glitch will result in incorrect Vcore voltage.

Note: The Tglitch is the time between STBY_CTL low level and the wakeup signal (PA0 high level).

Workarounds

Not available.

2.4. RCU

2.4.1. MCU cannot be waked up after entering deep-sleep mode when DSLP_HOLD bit is set

Description & impact

When DSLP_HOLD bit is set and debug the mcu in deep-sleep mode, the mcu will not be waked up.

Workarounds

When the DSLP_HOLD bit is set to enable low power debugging, the application programme need switch the system clock to IRC8M before entering the deep-sleep mode.

2.4.2. The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly

Description & impact

When LXTAL stops unexpectedly, the LXTALSTB bit cannot be cleared by disabling the LXTAL, which prevents the LXTAL from restarting.

Workarounds

By repeatedly setting and resetting the LXTALBPS more than ten times to clear the LXTALSTB bit, and then reconfiguring the LXTAL. The reference code for clearing LXTALSTB bits is as follows:

```
void lxtal_stb_clear(void)
{
    volatile    uint32_t i = 0U;
    /* close LXTAL clock */
    rcu_osci_off(RCU_LXTAL);
    for(i = 0; i < 10; i++) {
        /* enable the LXTAL bypass mode */
        rcu_osci_bypass_mode_enable(RCU_LXTAL);
        /* disable the LXTAL bypass mode */
        rcu_osci_bypass_mode_disable(RCU_LXTAL);
    }
}
```

2.5. ADC

2.5.1. ADC data acquisition error occurs when the ADC clock is much slower than the PCLK clock

Description & impact

When the ADC clock is much slower than the PCLK clock,the ADC_RDATA register is read immediately after the EOC is set and a data acquisition error occurs.

Workarounds

When the delay between reading EOC flag and reading ADC_RDATA is no more than two ADC clocks, after the EOC flag is set, software need to delay two ADC clocks before reading the ADC_RDATA register.

2.6. RTC

2.6.1. When FACTOR_A is set to 0 and the A1S bit is set to 1, it will cause an reload value error

Description & impact

When FACTOR_A bit is set to 0 and the A1S bit is set to 1, it will cause an error in the reload value.

Workarounds

When FACTOR_A is configured as 0, avoid setting the A1S bit.

2.6.2. During the AM 11 o'clock time slot, the add 1 hour function is abnormal

Description & impact

During the AM 11 o'clock time slot, setting A1H bit to add 1 hour will cause the date to be inaccurate.

Workarounds

Avoid setting A1H bit during the AM 11 o'clock time slot.

2.6.3. Calibrate abnormally when using both smooth digital calibration and FREQI calibration

Description & impact

Using both smooth digital calibration and FREQI calibration will cause calibration result abnormal.

Workarounds

1) Use RTC shift function to replace smooth digital calibration, such as setting A1S bit and configuring appropriate SFS bits to satisfy the accuracy requirement.
2) Use two 16 seconds calibration window to replace one 32 seconds calibration window.

2.7. TIMER

2.7.1. Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function

Description & impact

When using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function, DMA transfers data 0x00 to TIMERx_CHyCV register which will result in the second data lost after data 0x00.

Workarounds

Use one of the following methods:

1) Do not use data 0x00 in DMA transfer buffer.
2) Transfer the second data after the 0x00 twice.
3) Use the timer update event to trigger DMA transfer.

2.7.2. When the BRKP bit is set to 0, if the CMP output signal is used to trigger the braking of TIMER0, then the brake of TIMER0 will remain continuously active

Description & impact

When BRKP is configured to be effective at a low level, if the CMP output signal is used to trigger the braking of TIMER0, then the brake of TIMER0 will remain continuously active.

Workarounds

Configure BRKP to 1 and use a high level instead of a low level to trigger the brake.

2.8. I2C

2.8.1. Read one more data because the BTC flag was not cleared

Description & impact

If an interrupt occurs before reading I2C_DATA register when RBNE flag is set and BTC flag is reset, I2C will read an additional data if BTC flag is set during the interrupt processing because the read data operation cannot clear the BTC flag.

Workarounds

1) Using interrupt method to read the I2C_DATA register (need higher interrupt priority).
2) Using DMA method to read the I2C_DATA register (recommend).

2.8.2. Due to the timing difference of START signal between I2C0 and I2C1, the master that wins the arbitration cannot receive ACK, and the bus is blocked

Description & impact

The timing of the START signal of I2C0 and I2C1 is different, which leads to the misplaced SCL clock signal sent out, and the clock sent out in the address transmission phase is more than 8 clock signals. As a result, the master that wins the arbitration cannot receive ACK, so the SCL signal line is pulled down and the I2C bus is stuck.

Workarounds

Not available.

2.8.3. The 90ms timeout interrupt cannot be entered in SAM_V mode

Description & impact

When the SAM_V interface timeout detection function is enabled, the 90ms timeout interrupt cannot be triggered.

Workarounds

Enable the SMBus host mode by setting SMBSEL and SMBEN, and disable STOEN.

2.8.4. Switching I2CEN from the disabled state to the enabled state may cause the I2C to send a start signal

Description & impact

Switching I2CEN from the disabled state to the enabled state may cause the I2C to send a start signal.

Workarounds

Not available.

2.8.5. The I2C master cannot initiate a new access when arbitration is lost

Description & impact

The I2C master cannot initiate a new access when arbitration is lost.

Workarounds

Not available.

2.8.6. When SCL is pulled low, the timeout period for the first transaction is 25ms, and for all subsequent transactions, the timeout period is 130ms

Description & impact

By setting TOEN to enable the timeout counting function, when SCL is pulled low, the timeout period is 25ms for the first timeout and 130ms for subsequent timeouts.

Workarounds

In the I2C timeout interrupt handler, first disable (TOEN = 0)and then enable (TOEN = 1) the timeout counting function by.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Aug.12, 2024

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