GigaDevice Semiconductor Inc.

GD32 MCU Hardware Layout Design Reference

Application Note
AN191

Revision 1.1

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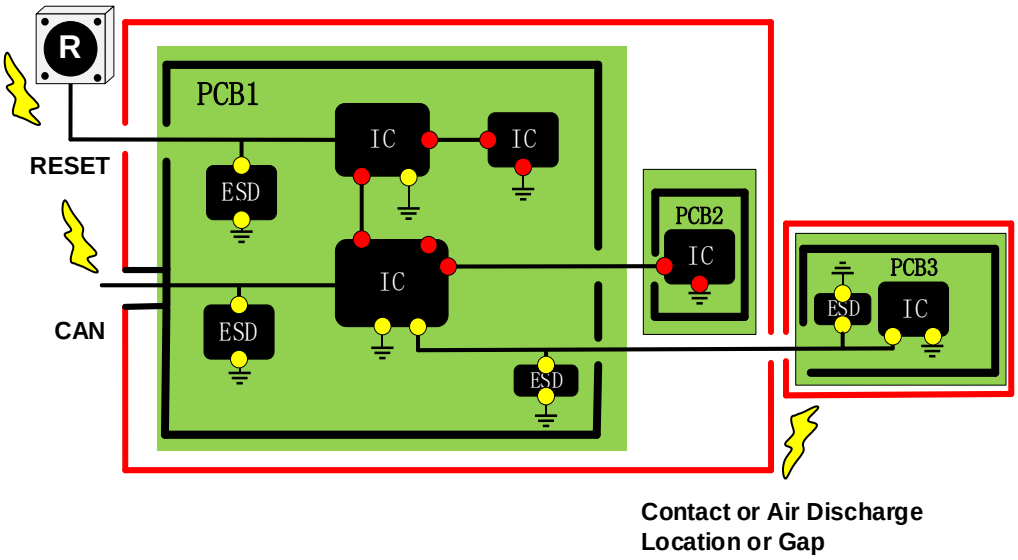
1. Introduction

With the miniaturization of semiconductor process technology and the improvement in performance, MCUs are facing increasingly complex electromagnetic environments. Particularly in systems, MCUs may encounter direct or indirect electrostatic discharge (ESD) or other transient interferences, potentially leading to issues such as MCU control module resets, crashes, hard failures, and other problems that affect the normal operation of the entire control system. Therefore, developers need to consider electromagnetic interference issues such as static electricity from both the design perspective and PCB layout perspective, optimizing designs to mitigate or even eliminate the impact of static electricity and other electromagnetic interferences on the system.

2. Electromagnetic Interference Protection Design at the Design End

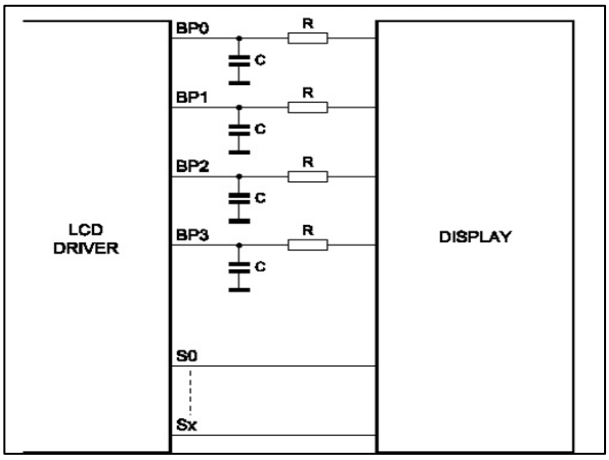
During system design, developers need to identify areas in the system that are prone to introducing static electricity or other electromagnetic interference, as well as the potential paths through which these interferences may directly or indirectly affect the pins of related ICs. As illustrated in ***Figure 2-1. Coupling Paths for Static Electricity and Electromagnetic Interference***, typical areas include connection points between PCB boards, CAN communication ports, USB ports, reset pin output ports, and other similar locations, which may introduce static electricity or electromagnetic interference. Reserving appropriate ESD protection devices at these critical points during the design phase can effectively save development time and enhance the robustness of the system board against ESD.

Figure 2-1. Coupling Paths for Static Electricity and Electromagnetic Interference



In system design, components such as CAN communication ports and USB ports are typically recognized as being susceptible to static electricity and other electromagnetic interference. However, certain other elements, such as driver pins for LCD screens, Reset pins, Enable (EN) pins, and the driver control pins for LED running lights, are also prone to introducing static electricity and electromagnetic interference, and thus require electromagnetic interference protection design as well. This is because these functional pins often have densely packed or long routing traces, or even cables leading off the board, making them more susceptible to crosstalk or to picking up static electricity and electromagnetic interference radiating from the environment. As shown in ***Figure 2-2. Display Protection Circuit***, for densely packed and longer routing traces like display driver pins, it is advisable to incorporate RC filtering, TVS diodes, or other ESD protection mechanisms into the design. For schematic design references related to hardware EMC protection, developers can refer to the "AN163 GD32 MCU Hardware Protection Design Reference" document.

Figure 2-2. Display Protection Circuit



3. Electromagnetic Interference Protection Design for PCB Layout

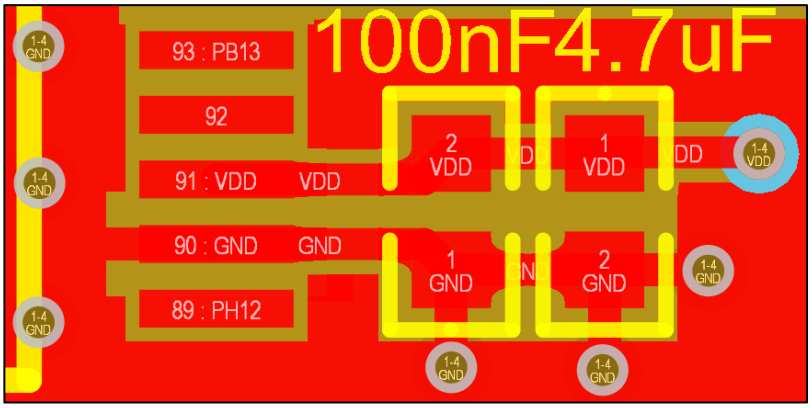
3.1. Placement of Decoupling Capacitors for MCU Power

Each power pin of the MCU should have at least one decoupling capacitor installed. On one hand, decoupling capacitors can stabilize the MCU's power supply voltage, provide instantaneous current, ensure power integrity, and reduce parasitic impedance; on the other hand, they can improve signal integrity and suppress electromagnetic noise. Decoupling capacitors can mitigate high-frequency currents generated by noise between nearby power and ground (GND), as well as suppress high-frequency currents caused by internal CMOS switching devices within the MCU. This helps prevent noise from propagating further along power lines. The smaller the current loop created by the decoupling capacitor, the less noise is generated, improving signal quality. Therefore, decoupling capacitors should be placed as close to the IC as possible.

A well-designed combination of decoupling capacitors and their PCB layout for MCU power pins not only enhances signal quality but also strengthens the MCU's ability to resist external interference. The key considerations for decoupling capacitors are as outlined below, and more detailed design guidelines for decoupling circuits can be found in the “AN058 Decoupling Circuit Design Guide" document.

- Recommended decoupling capacitor combinations: As shown in ***Figure 3-1. Recommended Decoupling Capacitor Combinations***, it is suggested to place 4.7uF + N*100nF capacitors on each pin of the GD MCU's VDD/VBAT power domain, and 1uF + 10nF capacitors on each pin of the VDDA power domain.
- Decoupling capacitors should be placed as close to the MCU as possible to ensure the lowest impedance and the smallest current loop path. When multiple decoupling capacitors are used, smaller-value capacitors should be placed closest to the MCU. Typically, 10nF capacitors are closest to the MCU pins, followed by 100nF, and 4.7uF capacitors are placed farther out.
- Ensure that the power current flows to the capacitor first before reaching the MCU. If the power and GND pins are relatively far apart, it is recommended to place the capacitors closer to the GND pin, as signals typically reference GND.
- Each capacitor should have its own dedicated via; sharing a via among multiple capacitors is strictly prohibited. The routing between the decoupling capacitors and the MCU pins should be as wide and short as possible to reduce impedance between the decoupling capacitors and the MCU power pins. The routing between the power network and decoupling capacitors should be as narrow and long as possible, or use vias in between to provide high impedance against potential power noise and ripple.

Figure 3-1. Recommended Decoupling Capacitor Combinations

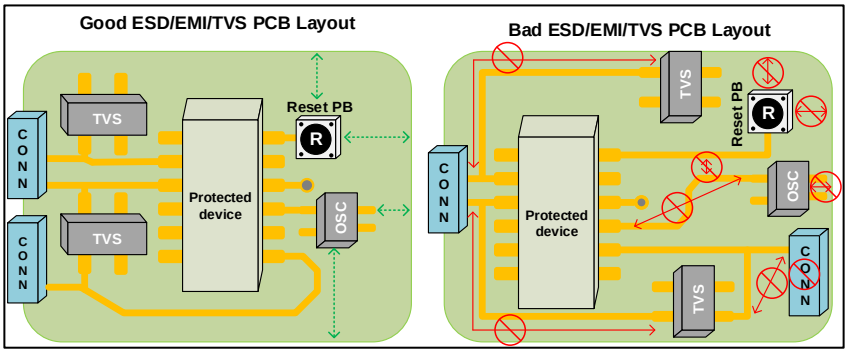


3.2. Placement of Protective Components for Static Electricity and Electromagnetic Interference

As shown in ***Figure 3-2. ESD/EMI/TVS PCB Layout Comparison***, to ensure system operation is not affected by static interference or other transient disturbances, RC filter circuits or protective components such as TVS can be added at the source of interference to discharge static interference or transient disturbances to the ground along the fastest and lowest impedance path. Protective components such as TVS or capacitors should be directly connected to the signal line at the source of the interfering signal. Their ground pins should be directly connected to the ground plane, avoiding excessively long traces between the TVS or capacitors and the signal line or ground, as this could increase the discharge path impedance. High impedance may allow interference to bypass protective components and affect IC devices, causing abnormal operations or even damage.

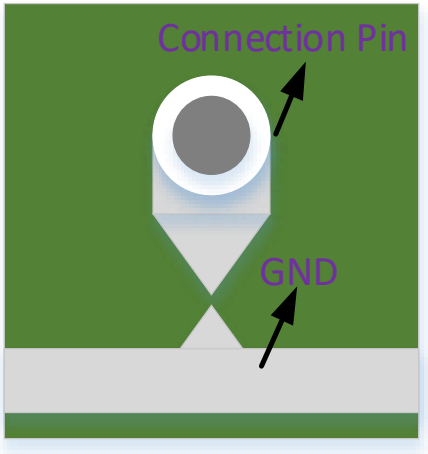
High-speed or sensitive analog/digital traces should be kept as far away from the edges of the PCB as possible. Signal traces near the board edges are less controlled in terms of associated electric and magnetic field lines, making them more susceptible to electromagnetic interference and events like ESD, EMI, and EFT. Furthermore, components or circuits that are easily affected by electromagnetic interference, such as clock crystals and reset circuits, should also be positioned away from the edges of the PCB.

Figure 3-2. ESD/EMI/TVS PCB Layout Comparison



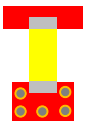
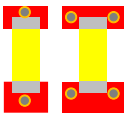
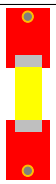
In addition to using methods such as series resistors, parallel varistors, capacitors, or parallel TVS diodes on signal lines to suppress static interference, spark gaps can also be designed on the PCB to discharge static interference to the ground. As shown in ***Figure 3-3. Discharge Spark Gap***, the gap between the spark discharge tip connected to the pin and the tip of the GND discharge point is typically 0.1–0.6mm. The advantage of this method is that it saves some protective components, but its downside lies in the longer response time. The amount of discharged static energy depends on pressure and temperature and can vary over time.

Figure 3-3. Discharge Spark Gap



To ensure that static interference or other transient disturbances are discharged to the ground along the fastest and lowest impedance path, thereby preventing significant interference from entering IC devices, the following protective device layout method is recommended, as shown in ***Figure 3-4. Reducing Parasitic Inductance Generated by Traces***.

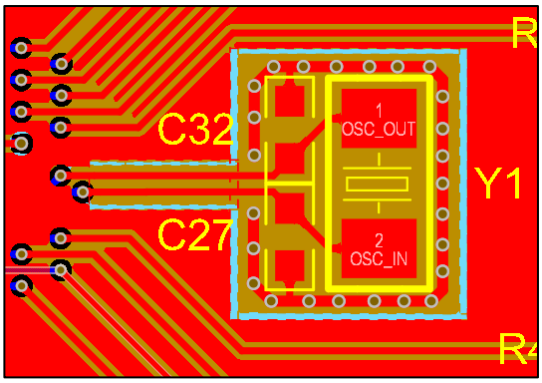
Figure 3-4. Reducing Parasitic Inductance Generated by Traces

Performance	Layout of protective components such as capacitors or TVS	Description
Best		Shorter paths and more ground vias can reduce the discharge current path impedance
Better		Shorter paths
General		Longer paths increase the parasitic inductance of the discharge path
Worst		Thinner traces increase the parasitic inductance of the discharge path

3.3. Layout of Clock Circuits

Clock circuits and components should be placed on the same layer of the circuit board as much as possible and kept away from high-speed switching power devices and RF-related components. Additionally, as shown in ***Figure 3-5. Recommended Clock Layout Design***, the clock circuit should be positioned as close as possible to the corresponding clock pins, with trace lengths not exceeding 12mm. Load capacitors should be placed close to the clock crystal itself and on the same layer of the circuit board. The connections between the crystal, capacitors, and integrated circuits should be as short as possible. A ground guard ring should be used around the clock circuit to isolate it from surrounding circuits.If using a double-layer PCB, avoid having any traces on the backside of the board where the clock is located. If using a multi-layer PCB, avoid having any traces on the layer directly underneath the clock circuit.

Figure 3-5. Recommended Clock Layout Design



3.4. Signal Return Path and Isolation Layer Issues

When current flows from the driving end of a signal, through the signal line, and into the receiving end of the signal, there is always a return current that flows in the opposite direction. This return current starts from the ground pin of the load at the receiving end, travels through the ground wire or copper ground plane, and returns to the driving end of the signal, forming a closed loop with the current flowing through the signal line.Because clock signals and high-speed signals have high frequencies, they are particularly susceptible to electromagnetic interference and tend to generate high-frequency noise. To enhance the anti-interference capability of clock and high-speed signals, reduce their emitted radiation interference, and improve signal quality, all clock and high-speed signal traces must have a complete reference ground plane or a minimal and unimpeded current return path. If there are parallel high-speed signal traces, the 3W rule can be applied to reduce crosstalk between adjacent signal lines, provided there is enough space on the PCB. The 3W rule specifies that the distance between the centers of signal traces should be three times the width of the signal trace.

As shown in ***Figure 3-6. Unimpeded Current Return Path*** and ***Figure 3-7. Congested Signal Return Path***, the presence of excessive vias in the signal return path increases the signal return path impedance and results in higher losses.

Figure 3-6. Unimpeded Current Return Path

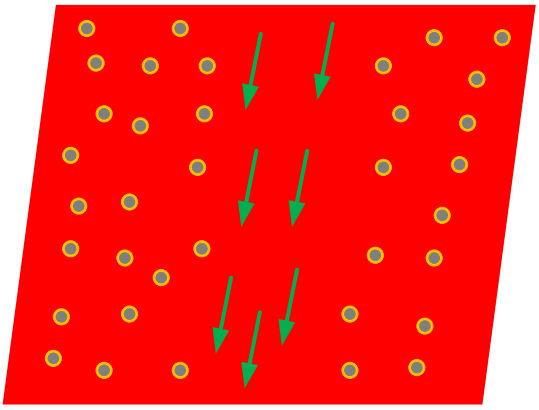
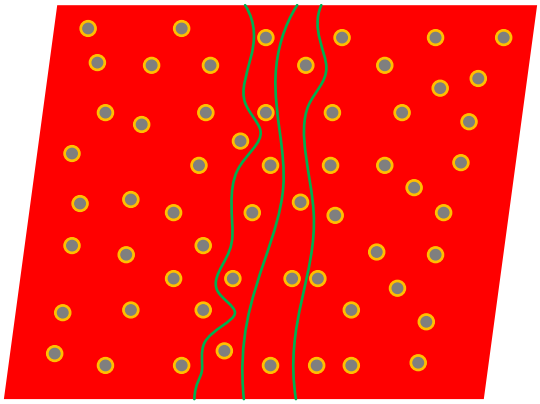


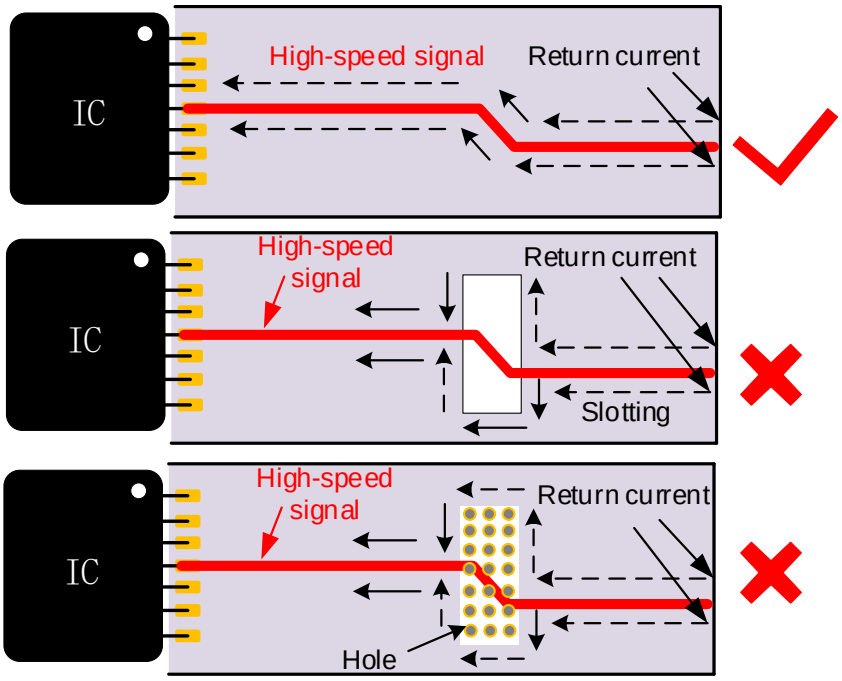
Figure 3-7. Congested Signal Return Path



The trace lengths for high-speed digital signals or clock lines should be kept as short as possible, as these traces typically act as the strongest sources of noise. The longer the traces, the greater the chances of coupling energy related to electromagnetic interference. Some important high-speed single-ended signals, such as clock signals and reset signals, are recommended to be shielded with ground. Ground vias should be evenly distributed along the ground shielding line. Additionally, for high-speed digital signals or clock lines, the signal loop area is usually more critical than the trace length; thus, it is essential to ensure there is a good high-frequency current return path near each trace. As shown in ***Figure 3-8. Slot for return path***, the presence of slots in the return path of clock signals and high-speed signals increases impedance and losses, and may also act as an antenna to absorb interference.

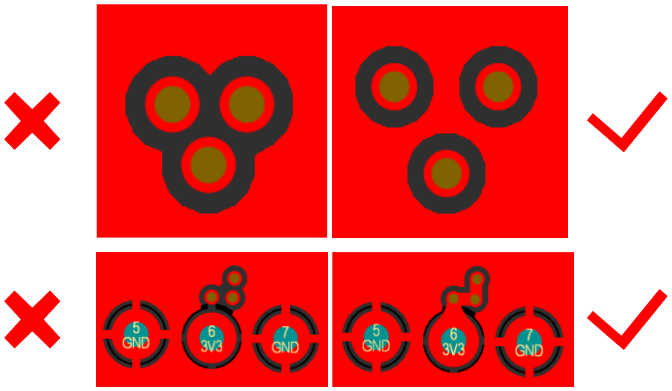
For high-speed signal lines that require strict impedance control, crossing segmented traces is prohibited because discontinuities in impedance caused by slotting can lead to severe signal integrity issues. In fact, both high-speed and low-speed signals should avoid crossing segmented traces as much as possible. Trace segmentation increases the current loop area, enlarges the loop inductance, and makes the output waveforms more prone to oscillation. Crossing segmented traces heightens spatial radiation interference and makes signal lines more susceptible to spatial magnetic field effects. Furthermore, trace segmentation can increase the likelihood of magnetic field coupling from other circuits on the PCB, and the heightened loop inductance and high-frequency voltage drops can form common-mode radiation sources, which produce radiation through external cables.

Figure 3-8. Slot for return path



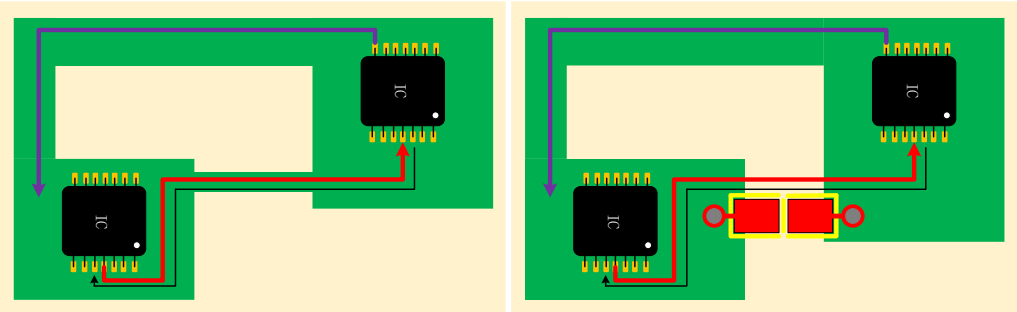
As shown in ***Figure 3-9. Avoid slots caused by vias***, slots caused by vias should be avoided as much as possible. If unavoidable, solutions such as connecting vias to traces or increasing the distance between vias can be employed to minimize the slot area.

Figure 3-9. Avoid slots caused by vias



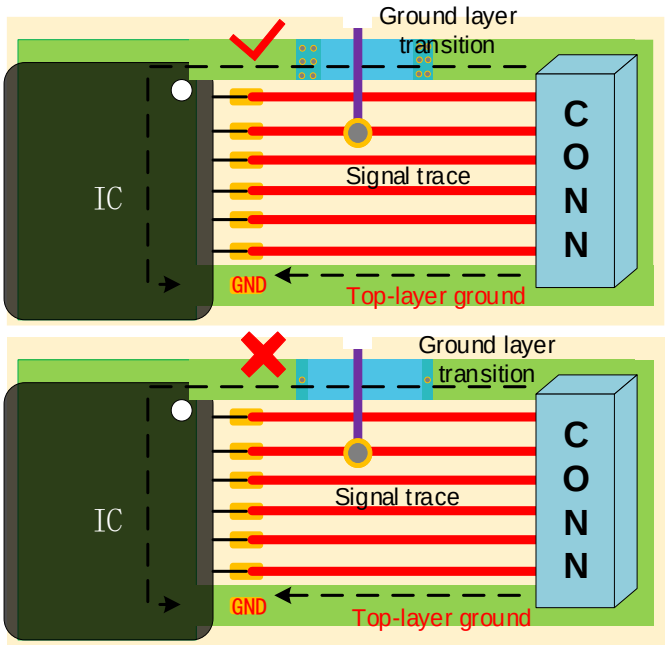
When signal traces cannot avoid crossing segmented planes, effective bridging needs to be implemented. Ground planes along the signal path direction should be connected to form a "bridge" between the slots. Then the signal trace is routed over this "bridge." For example, add stitching capacitors between the two reference planes at nearby split locations to provide a complete return path. As shown in ***Figure 3-10. Bridging across segmented lines***, Bridging Across Segmented Planes, the red line represents the signal current, the purple line illustrates the signal return path without bridging, and the black line shows the signal return path after bridging.

Figure 3-10. Bridging across segmented lines



As shown in ***Figure 3-11. Ground layer optimization in signal return paths***, it is often unavoidable to change ground layers due to the lack of a complete ground plane in the system board and the existence of signal traces routed on different layers. The return currents of the signal lines from this IC mainly rely on the copper ground planes on the top and bottom of the board, depicted as black dashed return paths.Since high-speed signals and high-frequency noise tend to seek the path of least impedance, this path is often the shortest one on the ground plane. Therefore, it is recommended to widen the ground plane at ground layer transitions and add more vias to reduce the parasitic inductance caused by via transitions. This ensures that signals have more return paths with small loop areas. If there are insufficient vias at the ground transitions, more high-frequency signals and noise will return through other ground connections on the board, degrading signal quality and potentially interfering with the IC's normal operation.Similarly, in system board designs where it is not possible to ensure a complete ground reference layer, efforts should be made to provide IC drivers on the system board with multiple ground return paths. Additionally, the return ground path for signals should have a minimal loop area and low impedance to maintain signal integrity.

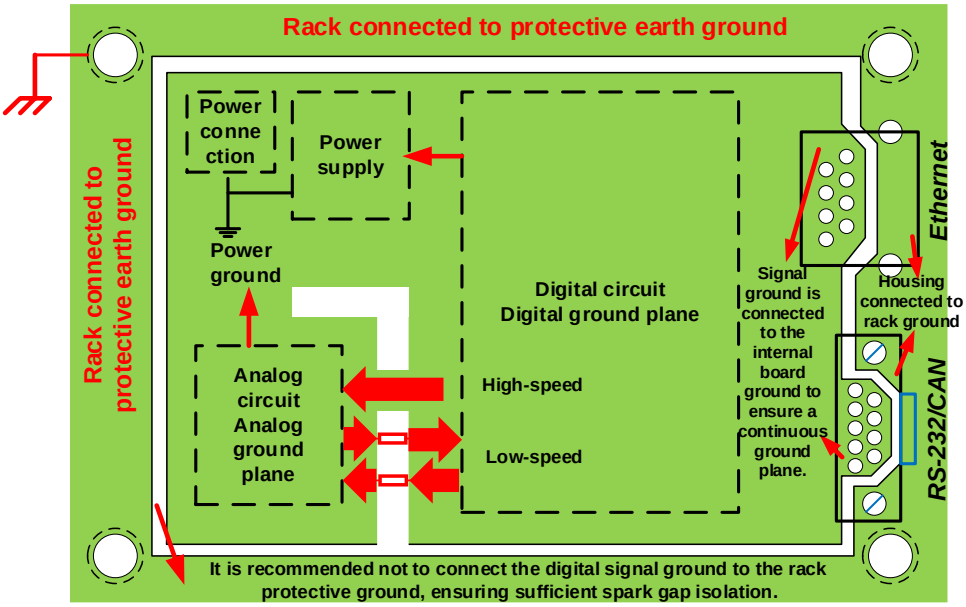
Figure 3-11. Ground layer optimization in signal return paths



3.5. Ground segmentation layout

As shown in ***Figure 3-12. Rack connected to protective earth ground with split layout***, and the layout is divided accordingly. Digital noise currents are typically much greater than analog circuit noise currents. Here, the analog ground and digital ground planes are separated, and the ground plane division ensures that the analog circuit stays away from digital noise currents. Additionally, the power circuit is positioned between the analog circuit and the digital circuit instead of being placed on the side of either the analog circuit or the digital circuit. This ensures that the analog ground and digital ground separately connect to the power source, keeping the analog circuit away from digital noise and current.USB, Ethernet, RS232, and other connectors whose signal interfaces include ground can be placed on the internal signal ground of the board to ensure a continuous ground plane for connector interfaces. The outer casing of the USB, Ethernet, RS232, and other connectors should be connected to the rack protective ground. There must be a clearance of at least 3.175 mm between the rack protective ground and the internal signal ground of the board to ensure an adequate discharge spark gap. This way, electrostatic interference or other transient disturbances on the connector casing can be discharged into the rack protective earth, rather than interfering with the internal signal ground of the board.

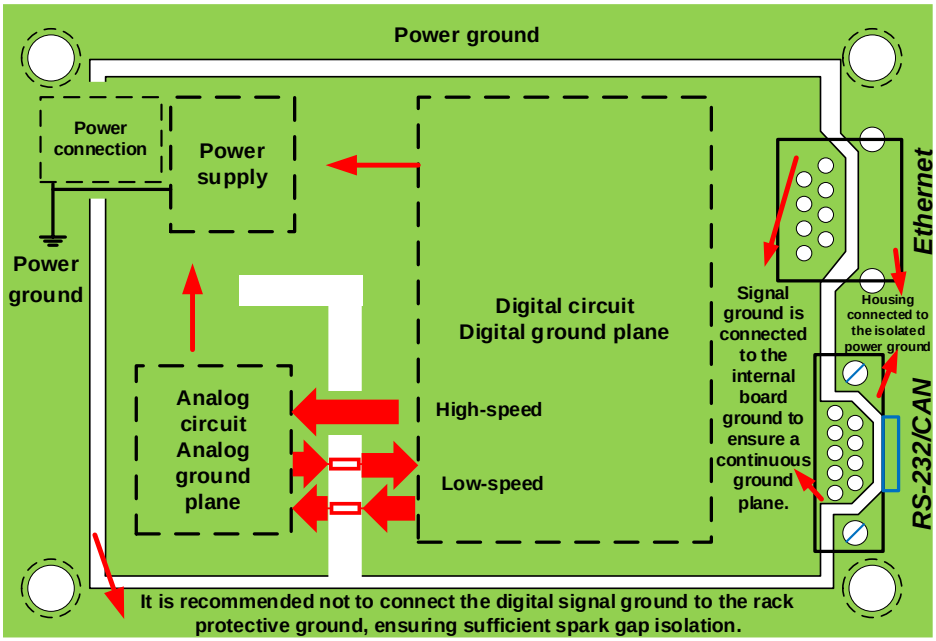
Figure 3-12. Rack connected to protective earth ground with split layout



As shown in ***Figure 3-13. Layout without external rack connection to protective ground***, isolation layers can still be used to isolate the ground. The power ground is placed at the point of lowest impedance relative to the internal circuit and other planar circuit layers. USB, Ethernet, RS232, and other connectors, including ground signal interfaces, can be placed on the internal signal ground of the board to ensure a continuous ground plane for connector interfaces. The housings of USB, Ethernet, RS232, and other connectors are connected to the isolated ground provided by the isolation layer. This layout ensures that electrostatic interference or other transient disturbances on the connector housings can dissipate through

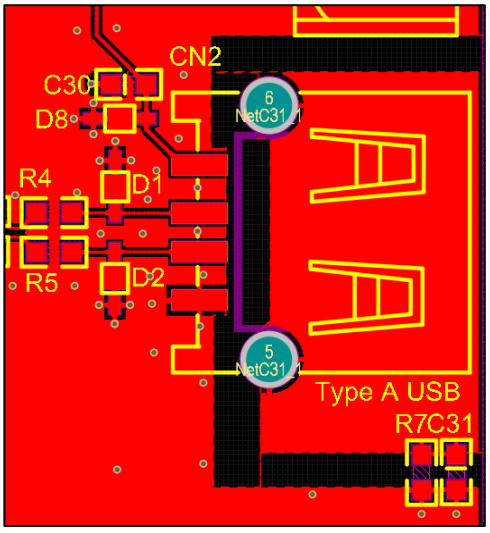
the power ground into the mains.

Figure 3-13. Layout without external rack connection to protective ground



As shown in ***Figure 3-14. Layout with localized ground splitting for interfaces***, in cases where the system board cannot use isolation layers to separately connect the power ground and interface ground due to space constraints, an isolation layer can be used to isolate a localized ground at the connector housing for USB, Ethernet, RS232, and similar interfaces. The shielding ground of the housing can then be connected to the internal ground of the system board via RC networks or ferrite beads. This layout ensures that electrostatic sparks on the interface shielding layer do not arc to the internal ground of the system board. It also allows electrostatic interference or other transient disturbances on the connector housing to be attenuated and suppressed before entering the internal signal ground of the system board.

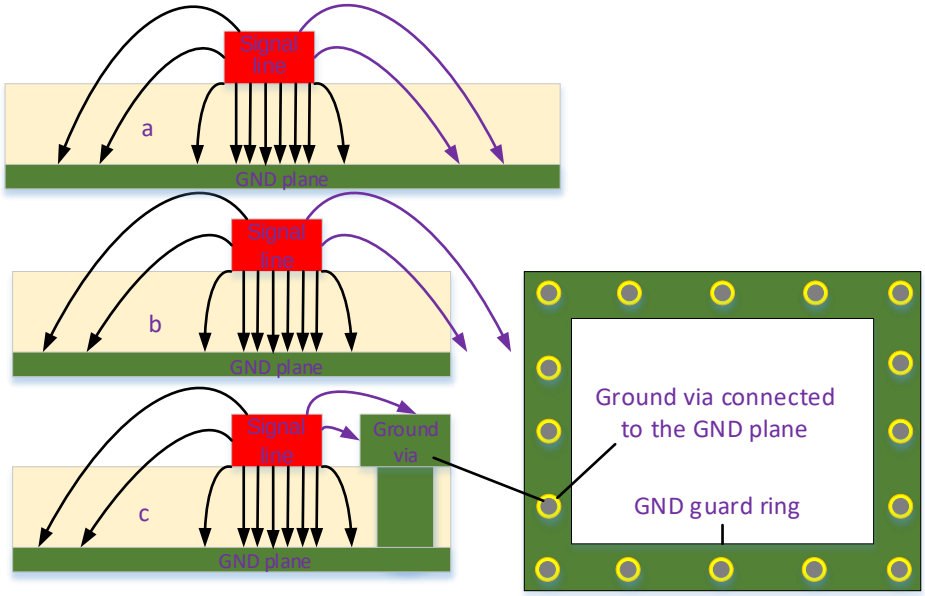
Figure 3-14. Layout with localized ground splitting for interfaces



3.6. PCB Edge Considerations

Near the edges of the PCB, the associated electric and magnetic field lines of signal traces are not well controlled, which not only makes them prone to electromagnetic radiation but also more susceptible to electromagnetic interference (EMI), electrostatic discharge (ESD), and electrical fast transient (EFT) events. Therefore, critical circuits and related traces that are sensitive to electromagnetic interference, such as clock signal lines, clock circuits, reset signal lines, and Vcore power lines, should be kept away from PCB edges.As shown in ***Figure 3-15. Electromagnetic field of the signal line at the board edge***, in diagram "a," when signal traces have sufficient distance from the PCB edge and are backed by a proper reference ground plane, most of the high-frequency energy associated with the traces will not radiate outside the board. Similarly, the impact of ESD, EMI, and EFT events on the signal traces will also be reduced. Typically, high-speed signal traces should maintain a distance of 10H from the board edge, where "H" represents the distance between the signal trace and its reference ground plane.As shown in diagram "b," if signal traces cannot avoid being close to the board edge, a guard ring can be created by adding vias connected to the ground plane along the board edge. In diagram "c," the spacing between adjacent vias is generally 1/10 of the high-frequency signal wavelength (λ) for the board-edge signal trace. The purpose of this guard ring is to absorb high-frequency energy radiating towards the PCB edge.

Figure 3-15. Electromagnetic field of the signal line at the board edge

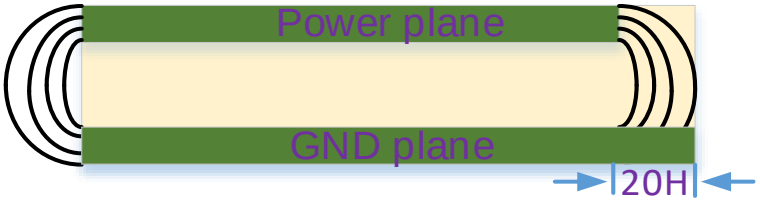


As shown in ***Figure 3-16. Electromagnetic field of the signal line at the board edge***, the left edge of a circuit board with a power plane following the 20H rule, for multilayer boards with a power plane, if the power plane at the edge of the circuit board is not recessed a certain distance relative to the GND plane, the power plane will radiate most of the electromagnetic field. As illustrated on the right edge of the circuit board in ***Figure 3-16. Electromagnetic field of the signal line at the board edge***, by recessing the power plane inward by a distance of 20H relative to the ground plane, the electromagnetic field radiation outside the board from

the power plane can be significantly reduced, where H represents the distance between the power plane and the reference ground plane.

In practical design, excessive inward contraction wastes routing space, so it is necessary to balance EMC and layout density. Therefore, in general scenarios, mid-to-low frequencies can be simplified to 3H-5H, while high-frequency scenarios require 5H-10H. Currently, an inward contraction of 1mm is suitable for most mid-to-low frequency designs in general scenarios, while 2-3mm inward contraction is recommended for high-frequency or high-speed scenarios, which can be further optimized through simulation.

Figure 3-16. Electromagnetic field of the signal line at the board edge



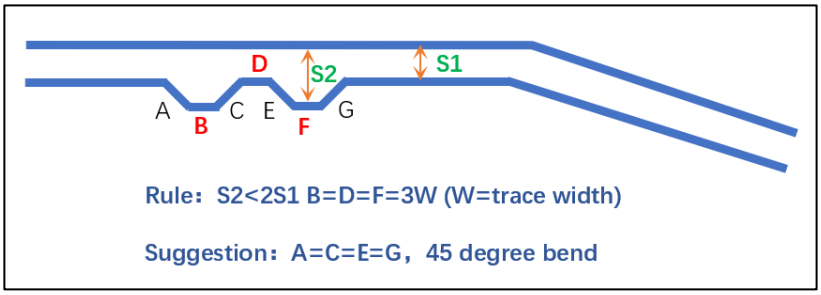
For the signal layer, the core principle is to ensure that there is a complete ground reference plane beneath the signal traces to avoid impedance discontinuities and edge radiation. The rule is that the projection of the signal layer's routing area must fall within the range of the ground plane. In general scenarios, the ground plane edge should extend outward by at least 0.5mm on each side of the signal layer routing. For high-frequency/sensitive signals (such as differential pairs and clock lines), the ground plane should extend outward by 1-2mm. Additionally, the signal traces should maintain a distance of at least 1mm from the board edge to prevent the loss of the reference ground plane due to manufacturing tolerances.

3.7. Differential Pair Routing Considerations

The most important matching rule for differential signal traces is equal length, ensuring minimal delay. If differential signal traces are of unequal length, the compensation principle is to compensate where the length difference occurs. For example, if the length difference occurs at the transmitting end, compensating with trace routing at the transmitting end can better maintain the synchronization of differential signals. If compensation is performed near the receiving end, it may introduce additional reflections or signal loss. Therefore, addressing the length difference as early as possible at its source is recommended. Additionally, to reduce impedance discontinuities caused by trace routing and ensure signal quality, it is advised to use the "3W-2S" rule for internal equal-length design. As shown in ***Figure 3-17. "3W-2S" Rule***, This rule refers to the constraints on the height and width of the compensation routing for the shorter trace when performing length matching in high-speed differential pairs. "3W" indicates that the spacing of the serpentine routing should be three times the trace width (W), while "2S" specifies that the farthest distance (S2) of the serpentine routing from the other trace should not exceed twice the internal spacing (S1) of the differential pair. Of course, this principle works well for high-speed signal designs within a certain rate range. However, in different design scenarios, such as high board density or limited routing space, designers may

find it difficult to strictly adhere to the "3W-2S" rule. In such cases, slightly adjusting the height and width of the compensation routing may not necessarily have a significant impact on signal quality.

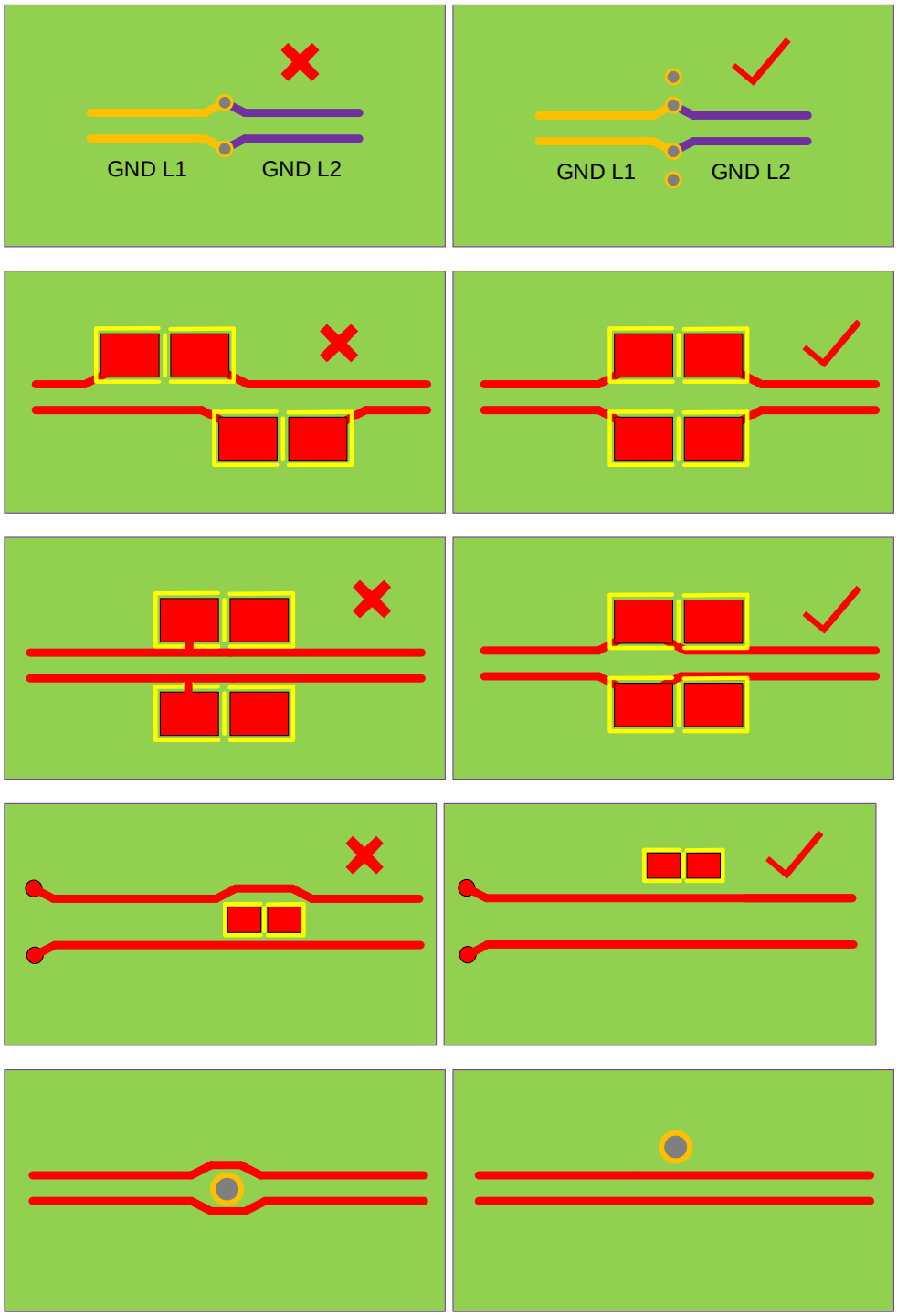
Figure 3-17. "3W-2S" Rule



Differential traces should be equal in length, equal in width, and closely spaced. Prioritize routing and ensure impedance matching. If equal length and equal spacing cannot be simultaneously achieved, prioritize matching the trace length. Impedance matching can be compensated by adding a resistor equal to the differential impedance value between the differential pair at the receiving end. Differential traces should be routed as close as possible to the ground plane, kept as short as possible, and avoid layer changes. The differential pair traces should remain on the same layer. Differential traces must have a complete reference ground plane and should not cross plane splits to ensure the shortest return path. Differential traces should minimize via corners, avoid right angles, and preferably use arcs or 135-degree angles to reduce impedance and reflection. Each differential signal pair should maintain a sufficient distance from other signal traces (especially high-speed signals and high-current interference signals) or other differential pairs. For example, the spacing between USB 2.0 differential pairs and other signal traces should be greater than or equal to 3W, while the spacing for USB 3.0 differential pairs should be greater than or equal to 5W. The spacing between USB differential pairs and power traces is recommended to be greater than or equal to 100 mil. It is advised that no parallel signal traces exist directly above or below the differential pair on adjacent signal layers. Differential pairs and other signal traces should ideally have GND isolation. Similarly, for high-speed connectors, ensure that each ground pad has at least one ground via, positioned as close to the pad as possible. The ground copper near the connector should ideally be spaced greater than or equal to 3W from the signal pins.

Prioritize differential pair routing and minimize layer changes. As shown in ***Figure 3-18. Symmetry Principle***, if routing involves layer changes and the reference planes before and after the layer change are ground planes, a companion via should be placed next to the signal via to ensure continuity of the return path. For differential signals, signal vias, return vias, and series/parallel resistors and capacitors should be placed symmetrically. For single-ended signals, it is recommended to place a return via next to the signal via to reduce the signal return path, enhance anti-interference capability, and lower radiation.

Figure 3-18. Symmetry Principle



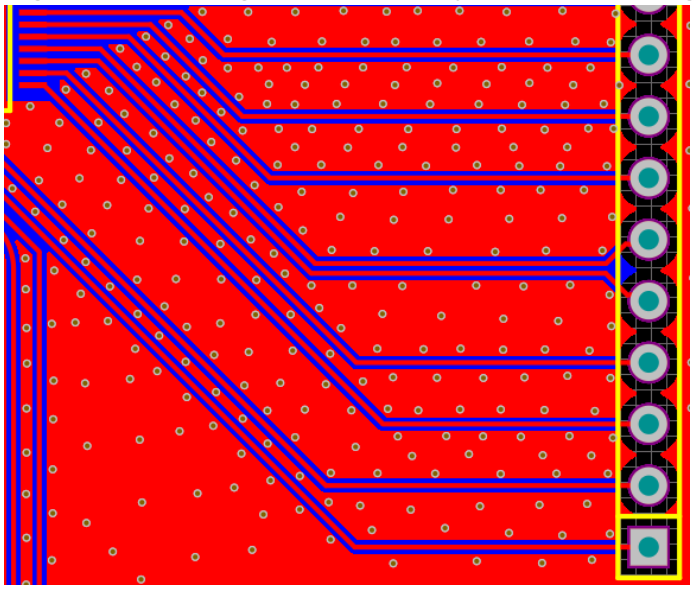
3.8. Display Interface Routing Considerations

The routing of display and other interfaces is typically long and consists of multiple parallel traces, making it susceptible to external electromagnetic interference and radiation, especially for signal traces near the display. To enhance the electromagnetic interference resistance of display and other interface routing and minimize radiation, the following rules are generally

applied for routing these interfaces.

- Due to the large number of traces required for display and other interfaces, which need to be routed in parallel to the interface, and the inevitable signal reflection caused by connections through the interface to related displays, it is recommended to keep the routing of display and other interfaces as short and straight as possible, minimize layer changes, and avoid unnecessary detours.
- As shown in ***Figure 3-19. Well-grounded display interface routing***, ensure that the routing path of display and other interfaces is accompanied by ground traces to couple noise from the interface traces to the ground. Additionally, accompanying ground traces between signals can effectively isolate crosstalk between signals and ensure a smaller return path for signals. If good ground isolation between signals cannot be guaranteed, it is best to maintain at least twice the trace width spacing between the traces.
- To further enhance resistance to external electromagnetic interference, RC circuits can be reserved along the routing of display and other interfaces. If the interface routing requires electrostatic testing, TVS and other protective circuits should be reserved at the point of electrostatic introduction.

Figure 3-19. Well-grounded display interface routing



4. Revision history

Table 4-1. Revision history

Revision No.	Description	Date
1.0	Intial Release	October 17, 2024
1.1	Add considerations for differential routing, display interface routing, and others	July 16, 2025

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