# GigaDevice Semiconductor Inc.

# GDSCN832xx

Datasheet

Revision 1.1

(May. 2025)

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# 1. General description

The GDSCN is a 2/3-port EtherCAT SubDevice controller with dual integrated Ethernet PHY which contain a full duplex 100BASE-TX transceiver and support 100Mbps (100BASE-TX) operation. The GDSCN supports HP Auto-MDIX, allowing the use of direct connect or cross-over LAN cables.

The GDSCN includes an EtherCAT SubDevice controller with 8K bytes of Process Data RAM(PDRAM) and 8 Fieldbus Memory Management Units (FMMUs). Each FMMU performs the task of mapping logical addresses to physical addresses. The EtherCAT SubDevice controller also includes 8 SyncManagers to allow the exchange of data between the EtherCAT main and the local application. Each SyncManager's direction and mode of operation is configured by the EtherCAT main. Two modes of operation are available: buffered mode or mailbox mode. In the buffered mode, both the local microcontroller and EtherCAT main can write to the device concurrently. The buffer within the GDSCN will always contain the latest data. If newer data arrives before the old data can be read out, the old data will be dropped. In mailbox mode, access to the buffer by the local microcontroller and the EtherCAT main is performed using handshakes, guaranteeing that no data will be dropped.

# 2. Device overview

## 2.1. Device information

**Table 2-1. GDSCN devices features and peripheral list**

| Feature | GDSCN |
|---|---|
| Ports | 3 ports(2PHYS,1MII) |
| FMMUs | 8 |
| SyncManagers | 8 |
| Process data RAM(PDRAM) | 8KB |
| Distributed Clocks | 64bit |
| Process Data Interfaces | Digital I/O<br>On-chip bus(SPI,EXMC) |
| Power supply | 1.1V Integrated voltage regulator for logic core/<br>2.5V Ethernet magnetics/<br>3.3V power supply voltage |
| I/O | 1.8V~3.3V compatible I/O |

## 2.2. Block diagram

**Figure 2-1. GDSCN system diagram**

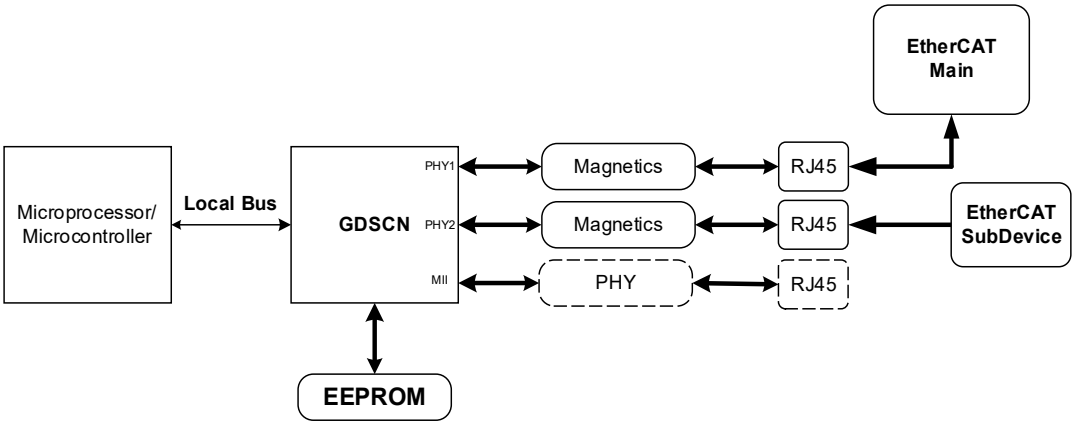
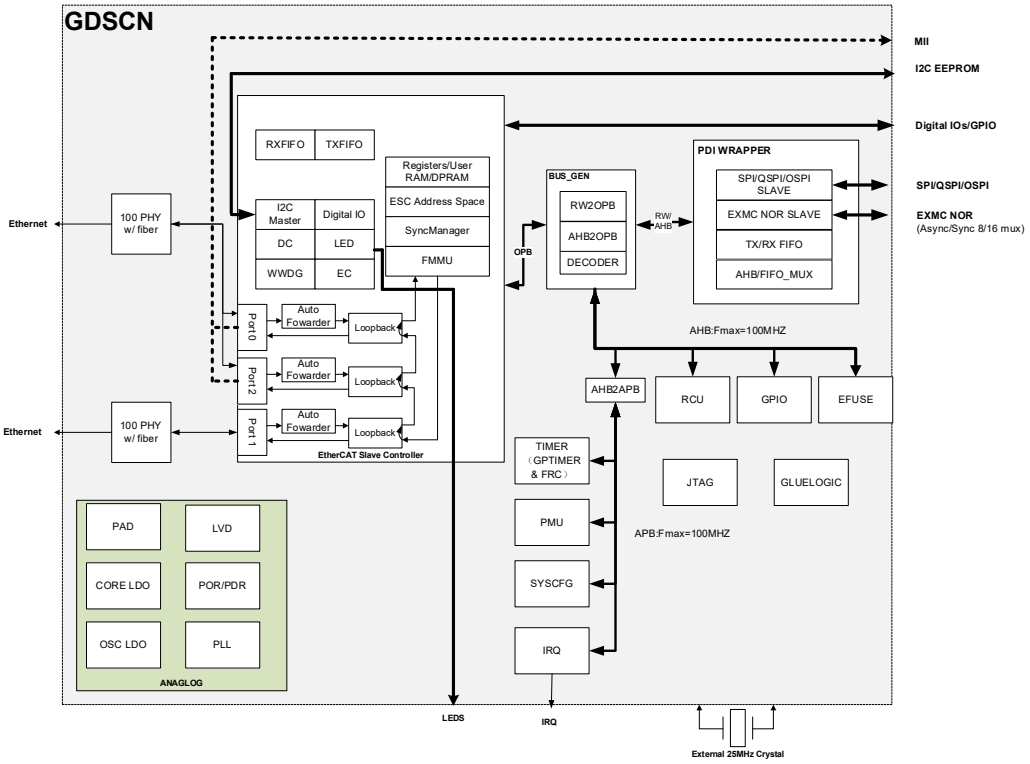
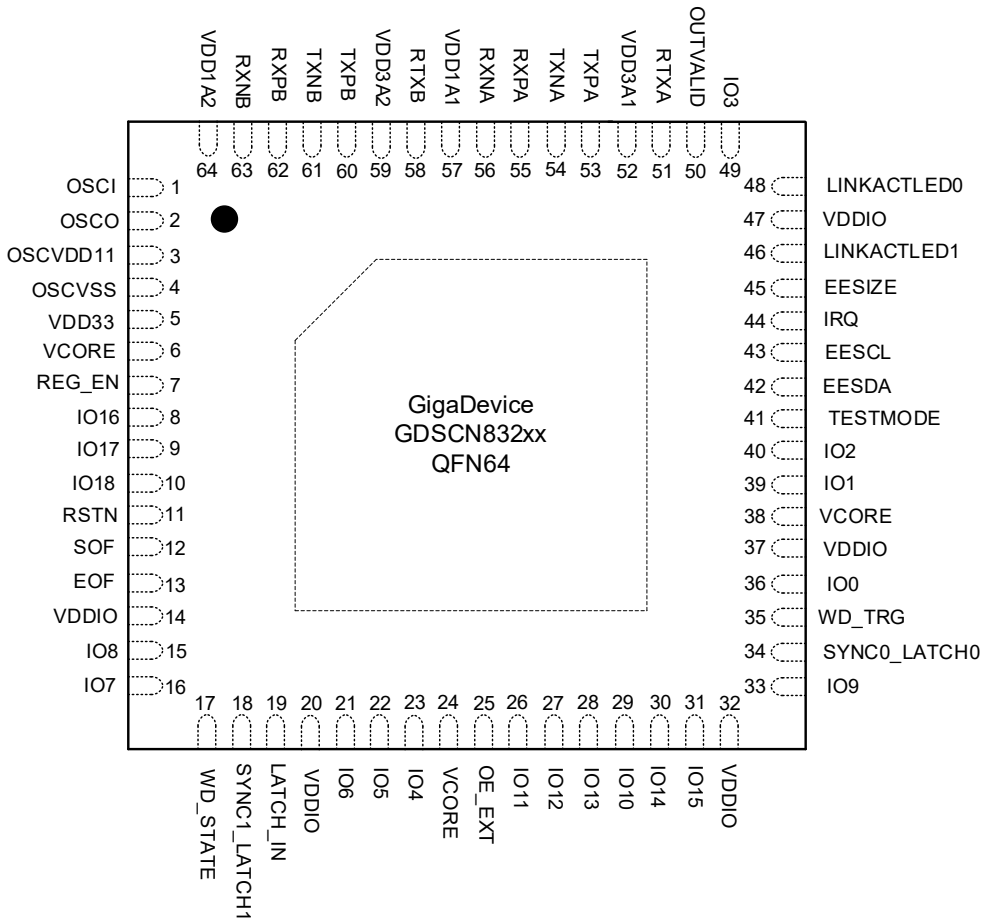



**Figure 2-2. GDSCN block diagram**



## 2.3. Pinouts and pin assignment

**Figure 2-3. GDSCN QFN64 pinouts**




## 2.4. Memory map

**Table 2-2. GDSCN memory map**

| Pre-defined Regions | Address | Peripherals |
|---|---|---|
| EtherCAT | 0x0000 | Type |
| | 0x0001 | Revision |
| | 0x0002 - 0x0003 | Build |
| | 0x0004 | FMMUs Supported |
| | 0x0005 | SyncManagers Supported |
| | 0x0006 | RAM Size |
| | 0x0007 | Port Descriptor |
| | 0x0008 - 0x0009 | ESC Features Supported |

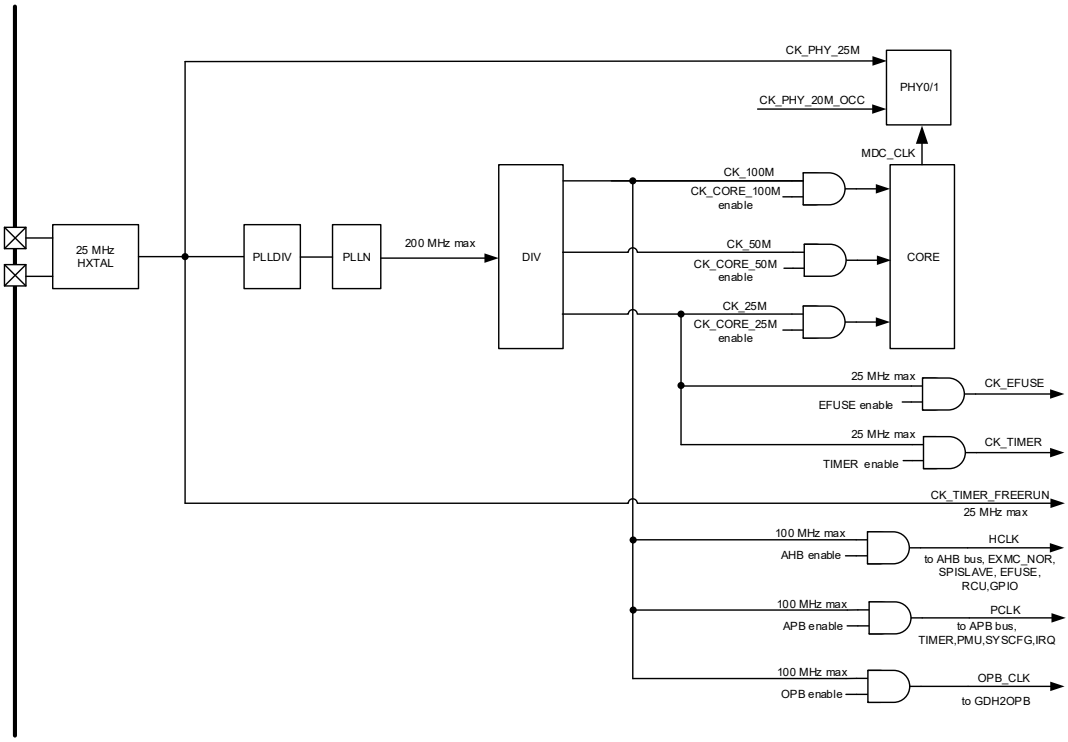
| Pre-defined Regions | Address | Peripherals |
|---|---|---|
| | 0x0010 - 0x0011 | Configured Station Address |
| | 0x0012 - 0x0013 | Configured Station Alias |
| | 0x0013 - 0x001F | Reserved |
| | 0x0020 | Write Register Enable |
| | 0x0021 | Write Register Protection |
| | 0x0022 - 0x002F | Reserved |
| | 0x0030 | ESC Write Enable |
| | 0x0031 | ESC Write Protection |
| | 0x0032 - 0x003F | Reserved |
| | 0x0040 | ESC Reset ECAT |
| | 0x0041 | ESC Reset PDI |
| | 0x0042 - 0x0FF | Reserved |
| | 0x0100 - 0x0103 | ESC DL Control |
| | 0x0104 - 0x0107 | Reserved |
| | 0x0108 - 0x0109 | Physical Read/Write Offset |
| | 0x0110 - 0x0111 | ESC DL Status |
| | 0x0112 - 0x011F | Reserved |
| | 0x0120 - 0x0121 | AL Control |
| | 0x0122 - 0x012F | Reserved |
| | 0x0130 - 0x0131 | AL Status |
| | 0x0132 - 0x0133 | Reserved |
| | 0x0134 - 0x0135 | AL Status Code |
| | 0x0136 - 0x0137 | Reserved |
| | 0x0138 | RUN LED Override |
| | 0x0139 | Reserved |
| | 0x0140 | PDI Control |
| | 0x0141 | ESC Configuration |
| | 0x0142 - 0x0143 | ASIC Configuration |
| | 0x0144 - 0x0145 | RESERVED Register |
| | 0x0146 - 0x014F | Reserved |
| | 0x0150 | PDI Configuration |
| | 0x0151 | Sync/Latch PDI Configuration |
| | 0x0152 - 0x0153 | Extended PDI Configuration |
| | 0x0154 - 0x01FF | Reserved |
| | 0x0200 - 0x0201 | ECAT Event Mask |
| | 0x0202 - 0x0203 | Reserved |
| | 0x0204 - 0x0207 | PDI AL Event Mask |
| | 0x0208 - 0x0209 | Reserved |
| | 0x0210 - 0x0211 | ECAT Event Request |
| | 0x0212 - 0x021F | Reserved |
| | 0x0220 - 0x0223 | AL Event Request |

| Pre-defined Regions | Address | Peripherals |
|---|---|---|
| | 0x0223 - 0x022F | Reserved |
| | 0x0300 - 0x0307 | RX Error Counter |
| | 0x0308 - 0x030B | Forwarded RX Error Counter |
| | 0x030C | ECAT Processing Unit Error Counter |
| | 0x030D | PDI Error Counter |
| | 0x030E | PDI Error Code |
| | 0x030F | Reserved |
| | 0x0310 - 0x0313 | Lost Link Counter |
| | 0x0314 - 0x03FF | Reserved |
| | 0x0400 - 0x0401 | Watchdog Divider |
| | 0x0410 - 0x0411 | Watchdog Time PDI |
| | 0x0420 - 0x0421 | Watchdog Time Process Data |
| | 0x0440 - 0x0441 | Watchdog Status Process Data |
| | 0x0442 | Watchdog Counter Process Data |
| | 0x0443 | Watchdog Counter PDI |
| | 0x0444 - 0x04FF | Reserved |
| | 0x0500 | EEPROM Configuration |
| | 0x0501 | EEPROM PDI Access State |
| | 0x0502 - 0x0503 | EEPROM Control/Status |
| | 0x0504 - 0x0507 | EEPROM Address |
| | 0x0508 - 0x050B | EEPROM Data |
| | 0x050C- 0x050F | Reserved |
| | 0x0510 - 0x0511 | MII Management Control/Status |
| | 0x0512 | PHY Address |
| | 0x0513 | PHY Register Address |
| | 0x0514 - 0x0515 | PHY DATA |
| | 0x0516 | MII Management ECAT Access State |
| | 0x0517 | MII Management PDI Access State |
| | 0x0518 - 0x051B | PHY Port Status |
| | 0x051C - 0x05FF | Reserved |
| | 0x0600 - 0x06FF | FMMU |
| | 0x0700 - 0x07FF | Reserved |
| | 0x0800 - 0x087F | SyncManager |
| | 0x0880 - 0x08FF | Reserved |
| | 0x0900 - 0x09FF | Distributed Clocks (DC) |
| | 0x0A00 - 0x0AFF | Reserved |
| | 0x0E00 - 0x0E07 | Product ID |
| | 0x0E08 - 0x0E0F | Vendor ID |
| | 0x0E10 - 0x0EFF | Reserved |
| | 0x0F00 - 0x0F03 | Digital I/O Output Data |
| | 0x0F04 - 0x0F0F | Reserved |

| Pre-defined Regions | Address | Peripherals |
|---|---|---|
| | 0x0F10 - 0x0F17 | General Purpose Outputs |
| | 0x0F18 - 0x0F1F | General Purpose Inputs |
| | 0x0F20 - 0x0F7F | Reserved |
| | 0x0F80 - 0x0FFF | User RAM |
| | 0x1000 - 0x2FFF | Process Data RAM |
| Peripheral | 0x3300 - 0x33FF | AHB2OPB Bridge |
| | 0x3400 - 0x34FF | RCU |
| | 0x3500 - 0x35FF | GPIO |
| | 0x3700 - 0x37FF | PMU |
| | 0x3800 - 0x38FF | TIMER |
| | 0x3900 - 0x39FF | SYSCFG |
| | 0x3A00 - 0x3AFF | IRQ |

## 2.5. Clock tree

**Figure 2-4. GDSCN clock tree**




**Legend:**

HXTAL: High speed crystal oscillator

## 2.6. Pin definitions

### 2.6.1. GDSCN QFN64 pin definitions

**Table 2-3. GDSCN QFN64 pin definitions**

| QFN64 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description** |
| OSCI | 1 | | | Default: OSCI |
| OSCO | 2 | | | Default: OSCO |
| OSCVDD11 | 3 | P | - | Default: OSCVDD11 |
| OSCVSS | 4 | P | - | Default: OSCVSS |
| VDD33 | 5 | P | - | Default: VDD33 |
| VCORE | 6 | P | - | Default: VCORE |
| REG_EN | 7 | I/O | 5VT | Default: REG_EN<br>Additional: REG_EN |
| IO16 | 8 | I/O | 5VT | Default: IO16<br>Alternate: SIO4, MCU_PDI_TYPE<br>Additional: VBG11 |
| IO17 | 9 | I/O | 5VT | Default: IO17<br>Alternate: SIO5, EFUSE_LDO_BYP |
| IO18 | 10 | I/O | 5VT | Default: IO18<br>Alternate: SIO6, PHYRST_MODE |
| RSTN | 11 | I/O | | Default: RSTN<br>Additional: RSTN |
| SOF | 12 | I/O | 5VT | Default: SOF<br>Alternate: EXMC_AD2, PDI_DIGIO_SOF, SIO2 |
| EOF | 13 | I/O | 5VT | Default: EOF<br>Alternate: EXMC_AD1, PDI_DIGIO_EOF, SIO1 |
| VDDIO | 14 | P | | Default: VDDIO |
| IO8 | 15 | I/O | 5VT | Default: IO8<br>Alternate: EXMC_AD14, PDI_DIGIO8, PDI_GPIO8, MII0_TXD3, MII2_TXD3, TX_SHIFT1 |
| IO7 | 16 | I/O | 5VT | Default: IO7<br>Alternate: EXMC_AD13, PDI_DIGIO7, PDI_GPIO7, MII0_TXD2, MII2_TXD2, TX_SHIFT0 |
| WD_STATE | 17 | I/O | 5VT | Default: WD_STATE<br>Alternate: EXMC_AD0, PDI_DIGIO_WD_STATE, SIO0 |
| SYNC1_LATCH1 | 18 | I/O | 5VT | Default: SYNC1_LATCH1<br>Alternate: SYNC1, LATCH1 |
| LATCH_IN | 19 | I/O | 5VT | Default: LATCH_IN<br>Alternate: EXMC_AD9, PDI_DIGIO_LATCH_IN, SCK |
| VDDIO | 20 | P | - | Default: VDDIO |

| QFN64 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description** |
| IO6 | 21 | I/O | 5VT | Default: IO6<br>Alternate: EXMC_AD12, PDI_DIGIO6, PDI_GPIO6, MII0_TXD1, MII2_TXD1 |
| IO5 | 22 | I/O | 5VT | Default: IO5<br>Alternate: EXMC_AD11, PDI_DIGIO5, PDI_GPIO5, MII0_TXD0, MII2_TXD0 |
| IO4 | 23 | I/O | 5VT | Default: IO4<br>Alternate: EXMC_AD10, PDI_DIGIO4, PDI_GPIO4, MII0_TX_EN, MII2_TX_EN |
| VCORE | 24 | P | - | Default: VCORE<br>Additional: VDDCR |
| OE_EXT | 25 | I/O | 5VT | Default: OE_EXT<br>Alternate: EXMC_NL, PDI_DIGIO_OE_EXT, MII_CLK25, SIO7 |
| IO11 | 26 | I/O | 5VT | Default: IO11<br>Alternate: EXMC_CLK, PDI_DIGIO11, PDI_GPIO11, MII2_RX_DV, MII0_RX_DV |
| IO12 | 27 | I/O | 5VT | Default: IO12<br>Alternate: EXMC_NWAIT, PDI_DIGIO12, PDI_GPIO12, MII0_RXD0, MII2_RXD0 |
| IO13 | 28 | I/O | 5VT | Default: IO13<br>Alternate: EXMC_NE, PDI_DIGIO13, PDI_GPIO13, MII0_RXD1, MII2_RXD1 |
| IO10 | 29 | I/O | 5VT | Default: IO10<br>Alternate: PDI_DIGIO10, PDI_GPIO10, MII0_LINKPOL, LINKACTLED2 |
| IO14 | 30 | I/O | 5VT | Default: IO14<br>Alternate: EXMC_NWE, PDI_DIGIO14, PDI_GPIO14, MII0_RXD2, MII2_RXD2 |
| IO15 | 31 | I/O | 5VT | Default: IO15<br>Alternate: EXMC_NOE, PDI_DIGIO15, PDI_GPIO15, MII0_RXD3, MII2_RXD3 |
| VDDIO | 32 | P | - | Default: VDDIO |
| IO9 | 33 | I/O | 5VT | Default: IO9<br>Alternate: EXMC_AD15, PDI_DIGIO9, PDI_GPIO9, MII0_RX_ER, MII2_RX_ER |
| SYNC0_LATCH0 | 34 | I/O | 5VT | Default: SYNC0_LATCH0<br>Alternate: SYNC0, LATCH0 |
| WD_TRIG | 35 | I/O | 5VT | Default: WD_TRIG<br>Alternate: EXMC_AD3, PDI_DIGIO_WD_TRIG, SIO3 |
| IO0 | 36 | I/O | 5VT | Default: IO0<br>Alternate: EXMC_AD6, PDI_DIGIO0, PDI_GPIO0, MII0_RX_CLK, MII2_RX_CLK |
| VDDIO | 37 | P | - | Default: VDDIO<br>Additional: VDDIO |

| QFN64 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description** |
| VCORE | 38 | P | - | Default: VCORE<br>Additional: VDDCR |
| IO1 | 39 | I/O | 5VT | Default: IO1<br>Alternate: EXMC_AD7, PDI_DIGIO1, PDI_GPIO1, MII_CLK |
| IO2 | 40 | I/O | 5VT | Default: IO2<br>Alternate: EXMC_AD8, PDI_DIGIO2, PDI_GPIO2, MII_DATA |
| TESTMODE | 41 | I/O | 5VT | Default: TESTMODE<br>Alternate: TESTMODE |
| EESDA | 42 | I/O | 5VT | Default: EESDA<br>Alternate: EEPROM_DATA, JTAG_TMS |
| EESCL | 43 | I/O | 5VT | Default: EESCL<br>Alternate: EEPROM_CLK, JTAG_TCK |
| IRQ | 44 | I/O | 5VT | Default: IRQ<br>Alternate: IRQ |
| EESIZE | 45 | I/O | 5VT | Default: EESIZE<br>Alternate: EEPROM_SIZE, RUNLED |
| LINKACTLED1 | 46 | I/O | 5VT | Default: LINKACTLED1<br>Alternate: LINKACTLED1, JTAG_TDI, CHIP_MODE1 |
| VDDIO | 47 | P | - | Default: VDDIO<br>Additional: VDDIO |
| LINKACTLED0 | 48 | I/O | 5VT | Default: LINKACTLED0<br>Alternate: LINKACTLED0, JTAG_TDO, CHIP_MODE0 |
| IO3 | 49 | I/O | 5VT | Default: IO3<br>Alternate: EXMC_AD4, PDI_DIGIO3, PDI_GPIO3, MII2_LINK, MII0_LINK<br>Additional: VCORE_REF |
| OUTVALID | 50 | I/O | 5VT | Default: OUTVALID<br>Alternate: EXMC_AD5, PDI_DIGIO_OUTVALID, SCS |
| RTXA | 51 | I/O | | Default: RTXA<br>Additional: RTX_P1 |
| VDD3A1 | 52 | P | - | Default: VDD3A1<br>Additional: VDA3PL_P1 |
| TXPA | 53 | I/O | | Default: TXPA<br>Additional: TXP_P1 |
| TXNA | 54 | I/O | | Default: TXNA<br>Additional: TXN_P1 |
| RXPA | 55 | I/O | | Default: RXPA<br>Additional: RXP_P1 |
| RXNA | 56 | I/O | | Default: RXNA<br>Additional: RXN_P1 |
| VDD1A1 | 57 | P | - | Default: VDD1A1 |

| QFN64 | | | | |
|---|---|---|---|---|
| **Pin Name** | **Pins** | **Pin Type(1)** | **I/O Level(2)** | **Functions description** |
| | | | | Additional: VDD1A_P1 |
| RTXB | 58 | I/O | | Default: RTXB<br>Additional: RTX_P2 |
| VDD3A2 | 59 | P | - | Default: VDD3A2<br>Additional: VDA3PL_P2 |
| TXPB | 60 | I/O | | Default: TXPB<br>Additional: TXP_P2 |
| TXNB | 61 | I/O | | Default: TXNB<br>Additional: TXN_P2 |
| RXPB | 62 | I/O | | Default: RXPB<br>Additional: RXP_P2 |
| RXNB | 63 | I/O | | Default: RXNB<br>Additional: RXN_P2 |
| VDD1A2 | 64 | P | - | Default: VDD1A2<br>Additional: VDD1A_P2 |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

### 2.6.2. GDSCN pin alternate functions

**Table 2-4.GDSCN alternate functions summary**

| Pin Name | EXMC | Digital IO | OSPI (8-wire) + GPIO | QSPI (4-wire) + MII (4-wire) | QSPI (4-wire) + MII |
|---|---|---|---|---|---|
| IO16 | MCU_PDITYPE | MCU_PDITYPE | SIO4/ MCU_PDITYPE | MCU_PDITYPE | MCU_PDITYPE |
| IO17 | EFUSE_LDO_BYP | EFUSE_LDO_BYP | SIO5/ EFUSE_LDO_BYP | EFUSE_LDO_BYP | EFUSE_LDO_BYP |
| IO18 | PHYRST_MODE | PHYRST_MODE | SIO6/ PHYRST_MODE | PHYRST_MODE | PHYRST_MODE |
| RSTn | RSTn | RSTn | RSTn | RSTn | RSTn |
| SOF | EXMC_AD2 | PDI_DIGIO_SOF | SIO2 | SIO2 | SIO2 |
| EOF | EXMC_AD1 | PDI_DIGIO_EOF | SIO1 | SIO1 | SIO1 |
| IO8 | EXMC_AD14 | PDI_DIGIO8 | PDI_DIGIO8 | MII2_TXD3/ TX_SHIFT1 | MII0_TXD3/ TX_SHIFT1 |
| IO7 | EXMC_AD13 | PDI_DIGIO7 | PDI_DIGIO7 | MII2_TXD2/ TX_SHIFT0 | MII0_TXD2/ TX_SHIFT0 |
| WD_STATE | EXMC_AD0 | PDI_DIGIO_WD_STATE | SIO0 | SIO0 | SIO0 |

| Pin Name | EXMC | Digital IO | OSPI (8-wire) + GPIO | QSPI (4-wire) + MII (4-wire) | QSPI (4-wire) + MII |
|---|---|---|---|---|---|
| SYNC1_LATCH1 | SYNC1/ LATCH1 | SYNC1/ LATCH1 | SYNC1/ LATCH1 | SYNC1/ LATCH1 | SYNC1/ LATCH1 |
| LATCH_IN | EXMC_AD9 | PDI_DIGIO_LATCH_IN | SCK | SCK | SCK |
| IO6 | EXMC_AD12 | PDI_DIGIO6 | PDI_DIGIO6 | MII2_TXD1 | MII0_TXD1 |
| IO5 | EXMC_AD11 | PDI_DIGIO5 | PDI_DIGIO5 | MII2_TXD0 | MII0_TXD0 |
| IO4 | EXMC_AD10 | PDI_DIGIO4 | PDI_DIGIO4 | MII2_TX_EN | MII0_TX_EN |
| OE_EXT | EXMC_NL | PDI_DIGIO_OE_EXT | SIO7 | MII_CLK25 | MII_CLK25 |
| IO11 | EXMC_CLK | PDI_DIGIO11 | PDI_GPIO11 | MII2_RX_DV | MII0_RX_DV |
| IO12 | EXMC_NWAIT | PDI_GPIO12 | PDI_GPIO12 | MII2_RXD0 | MII0_RXD0 |
| IO13 | EXMC_NE | PDI_GPIO13 | PDI_GPIO13 | MII2_RXD1 | MII0_RXD1 |
| IO10 | | PDI_GPIO10 | PDI_GPIO10 | MII_LINKPOL/ LINKACTLED2 | MII_LINKPOL/ LINKACTLED2 |
| IO14 | EXMC_NWE | PDI_GPIO14 | PDI_GPIO14 | MII2_RXD2 | MII0_RXD2 |
| IO15 | EXMC_NOE | PDI_GPIO15 | PDI_GPIO15 | MII2_RXD3 | MII0_RXD3 |
| IO9 | EXMC_AD15 | PDI_GPIO9 | PDI_GPIO9 | MII2_RX_ER | MII0_RX_ER |
| SYNC0_LATCH0 | SYNC0/ LATCH0 | SYNC0/ LATCH0 | SYNC0/ LATCH0 | SYNC0/ LATCH0 | SYNC0/ LATCH0 |
| WD_TRIG | EXMC_AD3 | PDI_DIGIO_WD_TRIG | SIO3 | SIO3 | SIO3 |
| IO0 | EXMC_AD6 | PDI_DIGIO0 | PDI_DIGIO0 | MII2_RX_CLK | MII0_RX_CLK |
| IO1 | EXMC_AD7 | PDI_DIGIO1 | PDI_DIGIO1 | MII_CLK | MII_CLK |
| IO2 | EXMC_AD8 | PDI_DIGIO2 | PDI_DIGIO2 | MII_DATA | MII_DATA |
| TESTMODE | TESTMODE | TESTMODE | TESTMODE | TESTMODE | TESTMODE |
| EESDA | EEPROM_DATA /JTAG_TMS | EEPROM_DATA/JTAG_TMS | EEPROM_DATA/ JTAG_TMS | EEPROM_DATA /JTAG_TMS | EEPROM_DATA/JTAG_TMS |
| EESCL | EEPROM_CLK /JTAG_TCK | EEPROM_CLK /JTAG_TCK | EEPROM_CLK /JTAG_TCK | EEPROM_CLK /JTAG_TCK | EEPROM_CLK /JTAG_TCK |
| IRQ | IRQ | IRQ | IRQ | IRQ | IRQ |
| EESIZE | EEPROM_SIZE/ RUNLED | EEPROM_SIZE/RUNLED | EEPROM_SIZE/ RUNLED | EEPROM_SIZE/ RUNLED | EEPROM_SIZE/RUNLED |
| LINKACTLE | LINKACTLED | LINKACTLED1/ | LINKACTLED | LINKACTLED | LINKACTLED1/ |

| Pin Name | EXMC | Digital IO | OSPI (8-wire) + GPIO | QSPI (4-wire) + MII (4-wire) | QSPI (4-wire) + MII |
|---|---|---|---|---|---|
| D1 | 1/ JTAG_TDI/ CHIP_MODE1 | JTAG_TDI/ CHIP_MODE1 | 1/ JTAG_TDI/ CHIP_MODE1 | 1/ JTAG_TDI/ CHIP_MODE1 | JTAG_TDI/ CHIP_MODE1 |
| LINKACTLED0 | LINKACTLED0/ JTAG_TDO/ CHIP_MODE0 | LINKACTLED0/ JTAG_TDO/ CHIP_MODE0 | LINKACTLED0/ JTAG_TDO/ CHIP_MODE0 | LINKACTLED0/ JTAG_TDO/ CHIP_MODE0 | LINKACTLED0/ JTAG_TDO/ CHIP_MODE0 |
| IO3 | EXMC_AD4 | PDI_DIGIO3 | PDI_GPIO3 | MII2_LINK | MII0_LINK |
| OUTVALID | EXMC_AD5 | PDI_DIGIO_OUTVALID | SCS | SCS | SCS |

# 3. Functional description

## 3.1. EtherCAT SubDevice Controller(ESC)

- Port support: 2 internal phy port and 1 external MII.
- 8 Fieldbus Memory Management Units (FMMUs).
- 8KB PDRAM.
- 64-bit distributed clock, support allows synchronization with other EtherCAT devices.
- 8 Syncmanager entities.
- DC synchronization less than 1us.

The EtherCAT SubDevice Controller (ESC), licensed from Beckhoff Automation, It takes care of the EtherCAT communication as an interface between the EtherCAT fieldbus and the sub application.

## 3.2. Clock, reset and supply management

- Supports 25Mhz HSE clock.
- PLL: 25Mhz 8x frequency to achieve 200Mhz clock
- System clock: PLL 2 frequency division, fixed 100Mhz
- AHB/APB clock: Fixed 100Mhz
- Other normally open clock: 50Mhz, 25Mhz free running clock, for special functions
- 1.1 to 3.3V application supply and I/Os.

The Clock Control Unit (CCU) provides an external High Speed crystal oscillator (HXTAL) and a phase-locked loop (PLL). This clock is usually provided by the OSCIN and OSCOUT of the passive 25MHz crystal oscillator or by the OSCIN pin of the single-ended 25MHz clock source driver. See ***Figure 2-4. GDSCN clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls two kinds of reset: system reset and module reset. System reset includes power-on reset (POR), external pin reset (NRST) and EtherCAT system reset, which can reset all circuits in the device. Module reset includes digital reset, PHY reset and EtherCAT core reset, which can reset each corresponding module.

Power supply schemes:

- $V_{DDIO}$ range: 1.8 to 3.3 V, external power supply for I/Os. Provided externally through VDDIO pins.
- $V_{DD33}$, $V_{DD3A1}$, $V_{DD3A2}$: 3.3 V, external power supplies for Internal 1.1V Core Regulator and 1.1V Oscillator Regulator, PHYA and PHYB.
- $V_{CORE}$, $V_{DD1A1}$, $V_{DD1A2}$: 1.1 V, power supply for I/Os, Core logic and PHY digital, PHYA and PHYB.

## 3.3. General-purpose inputs/outputs (GPIOs)

- Up to 35 GPIOs, 8 kinds of communication modes to can be choose
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 35 general purpose I/O pins (GPIO) in GDEHC to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

## 3.4. Power saving modes

The GDSCN supports four types of device level and three types of module level power saving modes, device level power saving modes including MOD0, MOD1, MOD2 and MOD3, module level power saving modes including EtherCAT clock management, PHY power management and the LED pins power management. These modes reduce the power consumption and allow the application to achieve the best tradeoff among the conflicting demands of device operating time, speed and power consumption.

The device supports three types of module level power saving modes:

- The ECATCLKDIS bit in PMU_CTL0 register can use to disable EtherCAT core clock.
- PHY power management
  - PHY A and B ED power down management, support auto ED power down.
  - Common power down management.
- LEDs output management
  - The LEDOUTDIS bit in PMU_CTL0 register can use to disable LEDs output.
  - The LEDMODCFG bit in PMU_CTL0 register can use to configure LEDs working mode (take effect only when LEDOUTDIS is set).
  - The LEDINACT bit in PMU_CTL0 register can use to configure the inactive state when LEDs work in push-pull mode (take effect only when LEDOUTDIS is set).

## 3.5. Timers and Free-Running Counter (TIMER and FRC)

- 16-bit down counter
- Generate periodic system interrupts
- Resolution is 100us

The basic timer module has a 16-bit counter that can be used as an unsigned counter. The basic timer can be configured to generate interrupts. The resolution of basic timer is 100 μs.

The Free-Running Counter has a 32-bit counter that can be used as an unsigned counter.The counter clock is 25MHz.

- 32-bit up counter
- Driven by free running 25Mhz clock

## 3.6. Process Data Interface (PDI) Wrapper

- Support SPI slave and EXMC mode.
- Supports three types SPI, QSPI, OSPI slave.
- EXMC supports both async and sync modes, 8-bit and 16-bit.

The Process Data Interface (PDI) Wrapper realizes the connection between ESC system bus and ESC core. through the AHB2OPB to connect. The SPI SLAVE and EXMC have only one work at the same time, which is selected by the pad of IO16(MCU_PDITYPE).

## 3.7. Ethernet PHYS

- Two internal phys connect to ESC core
- Supports MII interfaces, Auto negotiation and parallel detection capability for automatic speed and duplex selection

The GDSCN contains PHYs A and B, there are identical in functionality. The PHY A connects to the EtherCAT port 0 or 2. The PHY B connects to EtherCAT port 1. These PHYs interface with their respective MAC via an internal MII interface. The PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full duplex 100 Mbps (100BASE-TX / 100BASE-FX) Ethernet operation. All PHYs registers follow the IEEE 802.3 specified MII management register set and are fully configurable.

## 3.8. Package and operation temperature

- QFN64 (GDSCN832R2U6) & QFN64 (GDSCN832R2U7).
- Operation temperature range: -40°C to +105°C (industrial level).

# 4. Electrical characteristics

## 4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4-1. Absolute maximum ratings(1)(3)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD1Ax}$ | Analog 1.1V power for Ethernet PHY | $V_{SS}$ - 0.3 | $V_{SS}$ + 1.21 | V |
| $V_{OSCVDD11}$ | Internal 1.1V oscillator supply voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 1.21 | V |
| $V_{CORE}$ | Digital core supply voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 1.21 | V |
| $V_{DD3Ax}$ | Analog 3.3V power for Ethernet PHY(2) | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{DD33}$ | Supply voltage for the internal regulators(2) | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{DDIO}$ | IO supply voltage(2) | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{OSCI}$ | oscillator supply voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{IN}$ | Input voltage on 5VT I/O(4) | $V_{SS}$ - 0.3 | $V_{DDIO}$ + 3.6 | V |
| | Input voltage on other I/O | $V_{SS}$ - 0.3 | $V_{DD}$ + 0.3 | |
| $T_A$ | Operating temperature range for grade 6 device | -40 | 85 | °C |
| | Operating temperature range for grade 7 device | -40 | 105 | |
| $P_D$(5) | Power dissipation at $T_A$ = 85°C of QFN64(6) | — | 1688 | mW |
| | Power dissipation at $T_A$ = 105°C of QFN64(6) | — | 844 | |
| $T_{STG}$ | Storage temperature range | -65 | 150 | °C |
| $T_J$ | Maximum junction temperature | — | 125 | °C |

(1) Value guaranteed by design, not 100% tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) The device junction temperature must be kept below maximum $T_J$.

(4) $V_{IN}$ maximum value cannot exceed 5.5 V.

(5) If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$.

(6) For grade 7 devices, the parameter of $T_A$ = 105°C, For grade 3 device, the parameter of $T_A$ = 125°C.

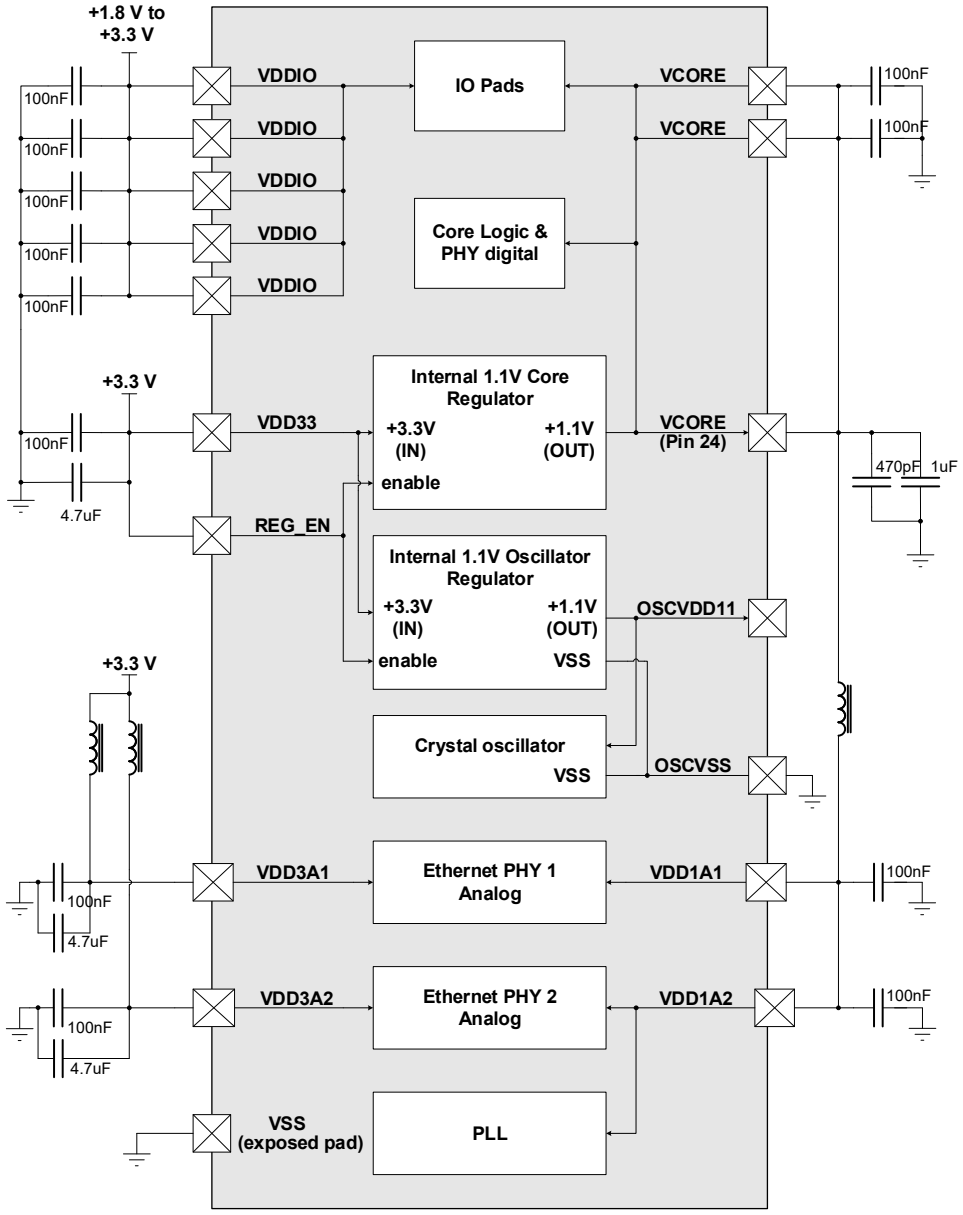
## 4.2. Recommended DC characteristics

**Table 4-2. DC operating conditions**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD1Ax}$ | Analog 1.1V power for Ethernet PHY | — | 1.05 | 1.1 | 1.15 | V |
| $V_{OSCVDD11}$ | Internal 1.1V oscillator supply voltage | — | 1.0 | 1.1 | 1.2 | V |
| $V_{CORE}$ | Digital core supply voltage | — | 1.05 | 1.1 | 1.15 | V |
| $V_{DD3Ax}$ | Analog 3.3V power for Ethernet PHY | — | 3.0 | 3.3 | 3.6 | V |
| $V_{DD33}$ | Supply voltage for the internal regulator | — | 3.0 | 3.3 | 3.6 | V |
| $V_{DDIO}$ | IO supply voltage | — | 1.8 | 3.3 | 3.6 | V |

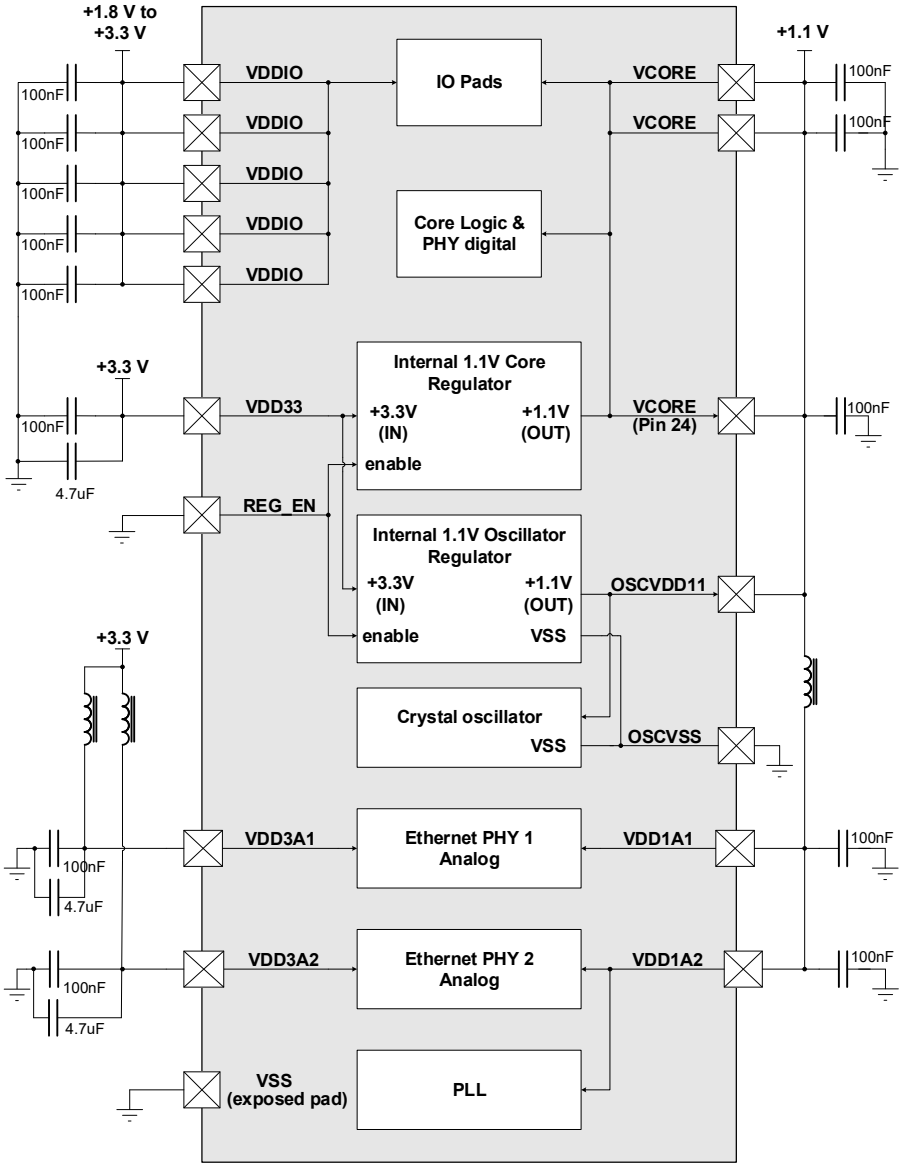
(1) Value guaranteed by characterization, not 100% tested in production.

**Figure 4-1. Recommended power connections(regulators enabled)(1)**




(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

**Figure 4-2. Recommended power connections(regulators disabled)(1)**




(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

**Table 4-3. Power supply on and off timing values(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PON}$ | Power supply turn on time | — | — | — | 50 | ms |
| $t_{POFF}$ | Power supply turn off time | — | — | — | 500 | ms |

(1) Value guaranteed by design, not 100% tested in production.

**Figure 4-3. Power supply on and off timing (internal regulators)**

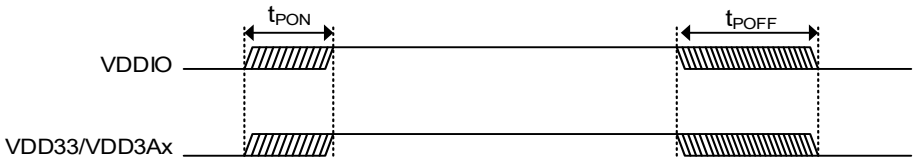


**Figure 4-4. Power supply on and off timing (external regulators)**

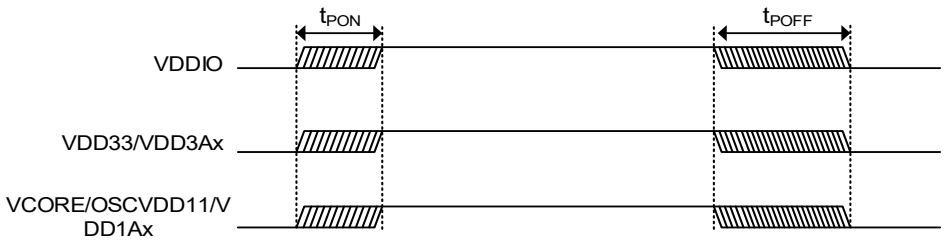


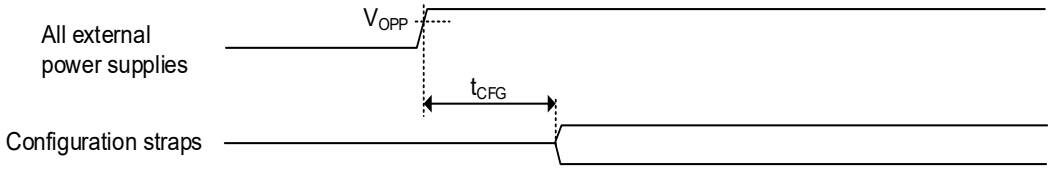

**Table 4-4. Power-on configuration strap latching timing values(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CFG}$ | Configuration strap valid time | — | — | — | 15 | ms |

(1) Value guaranteed by design, not 100% tested in production.

(2) Configuration straps must only be pulled high or low. Configuration straps must not be driven as inputs.

**Figure 4-5. Power-on configuration strap latching timing diagram**




## 4.3. EMC characteristics

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

**Table 4-5. Component level ESD and latch-up characteristics (1)**

| Symbol | Description | Conditions | Package | Max | Unit | Level |
|---|---|---|---|---|---|---|
| $V_{HBM}$ | Human body model electrostatic discharge voltage (Any pin combination) | $T_J$ = 25 °C; JS-001-2017 | QFN64 | TBD | V | TBD |
| $V_{CDM}$ | Charge device model electrostatic discharge voltage (All pins) | $T_J$ = 25 °C; JS-002-2018 | QFN64 | TBD | V | TBD |
| LU | I-test | $T_A$ = 125 °C, JESD78F | QFN64 | TBD | mA | TBD |
| | $V_{supply}$ over voltage | | | TBD | V | |

(1) Value guaranteed by characterization, not 100% tested in production.

## 4.4. Power consumption

**Table 4-6. Power consumption characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Regulators enabled | | | | | | |
| **3.3V Device Current(2)** | Supply current (MOD0) | Disconnect to the Ethernet cable | — | 36 | — | mA |
| | | 100BASE-TX with traffic | — | 86 | — | |
| | | 100BASE-TX with idle | — | 85 | — | |
| | Supply current (MOD1) | 100BASE-TX with idle | — | 82 | — | |
| | Supply current (MOD2) | 100BASE-TX with idle | — | 80 | — | |
| | Supply current (MOD3) | All clocks off | — | 17 | — | |
| Regulators disabled | | | | | | |
| **3.3V Device Current(2)** | Supply current (MOD0) | Disconnect to the Ethernet cable | — | 24 | — | mA |
| | | 100BASE-TX with traffic | — | 42 | — | |
| | | 100BASE-TX with idle | — | 42 | — | |
| | Supply current (MOD1) | 100BASE-TX with idle | — | 40 | — | |
| | Supply current (MOD2) | 100BASE-TX with idle | — | 40 | — | |
| | Supply current (MOD3) | All clocks off | — | 16 | — | |
| **1.1V Device Current(3)** | Supply current (MOD0) | Disconnect to the Ethernet cable | — | 8 | — | |
| | | 100BASE-TX with traffic | — | 44 | — | |
| | | 100BASE-TX with idle | — | 44 | — | |
| | Supply current (MOD1) | 100BASE-TX with idle | — | 42 | — | |
| | Supply current (MOD2) | 100BASE-TX with idle | — | 40 | — | |
| | Supply current (MOD3) | All clocks off | — | 0 | — | |

(1) Value guaranteed by sample, not 100% tested in production.

(2) Including the following pins，VDD33,VDD3Ax,VDDIO.

(3) Including the following pins，OSCVDD11,VDD1Ax,VCORE.

## 4.5. I/O characteristics

**Table 4-7. Non-variable I/O DC electrical characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Analog input buffer(RXPA/RXNA/RXPB/RXNB)** | | | | | | |
| $V_{IN_DIFF}$ | Differential input level | — | — | 2 | — | V |
| $V_{CM}$ | Common mode voltage | | — | 1.65 | — | |
| $C_{IN}$ | Input capacitance | | — | 3.27 | — | pF |
| **Crystal oscillator input buffer(OSCI input)** | | | | | | |
| $V_{ILI}$ | Low input level | — | -0.3 | — | 0.35 | V |
| $V_{IHI}$ | High input level | | OSCVDD11-0.35 | — | 3.6 | |
| **Low voltage PECL input buffer** | | | | | | |
| $V_{IL}$ | Low input level | — | -0.3 | — | 0.8 | V |
| $V_{IH}$ | High input level | | 2 | — | 3.93 | |
| **Low voltage PECL output buffer** | | | | | | |
| $V_{OL}$ | Low input level | — | — | — | 0.4 | V |
| $V_{OH}$ | High input level | | 2.4 | — | — | |
| $C_{LOAD}$ | Load capacitance | | — | 1.1 | — | pF |

(1) Value guaranteed by design, not 100% tested in production.

**Table 4-8. Variable I/O DC electrical characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 1.8V | 3.3V | | |
| **Schmitt-triggered input buffer** | | | | | | | |
| $V_{ILI}$ | Low input level | — | -0.3 | — | — | — | V |
| $V_{IHI}$ | High input level | | — | — | — | 3.6 | |
| $V_{ILT}$ | Negative-going threshold | | 0.65 | 0.8 | 1.47 | 1.75 | |
| $V_{IHT}$ | Positive-going threshold | | 0.81 | 0.96 | 1.61 | 1.88 | |
| $V_{HYS}$ | Schmitt trigger hysteresis ($V_{IHT}$ - $V_{ILT}$) | | 120 | 150 | 145 | 210 | mV |
| $I_{IH}$ | Input leakage ($V_{IN}$ = VSS or VDDIO) | | -10 | — | — | 10 | uA |
| $C_{IN}$ | Input capacitance | | — | 5 | 5 | 7 | pF |
| $R_{PU}$ | Weak pull-up equivalent resistor ($V_{IN}$ = VSS) | | 57.6 | 68 | 68 | 80 | kΩ |
| $I_{PU}$ | Pull-up current ($V_{IN}$ = VSS) | | 62.5 | 26 | 48 | 20.25 | uA |
| $R_{PD}$ | Weak pull-down equivalent resistor ($V_{IN}$ = VDD33) | | 57.5 | 68 | 68 | 80.1 | kΩ |
| $I_{PD}$ | Pull-down current ($V_{IN}$ = VDD33) | | 62.6 | 26 | 48 | 20.2 | uA |
| **Variable voltage output with 8 mA sink and 8 mA source buffers** | | | | | | | |
| $V_{OL}$ | Low output level | $I_{load}$ = 8mA | — | — | — | 0.4 | V |
| $V_{OH}$ | High output level | $I_{load}$ = -8mA | VDDIO - 0.4 | — | — | — | |
| **Variable voltage open-drain output with 8 mA sink buffers** | | | | | | | |
| $V_{OL}$ | Low output level | $I_{load}$ = 8mA | — | — | — | 0.4 | V |
| **Variable voltage output with 12 mA sink and 12 mA source buffers** | | | | | | | |
| $V_{OL}$ | Low output level | $I_{load}$ = 12mA | — | — | — | 0.4 | V |
| $V_{OH}$ | High output level | $I_{load}$ = -12mA | VDDIO - 0.4 | — | — | — | |
| **Variable voltage open-drain output with 12 mA sink buffers** | | | | | | | |
| $V_{OL}$ | Low output level | $I_{load}$ = 12mA | — | — | — | 0.4 | V |
| **Variable voltage open-source output with 12 mA source buffers** | | | | | | | |
| $V_{OH}$ | High output level | $I_{load}$ = -12mA | VDDIO -0.4 | — | — | — | V |

(1) Value guaranteed by design, not 100% tested in production.

**Table 4-9. 100base-TX transceiver characteristics(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{PPH}$(2) | Peak differential output voltage high | 950 | — | 1050 | mVpk |
| $V_{PPL}$(2) | Peak differential output voltage low | -950 | — | -1050 | mVpk |
| $V_{SS}$(2) | Signal amplitude symmetry | 98 | — | 102 | % |
| $T_{RF}$(2) | Signal rise and fall time | 3 | — | 5 | ns |
| $T_{RFS}$(2) | Rise and fall symmetry | — | — | 0.5 | ns |
| $D_{CD}$ | Duty cycle distortion | — | — | 0.5 | ns |
| $V_{OS}$ | Overshoot and undershoot | — | — | 5 | % |
| — | Jitter | — | — | 1.4 | ns |

(1) Value guaranteed by characterization, not 100% tested in production.

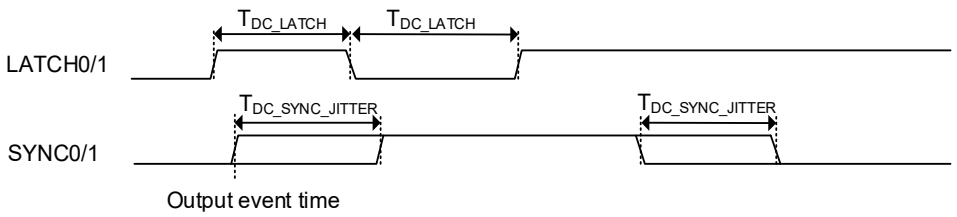
(2) Measured at line side of transformer, line replace by 100ohm(±1%) resistor.

**Table 4-10. EtherCAT SYNC/LATCH timing values(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{DC_LATCH}$ | Time between LATCH0 or LATCH1 events | — | 15 | — | — | ns |
| $t_{DC_SYNC_JITTER}$ | SYNC0 or SYNC1 output jitter | — | — | — | 15 | ns |

(1) Value guaranteed by characterization, not 100% tested in production.

**Figure 4-6. EtherCAT SYNC/LATCH timing diagram**



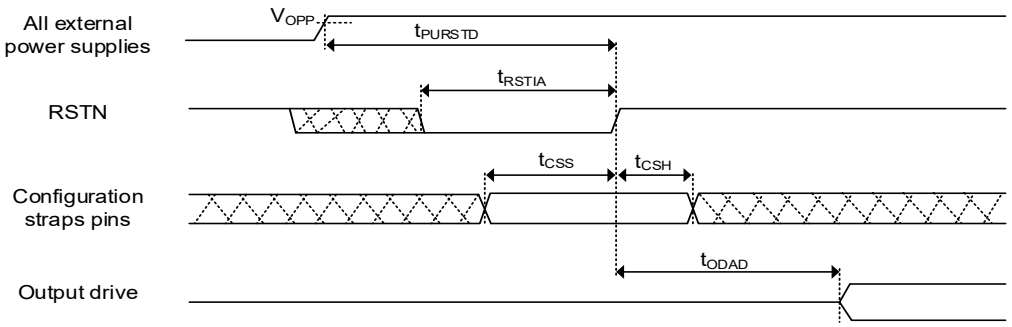

## 4.6. RSTN pin characteristics

**Table 4-11. RSTN pin configuration strap latching timing values(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PURSTD}$ | External power supplies at operational level to RSTN invalid time | — | 25 | — | — | ms |
| $t_{RSTIA}$ | RSTN input valid time | — | 200 | — | — | us |
| $T_{CSS}$ | Configuration strap pins setup time to RSTN invalid | — | 200 | — | — | ns |
| $t_{CSH}$ | Configuration strap pins hold time after RSTN invalid | — | 30 | — | — | ns |
| $t_{ODAD}$ | Output drive time after RSTN invalid | — | 3 | — | — | us |

(1) Value guaranteed by design, not 100% tested in production.

**Figure 4-7. Power-on configuration strap latching timing diagram**




## 4.7. Clock characteristics

**Table 4-12. Crystal specifications**(1)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Crystal cut | | AT, typ | | | |
| Crystal oscillation mode | | Fundamental mode | | | |
| Crystal calibration mode | | Parallel resonant mode | | | |
| $F_{FUND}$ | Frequency | — | 25.000 | — | MHZ |
| $F_{TOL}$ | 802.3 Frequency tolerance at 25°C | — | — | ±40 | ppm |
| $F_{TEMP}$ | 802.3 Frequency stability over temp | — | — | ±40 | ppm |
| $F_{AGE}$ | 802.3 Frequency deviation over time | — | ±3 ~ 5 | — | ppm |
| 802.3 total allowable PPM budget | | — | — | ±50 | ppm |
| $F_{TOL}$ | EtherCAT frequency tolerance at 25°C | — | — | ±15 | ppm |
| $F_{TEMP}$ | EtherCAT frequency stability over Temp | — | — | ±15 | ppm |
| $F_{AGE}$ | EtherCAT frequency deviation over Time | — | ±3 ~ 5 | — | ppm |
| EtherCAT total allowable PPM budget | | — | — | ±25 | ppm |
| $C_O$ | Parallel Capacitance | — | — | 7 | pF |
| $C_L$ | Recommended matching capacitance on OSCI and OSCO | — | 10 | 20 | pF |
| $R_1$ | Equivalent Series Resistance | — | — | 100 | Ω |
| Operating Temperature Range | | -40 | — | 125 | °C |
| OSCI Pin Capacitance | | — | 3 | — | pF |
| OSCO Pin Capacitance | | — | 3 | — | pF |

(1) Value guaranteed by design, not 100% tested in production.

## 4.8. Digital I/O characteristics

**Table 4-13. EtherCAT I/O timing values(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{INDATASYNCS}$ | Input data setup to SYNC0/1 rising | 10 | — | — | ns |
| $t_{INDATASYNCH}$ | Input data hold from SYNC0/1 rising | 0 | — | — | ns |
| $t_{INDATALATCHS}$ | Input data setup to LATCH_IN rising | 8 | — | — | ns |
| $t_{INDATALATCHH}$ | Input data hold from LATCH_IN rising | 4 | — | — | ns |
| $t_{LATCHIN}$ | LATCH_IN rising | 8 | — | — | ns |
| $t_{LATCHINDELAY}$ | Time between consecutive input events | 440 | — | — | ns |
| $t_{SOF}$ | SOF high time | 35 | — | — | ns |
| $t_{SOFDATAV}$ | Input data valid after SOF active, so that input data can be read in the same frame | — | — | 1.2 | us |
| $t_{SOFDATAH}$ | Input data hold after SOF active, so that input data can be read in the same frame | 1.6 | — | — | us |
| $t_{OUTDATAS}$ | Output data setup to OUTVALID rising | 65 | — | — | ns |
| $t_{OUTDATAH}$ | Output data hold from OUTVALID falling | 65 | — | — | ns |
| $t_{OUTVALID}$ | OUTVALID high time | 75 | — | — | ns |
| $t_{OUTVALIDDELAY}$ | Time between consecutive output events | 320 | — | — | ns |
| $t_{EOF}$ | EOF high time | 35 | — | 45 | ns |
| $t_{EOFDATA}$ | Output data valid after EOF | — | — | 35 | ns |
| $t_{WD_TRIG}$ | WD_TRIG high time | 35 | — | 45 | ns |
| $t_{WD_TRIGDATA}$ | Output data valid after WD_TRIG | — | — | 35 | ns |
| $t_{SYNCDATA}$ | Output data valid after SYNC0/1 | — | — | 25 | ns |
| $t_{OE_EXTDATA}$ | OE_EXT to data low | 0 | — | 15 | ns |
| $t_{BIDIRDELAY}$ | Time between consecutive input or output events | 440 | — | — | ns |

(1) Value guaranteed by design, not 100% tested in production.

**Figure 4-8. EtherCAT digital I/O input timing diagram**

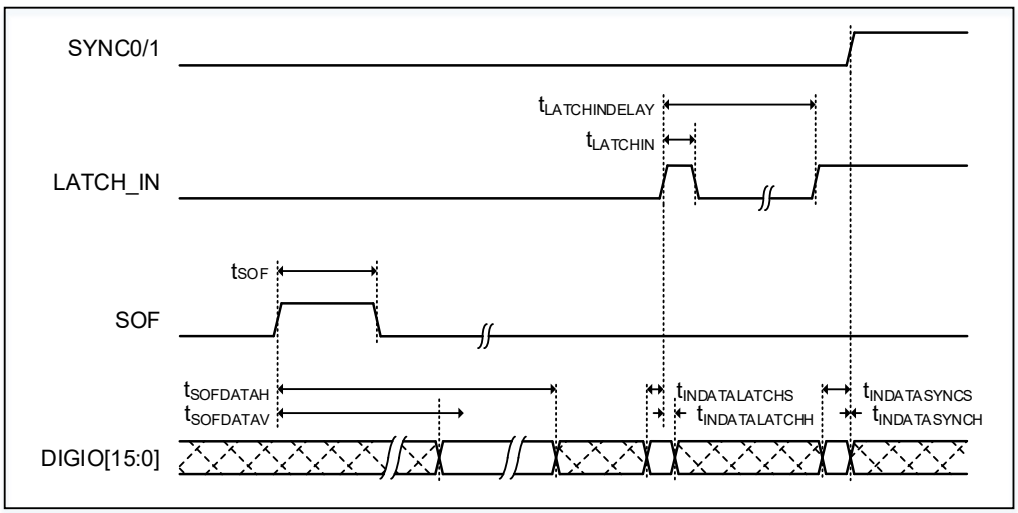


**Figure 4-9. EtherCAT digital I/O output timing diagram**

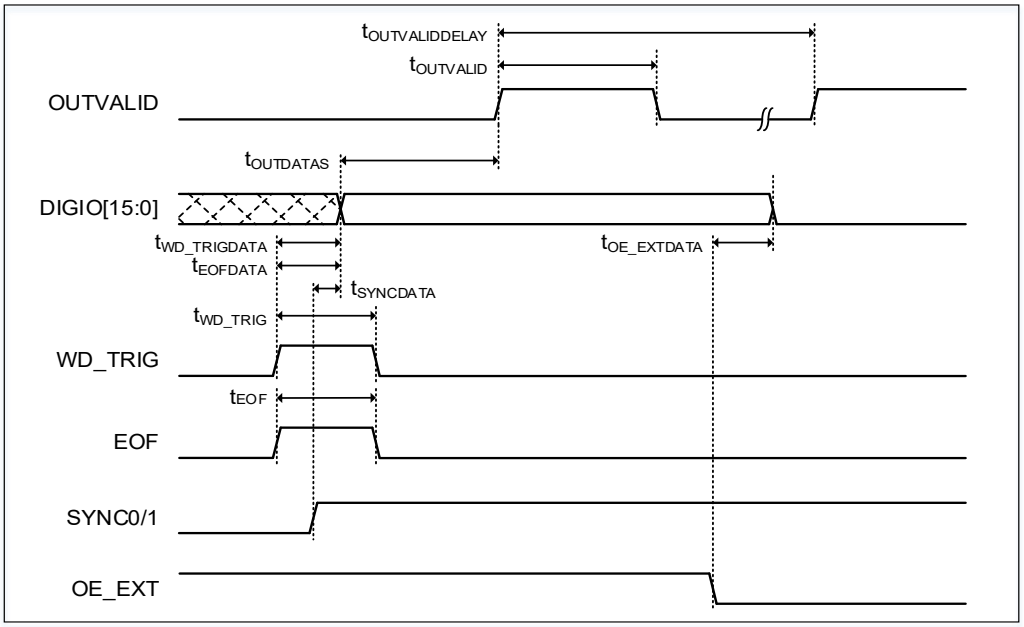
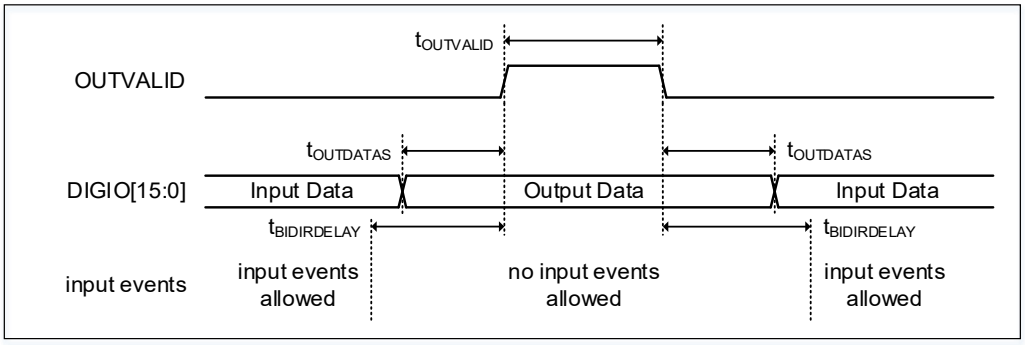



**Figure 4-10. EtherCAT digital I/O bi-directional timing diagram**



## 4.9. I2C characteristics

**Table 4-14. I2C controller timing values(1)**

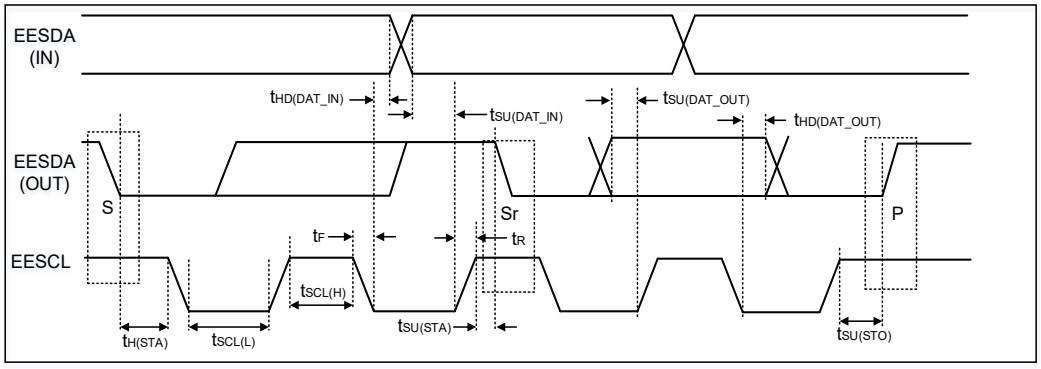
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | EESCL clock frequency | — | — | 148.8 | — | KHz |
| $t_{SCL(H)}$ | EESCL clock high time | — | 3.0 | — | — | us |
| $t_{SCL(L)}$ | EESCL clock low time | — | 3.0 | — | — | us |
| $t_{r(SDA/SCL)}$ | EESDA and EESCL rise time | — | — | — | 300 | ns |
| $t_{f(SDA/SCL)}$ | EESDA and EESCL fall time | — | — | — | 300 | ns |
| $t_{SU(STA)}$(2) | Setup time (provided to target) of EESCL high before EESDA output falling for repeated start condition | — | 1000 | — | — | ns |
| $t_{HD(STA)}$(2) | Hold time (provided to target) of EESCL after EESDA output falling for start or repeated start condition | — | 1000 | — | — | ns |
| $t_{SU(DAT_IN)}$(3) | Setup time (from target) EESDA input before EESCL rising | — | 200 | — | — | ns |
| $t_{HD(DAT_IN)}$ | Hold time (from target) of EESDA input after EESCL falling | — | 0 | — | — | ns |
| $t_{SU(DAT_OUT)}$(3) | Setup time (provided to target) EESDA output before EESCL rising | — | 400 | — | — | ns |
| $t_{HD(DAT_OUT)}$(3) | Hold time (provided to target) of EESDA output after EESCL falling | — | 400 | — | — | ns |
| $t_{SU(STO)}$(2) | Setup time (provided to target) of EESCL high before EESDA output rising for stop condition | — | 1000 | — | — | ns |

(1) Guaranteed by design, not 100% tested in production.

(2) These values provide 400ns of margin compared to the I2C fast-mode specification.

(3) These values provide a margin of approximately 2100ns compared to the I2C fast-mode specification.

**Figure 4-11. I2C bus timing diagram**



## 4.10. SPI /QSPI/OSPI slave characteristics

**Table 4-15. SPI/QSPI/OSPI slave timing values (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | — | — | — | 100 | MHz |
| $t_{HIGH}$ | SCK high time | — | — | 5 | — | ns |
| $t_{LOW}$ | SCK low time | — | — | 5 | — | ns |
| $t_{SCSS}$ | SCS setup time to SCK | — | 5 | — | — | ns |
| $t_{SCSH}$ | SCS hold time from SCK | — | 5 | — | — | ns |
| $t_{SCSHL}$ | SCS inactive time | — | — | 50 | — | ns |
| $t_{SU}$ | Data input setup time to SCK | — | 2 | — | — | ns |
| $t_{HD}$ | Data input hold time from SCK | — | 3 | — | — | ns |
| $t_{ON}$ | Data output turn on time from SCK | — | 0 | — | — | ns |
| $t_V$ | Data output valid time from SCK | — | — | — | 8 | ns |
| $t_{HO}$ | Data output hold time from SCK | — | 0 | — | — | ns |
| $t_{DIS}$ | Data output disable time from SCS inactive | — | — | — | 20 | ns |

(1) Value guaranteed by design, not 100% tested in production.

**Figure 4-12. SPI/QSPI/OSPI input timing diagram**

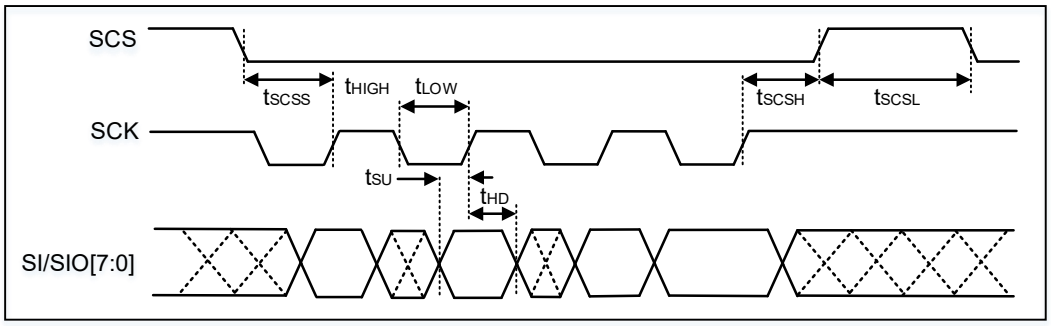
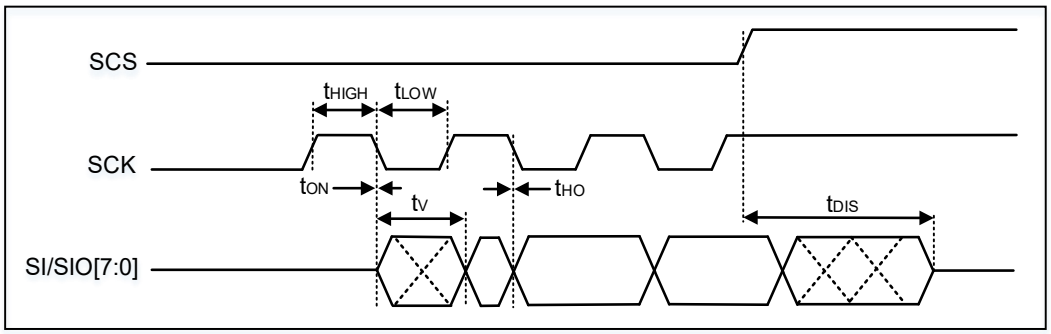



**Figure 4-13. SPI/QSPI/OSPI output timing diagram**



## 4.11. EXMC characteristics

**Table 4-16. Synchronous multiplexed read timings(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{CLK}$ | EXMC clock frequency | — | — | 80 | MHz |
| $t_{su(NEL_CLKH)}$ | EXMC_NE low setup time to EXMC_CLK high | 3.25 | — | — | ns |
| $t_{su(NLL_CLKH)}$ | EXMC_NL low setup time to EXMC_CLK high | 4 | — | — | ns |
| $t_{su(NOEL_CLKH)}$ | EXMC_NOE low setup time to EXMC_CLK high | 3.75 | — | — | ns |
| $t_{su(ADV_CLKH)}$ | EXMC_ADV setup time to EXMC_CLK high | 3 | — | — | ns |
| $t_{d(CLKH_DV)}$ | EXMC_CLK high valid time to EXMC_DV | — | — | 9.5 | ns |
| $t_{d(CLKH_DIV)}$ | EXMC_CLK high valid time to EXMC_DIV | 0 | — | — | ns |
| $t_{d(CLKH_NWAITL)}$ | EXMC_CLK high valid time to EXMC_NWAIT low | — | — | 9 | ns |
| $t_{d(CLKH_NWAITH)}$ | EXMC_CLK high valid time to EXMC_NWAIT high | 2.5 | — | — | ns |

(1) Value guaranteed by design, not 100% tested in production.

**Table 4-17. Synchronous multiplexed write timings(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{CLK}$ | EXMC clock frequency | — | — | 80 | MHz |
| $t_{su(NLL_CLKH)}$ | EXMC_NL low setup time to EXMC_CLK high | 3.25 | — | — | ns |
| $t_{su(NWEL_CLKH)}$ | EXMC_NWE low setup time to EXMC_CLK high | 4 | — | — | ns |
| $t_{su(ADV_CLKH)}$ | EXMC_ADV setup time to EXMC_CLK high | 3.75 | — | — | ns |
| $t_{su(DV_CLKH)}$ | EXMC_DV setup time to EXMC_CLK high | 3 | — | — | ns |
| $t_{d(DV_CLKH)}$ | EXMC_DV high valid time to EXMC_CLK | 3.25 | — | — | ns |
| $t_{d(CLKH_NWAITL)}$ | EXMC_CLK high valid time to EXMC_NWAIT low | — | — | 9 | ns |
| $t_{d(CLKH_NWAITH)}$ | EXMC_CLK high valid time to EXMC_NWAIT high | 2.5 | — | — | ns |

(1) Value guaranteed by design, not 100% tested in production.

## 4.12. Ethernet PHY characteristics

**Table 4-18. MII TX timing values(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CLKP}$ | MII_CLK25 period | 40 | — | — | ns |
| $t_{CLKH}$ | MII_CLK25 high time | 18 | — | 22 | ns |
| $t_{CLKL}$ | MII_CLK25 low time | 18 | — | 22 | ns |
| $t_{VAL}$ | MII_TXD[3:0], MII_TXEN output valid from rising edge of MII_CLK25 | — | — | 10 | ns |
| $t_{HOLD}$ | MII_TXD[3:0], MII_TXEN output hold from rising edge of MII_CLK25 | 0 | — | — | ns |

(1) Value guaranteed by design, not 100% tested in production.

**Figure 4-14. MII TX timing diagram**

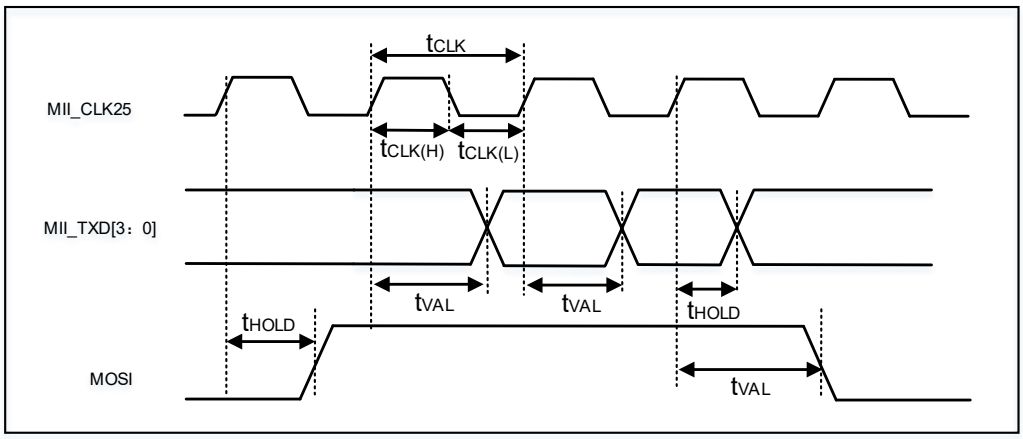



**Table 4-19. MII RX timing values(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CLKP}$ | MII_RXCLK period | 40 | — | — | ns |
| $t_{CLKH}$ | MII_RXCLK high time | 16 | — | 24 | ns |
| $t_{CLKL}$ | MII_RXCLK low time | 16 | — | 24 | ns |
| $t_{SU}$ | MII_RXD[3:0], MII_RXER, MII_RXDV setup time to rising edge of MII_RXCLK | 5 | — | — | ns |
| $t_{HOLD}$ | MII_RXD[3:0], MII_RXER, MII_RXDV hold time after rising edge of MII_RXCLK | 6 | — | — | ns |

(1) Value guaranteed by design, not 100% tested in production.

**Figure 4-15. MII RX timing diagram**

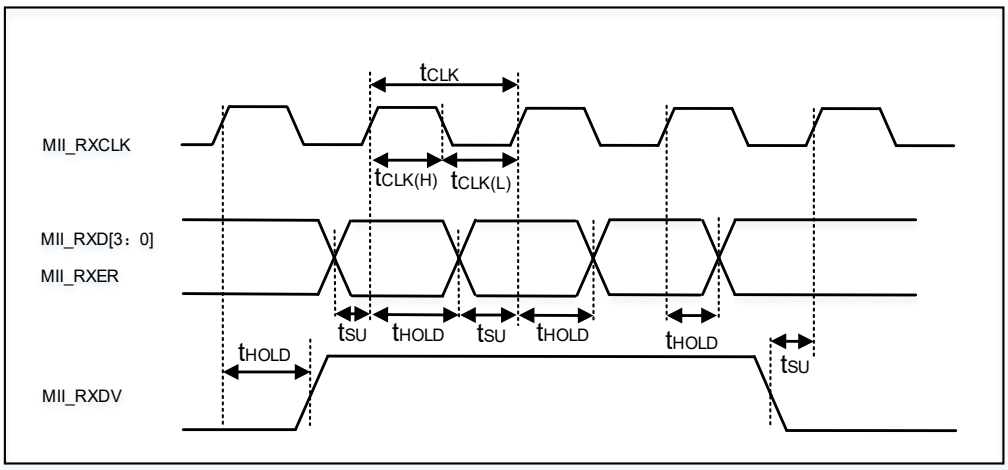
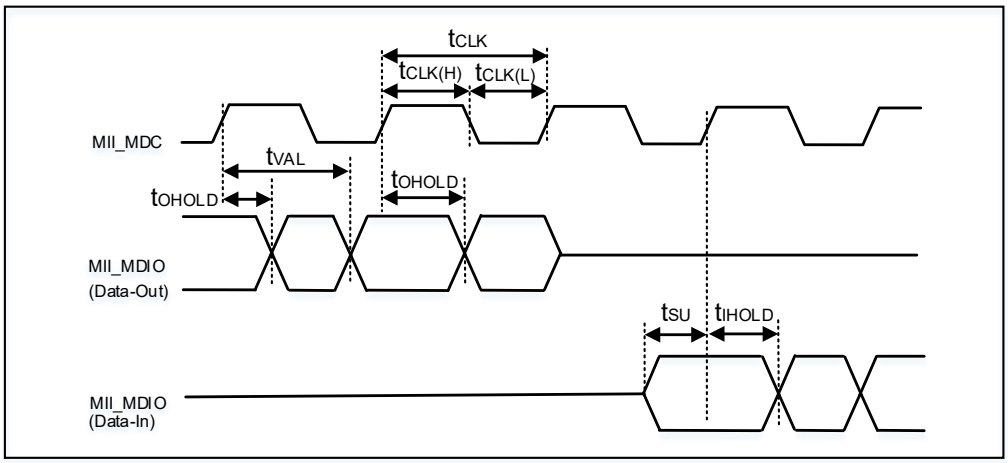


**Table 4-20. Management access timing values(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CLKP}$ | MII_MDC period | 400 | — | — | ns |
| $t_{CLKH}$ | MII_MDC high time | 180 | — | — | ns |
| $t_{CLKL}$ | MII_MDC low time | 180 | — | — | ns |
| $t_{VAL}$ | MII_MDIO output valid from rising edge of MII_MDC | — | — | 250 | ns |
| $t_{OHOLD}$ | MII_MDIO output hold from rising edge of MII_MDC | 150 | — | — | ns |
| $t_{SU}$ | MII_MDIO input setup time to rising edge of MII_MDC | 70 | — | — | ns |
| $t_{IHOLD}$ | MII_MDIO input hold time after rising edge of MII_MDC | 0 | — | — | ns |

(1) Value guaranteed by design, not 100% tested in production.

**Figure 4-16. Management access timing diagram**



# 5. Package information

## 5.1. QFN64 package outline dimensions

**Figure 5-1. QFN64 package outline**

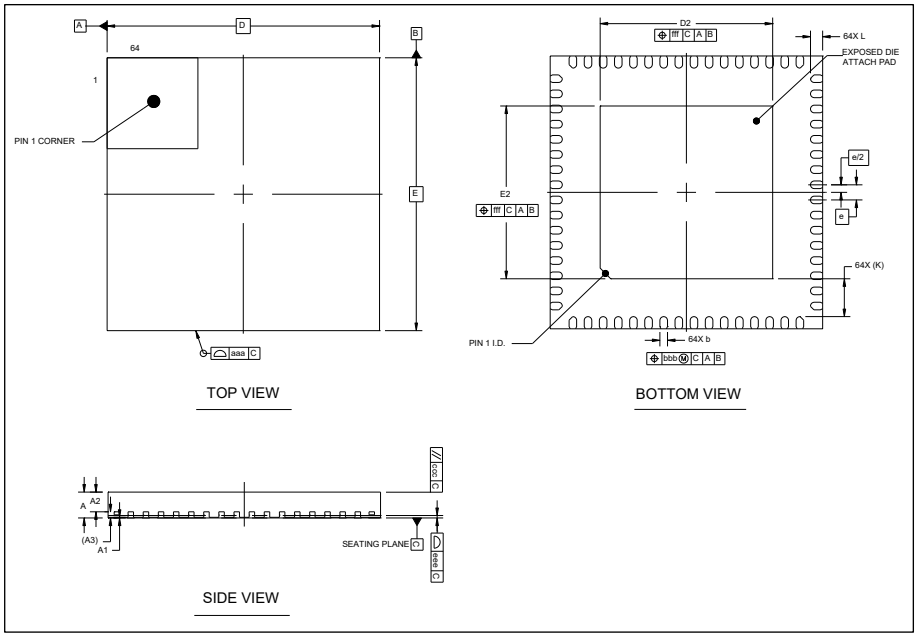
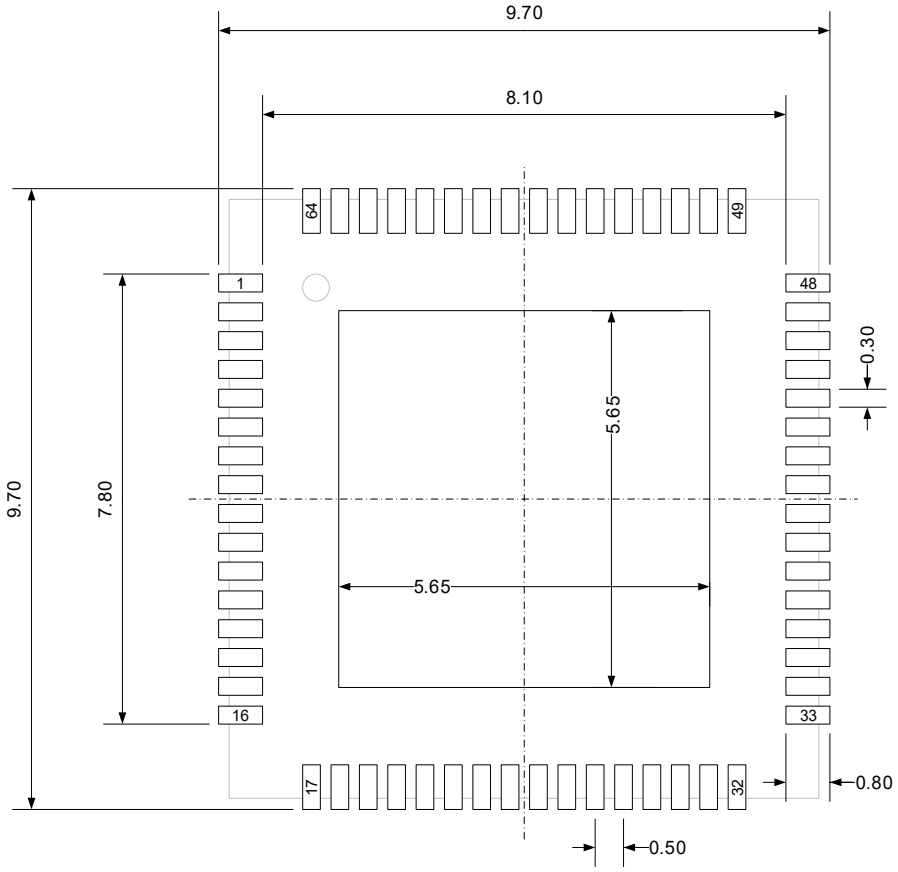



**Table 5-1. QFN64 package dimensions**

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0 | 0.02 | 0.05 |
| A2 | — | 0.65 | — |
| A3 | — | 0.203 | — |
| b | 0.20 | 0.25 | 0.30 |
| D | — | 9.00 | — |
| D2 | 5.60 | 5.70 | 5.80 |
| E | — | 9.00 | — |
| E2 | 5.60 | 5.70 | 5.80 |
| e | — | 0.50 | — |
| K | — | 1.25 | — |
| L | 0.30 | 0.40 | 0.50 |
| aaa | — | 0.10 | — |
| bbb | — | 0.10 | — |
| ccc | — | 0.10 | — |
| eee | — | 0.08 | — |
| fff | — | 0.10 | — |

(Original dimensions are in millimeters)

**Figure 5-2. QFN64 recommended footprint**




(Original dimensions are in millimeters)

## 5.2. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

$\theta_{JA}$: Thermal resistance, junction-to-ambient.

$\theta_{JB}$: Thermal resistance, junction-to-board.

$\theta_{JC}$: Thermal resistance, junction-to-case.

$\Psi_{JB}$: Thermal characterization parameter, junction-to-board.

$\Psi_{JT}$: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, $T_J$ = Junction temperature.

$T_A$ = Ambient temperature

$T_B$ = Board temperature

$T_C$ = Case temperature which is monitoring on package surface

$P_D$ = Total power dissipation

$\theta_{JA}$ represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower $\theta_{JA}$ can be considerate as better overall thermal performance. $\theta_{JA}$ is generally used to estimate junction temperature.

$\theta_{JB}$ is used to measure the heat flow resistance between the chip surface and the PCB board.

$\theta_{JC}$ represents the thermal resistance between the chip surface and the package top case. $\theta_{JC}$ is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

**Table 5-2. Package thermal characteristics(1)**

| Symbol | Condition | Package | Value | Unit |
|---|---|---|---|---|
| $\theta_{JA}$ | Natural convection, 2S2P PCB | QFN64 | 23.7 | °C/W |
| $\theta_{JB}$ | Cold plate, 2S2P PCB | QFN64 | 10 | °C/W |
| $\theta_{JC}$ | Cold plate, 2S2P PCB | QFN64 | 18 | °C/W |
| $\Psi_{JB}$ | Natural convection, 2S2P PCB | QFN64 | 10 | °C/W |
| $\Psi_{JT}$ | Natural convection, 2S2P PCB | QFN64 | 0.8 | °C/W |

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

# 6. Ordering information

**Table 6-1. Part ordering code for GDSCN832xx devices**

| Ordering code | Package | Package type | Temperature operating range |
|---|---|---|---|
| GDSCN832R2U6 | QFN64 | Green | Industrial<br>-40 °C to +85 °C |
| GDSCN832R2U7 | QFN64 | Green | Industrial<br>-40 °C to +105 °C |

# 7. Revision history

**Table 7-1. Revision history**

| Revision No. | Description | Date |
|---|---|---|
| 1.0 | Initial Release | Nov.8, 2024 |
| 1.1 | 1. In Figure 2-1, change "master" to "main" and "slave" to "subdevice."<br>2. Delete EXMC timing diagrams 4-14,4-15.<br>3. Add descriptions for Model GDSCN832R2U7 | May.15.2025 |

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