GigaDevice Semiconductor Inc.

GD32H75Exx
Arm® Cortex®-M7 32-bit MCU

Datasheet

Revision 1.2

(Apr. 2025)

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1. General description

The GD32H75Exx device belongs to the high performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M7 core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Arm® Cortex®-M7 processor is a highly efficient high-performance, embedded processor that features low interrupt latency, low-cost debug, and has backwards compatibility with existing Cortex-M profile processors. The processor has an in-order super-scalar pipeline that means many instructions can be dual-issued, including load/load and load/store instruction pairs because of multiple memory interfaces. The Cortex-M7 is a high-performance processor, which features a 6-stage superscalar pipeline with branch prediction and an optional FPU capable of single-precision and optionally double-precision operations. The instruction and data buses have been enlarged to 64-bit wide over the previous 32-bit buses. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32H75Exx device incorporates the Arm® Cortex®-M7 32-bit processor core operating at 600 MHz frequency with Flash security protection to prevent illegal code/data access. It provides up to 3840 KB on-chip Flash memory, 512KB AXI SRAM and 512KB RAM shared (ITCM/DTCM/AXI) memory. An extensive range of enhanced I/Os and peripherals connected to four APB buses. The devices offer up to two 14-bit 4 MSPS ADCs, a 12-bit 5.3 MSPS ADC, a 12-bit DAC, up to ten general 16-bit timers, two 16-bit PWM advanced timers, four 32-bit general timers, two 32-bit basic timers, and two 64-bit basic timers, as well as standard and advanced communication interfaces: up to six SPIs, one OSPI, four I2Cs, four USARTs and four UARTs, four I2Ss, three CAN-FDs one USBFS and one USBHS. Additional peripherals as EXMC interface, Filter arithmetic accelerator (FAC) and high performance digital filter module (HPDF) are included. The GD32H75Exx device also integrates the EtherCAT subdevice controller (ESC).

The device operates from a 1.71V to 3.6V power supply and available in –40 to +85 °C temperature range for grade 6 devices, -40 to +105 °C temperature range for grade 7 devices. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32H75Exx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as inverters, stepper drives, IO modules, factory communication modules, servo drive control and so on.

2. Device overview

2.1. Device information

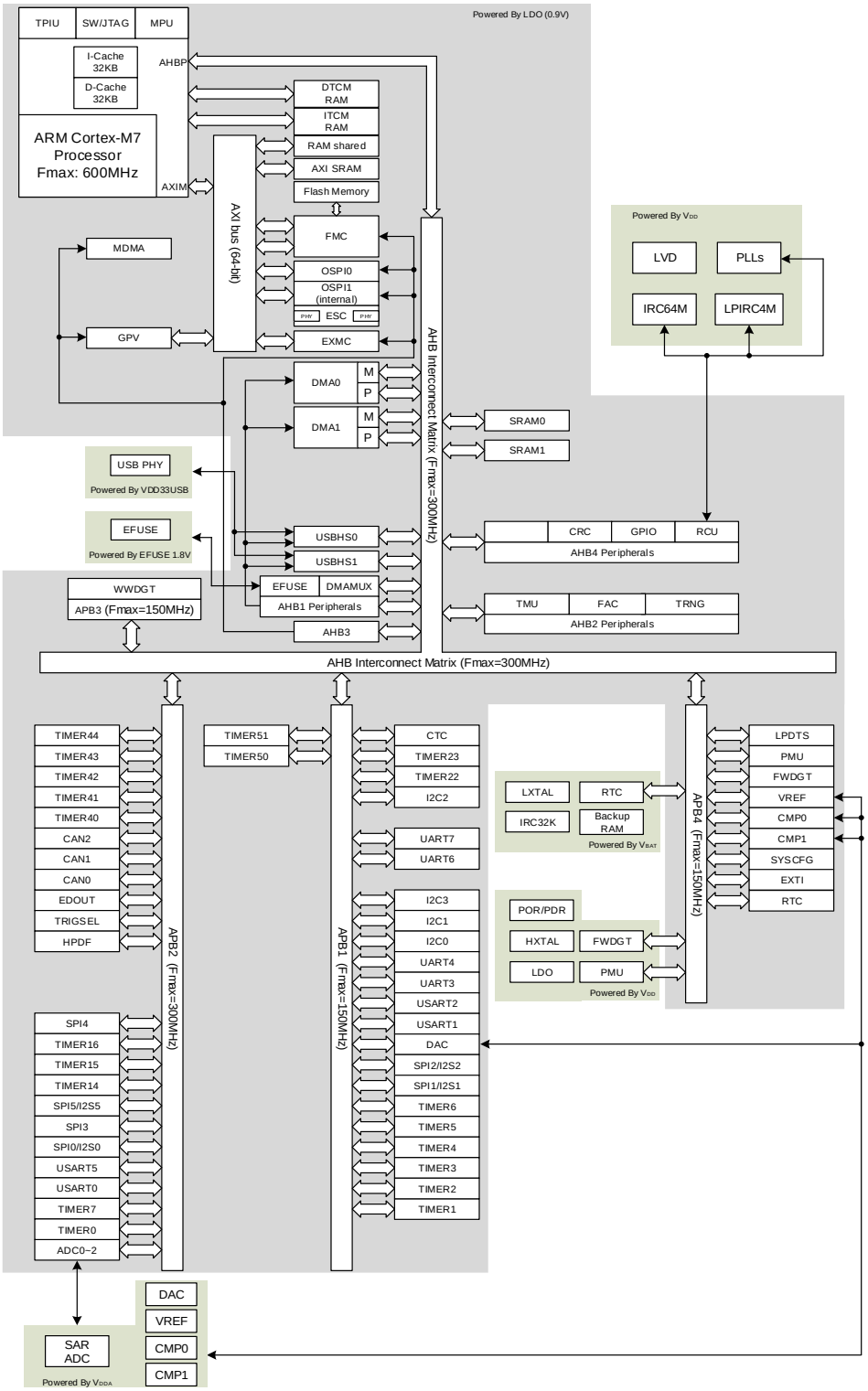
Table 2-1. GD32H75Exx devices features and peripheral list

Part Number		GD32H75EYM
FLASH (KB)		3840
SRAM (KB)		1024
Timers	General timer (16-bit)	10 (2-3,14-16,40-44)
	General timer (32-bit)	4 (1,4,22,23)
	Advanced timer(16-bit)	2 (0,7)
	Basic timer (32-bit)	2 (5,6)
	Basic timer (64-bit)	2 (50,51)
	SysTick	1
	Watchdog	2
	RTC	1
Connectivity	USART	4
	UART	4
	I2C	4
	SPI/I2S	6/4 (0-5)/(0-2,5)
	OSPI	1
	CAN	3xFD
	USBFS	1
	USBHS	1
	ESC	1
	Ethernet PHY	2
HPDF		1
EXMC		1
FAC		1

Part Number		GD32H75EYM
EDOUT		1
TMU		1
14bit ADC	Units	2
	Channels	22
12bit ADC	Units	1
	Channels	15
DAC	Units	1
CMP		2
GPIO		116
Package		BGA240

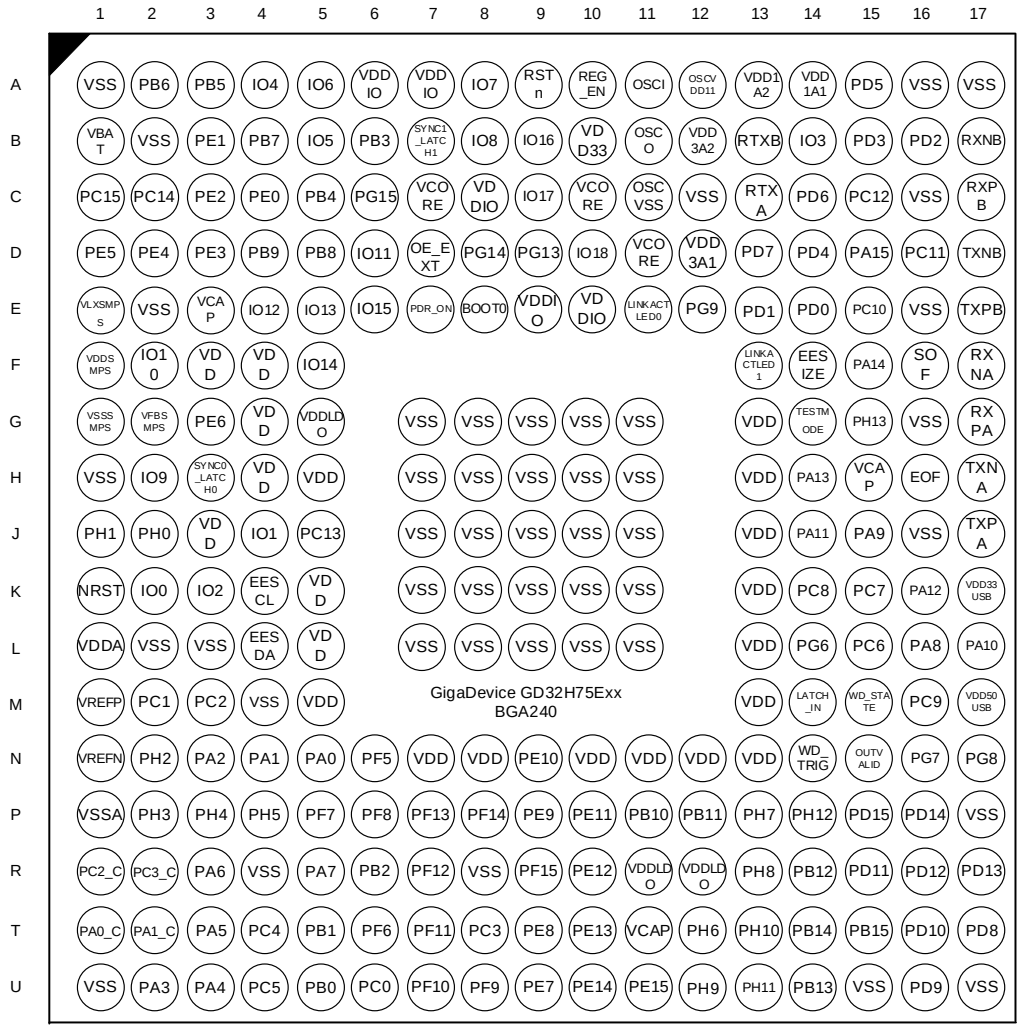
2.2. Block diagram

Figure 2-1. GD32H75Exx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32H75Exx BGA240 pinouts



2.4. Memory map

Table 2-2. Memory map of GD32H75Exx devices

Pre-defined Regions	Bus	Address	Peripherals
External RAM		0xD000 0000 – 0xDFFF FFFF	EXMC – SDRAM device 1
		0xC000 0000 – 0xCFFF FFFF	EXMC – SDRAM device 0 (EXMC Bank 0 Region 0-3)
		0xA000 1000 – 0xBFFF FFFF	Reserved
		0xA000 0000 – 0xA000 0FFF	Reserved
		0x9000 0000 – 0x9FFF FFFF	OSPI0

Pre-defined Regions	Bus	Address	Peripherals
		0x8000 0000 – 0x8FFF FFFF	EXMC – NAND
		0x7000 0000 – 0x7FFF FFFF	OSPI1
		0x6000 0000 – 0x6FFF FFFF	EXMC – NOR/PSRAM/SRAM
Peripheral	AHB4	0x5802 7000 – 0x5FFF FFFF	Reserved
		0x5802 6400 – 0x5802 67FF	Reserved
		0x5802 6000 – 0x5802 63FF	Reserved
		0x5802 5000 – 0x5802 5FFF	Reserved
		0x5802 4C00 – 0x5802 4FFF	CRC
		0x5802 4800 – 0x5802 4BFF	Reserved
		0x5802 4400 – 0x5802 47FF	RCU
		0x5802 2C00 – 0x5802 43FF	Reserved
		0x5802 2800 – 0x5802 2BFF	Reserved
		0x5802 2400 – 0x5802 27FF	Reserved
		0x5802 2000 – 0x5802 23FF	Reserved
		0x5802 1C00 – 0x5802 1FFF	GPIOH
		0x5802 1800 – 0x5802 1BFF	GPIOG
		0x5802 1400 – 0x5802 17FF	GPIOF
		0x5802 1000 – 0x5802 13FF	GPIOE
		0x5802 0C00 – 0x5802 0FFF	GPIOD
		0x5802 0800 – 0x5802 0BFF	GPIOC
		0x5802 0400 – 0x5802 07FF	GPIOB
		0x5802 0000 – 0x5802 03FF	GPIOA
		0x5801 0000 – 0x5801 FFFF	Reserved
	APB4	0x5800 7400 – 0x5800 FFFF	Reserved
		0x5800 7000 – 0x5800 73FF	Reserved
		0x5800 6C00 – 0x5800 6FFF	Reserved
		0x5800 6800 – 0x5800 6BFF	LPDTS
		0x5800 5800 – 0x5800 67FF	PMU
		0x5800 5400 – 0x5800 57FF	Reserved
		0x5800 4C00 – 0x5800 53FF	Reserved
		0x5800 4800 – 0x5800 4BFF	FWDGT
		0x5800 4000 – 0x5800 43FF	RTC
		0x5800 3C00 – 0x5800 3FFF	VREF
		0x5800 3800 – 0x5800 3BFF	CMP0 – CMP1
		0x5800 3400 – 0x5800 37FF	Reserved
		0x5800 3000 – 0x5800 33FF	Reserved
		0x5800 2C00 – 0x5800 2FFF	Reserved
		0x5800 2800 – 0x5800 2BFF	Reserved
		0x5800 2400 – 0x5800 27FF	Reserved
		0x5800 2000 – 0x5800 23FF	Reserved
		0x5800 1C00 – 0x5800 1FFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x5800 1400 – 0x5800 17FF	Reserved
		0x5800 0800 – 0x5800 13FF	Reserved
		0x5800 0400 – 0x5800 07FF	SYSCFG
		0x5800 0000 – 0x5800 03FF	EXTI
	AHB3	0x5200 C000 – 0x57FF FFFF	Reserved
		0x5200 BC00 – 0x5200 BFFF	Reserved
		0x5200 B800 – 0x5200 BBFF	Reserved
		0x5200 B400 – 0x5200 B7FF	OSPIM
		0x5200 B000 – 0x5200 B3FF	Reserved
		0x5200 A000 – 0x5200 AFFF	OSPI1(internal)
		0x5200 9400 – 0x5200 9FFF	Reserved
		0x5200 9000 – 0x5200 93FF	RAMECCMU Region 0
		0x5200 8000 – 0x5200 8FFF	Reserved
		0x5200 7000 – 0x5200 7FFF	Reserved
		0x5200 6000 – 0x5200 6FFF	Reserved
		0x5200 5000 – 0x5200 5FFF	OSPI0
		0x5200 4000 – 0x5200 4FFF	EXMC
		0x5200 3400 – 0x5200 3FFF	Reserved
		0x5200 3000 – 0x5200 33FF	Reserved
		0x5200 2000 – 0x5200 2FFF	Flash memory interface
		0x5200 1000 – 0x5200 1FFF	Reserved
		0x5200 0000 – 0x5200 0FFF	MDMA
		0x5110 0000 – 0x51FF FFFF	Reserved
		0x5100 0000 – 0x510F FFFF	AXI interconnect matrix
	APB3	0x5006 1000 – 0x50FF FFFF	Reserved
		0x5006 0C00 – 0x5006 0FFF	Reserved
		0x5006 0800 – 0x5006 0BFF	Reserved
		0x5006 0400 – 0x5006 07FF	Reserved
		0x5006 0000 – 0x5006 03FF	Reserved
		0x5005 0400 – 0x5005 FFFF	Reserved
		0x5005 0000 – 0x5005 03FF	Reserved
		0x5004 0000 – 0x5004 FFFF	Reserved
		0x5000 0000 – 0x5003 FFFF	Reserved
		0x5000 3000 – 0x5000 3FFF	WWDGT
		0x5000 2000 – 0x5000 2FFF	Reserved
		0x5000 1000 – 0x5000 1FFF	Reserved
		0x5000 0000 – 0x5000 0FFF	Reserved
	AHB2	0x4802 5000 – 0x4FFF FFFF	Reserved(AHB2)
		0x4802 4800 – 0x4802 4FFF	FAC
		0x4802 4400 – 0x4802 47FF	TMU
		0x4802 4000 – 0x4802 43FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4802 3000 – 0x4802 3FFF	RAMECCMU Region 1
		0x4802 2C00 – 0x4802 2FFF	Reserved(AHB2)
		0x4802 2800 – 0x4802 2BFF	Reserved
		0x4802 2400 – 0x4802 27FF	Reserved
		0x4802 1C00 – 0x4802 23FF	Reserved(AHB2)
		0x4802 1800 – 0x4802 1BFF	TRNG
		0x4802 1400 – 0x4802 17FF	Reserved
		0x4802 1000 – 0x4802 13FF	Reserved
		0x4802 0400 – 0x4802 0FFF	Reserved(AHB2)
		0x4802 0000 – 0x4802 03FF	Reserved
		0x4800 1800 – 0x4801 FFFF	Reserved(AHB2)
		0x4800 1400 – 0x4800 17FF	Reserved
		0x4800 1000 – 0x4800 13FF	Reserved
		0x4800 0C00 – 0x4800 0FFF	Reserved
		0x4800 0800 – 0x4800 0BFF	Reserved
		0x4800 0400 – 0x4800 07FF	Reserved
		0x4800 0000 – 0x4800 03FF	Reserved
	AHB1	0x400C 0000 – 0x47FF FFFF	Reserved(AHB1)
		0x4008 0000 – 0x400B FFFF	USBHS1
		0x4004 0000 – 0x4007 FFFF	USBHS0
		0x4003 8C00 – 0x4003 FFFF	Reserved
		0x4003 8400 – 0x4003 8BFF	Reserved
		0x4003 8000 – 0x4003 83FF	Reserved
		0x4003 3000 – 0x4003 7FFF	Reserved
		0x4003 0000 – 0x4003 2FFF	Reserved
		0x4002 C000 – 0x4002 FFFF	Reserved
		0x4002 BC00 – 0x4002 BFFF	Reserved
		0x4002 B000 – 0x4002 BBFF	
		0x4002 A000 – 0x4002 AFFF	
		0x4002 8000 – 0x4002 9FFF	Reserved
		0x4002 6800 – 0x4002 7FFF	Reserved
		0x4002 6400 – 0x4002 67FF	Reserved
		0x4002 6000 – 0x4002 63FF	Reserved
		0x4002 5000 – 0x4002 5FFF	Reserved
		0x4002 4000 – 0x4002 4FFF	Reserved
		0x4002 3C00 – 0x4002 3FFF	Reserved
		0x4002 3800 – 0x4002 3BFF	Reserved
		0x4002 3400 – 0x4002 37FF	Reserved
		0x4002 3000 – 0x4002 33FF	Reserved
		0x4002 2C00 – 0x4002 2FFF	Reserved
		0x4002 2800 – 0x4002 2BFF	EFUSE

Pre-defined Regions	Bus	Address	Peripherals
		0x4002 2400 – 0x4002 27FF	Reserved
		0x4002 2000 – 0x4002 23FF	Reserved
		0x4002 1C00 – 0x4002 1FFF	Reserved
		0x4002 1800 – 0x4002 1BFF	Reserved
		0x4002 1400 – 0x4002 17FF	Reserved
		0x4002 1000 – 0x4002 13FF	Reserved
		0x4002 0C00 – 0x4002 0FFF	Reserved
		0x4002 0800 – 0x4002 0BFF	DMAMUX
		0x4002 0400 – 0x4002 07FF	DMA1
		0x4002 0000 – 0x4002 03FF	DMA0
	APB2	0x4001 F400 – 0x4001 FFFF	Reserved
		0x4001 F000 – 0x4001 F3FF	TIMER44
		0x4001 DC00 – 0x4001 DFFF	TIMER43
		0x4001 D800 – 0x4001 DBFF	TIMER42
		0x4001 D400 – 0x4001 D7FF	TIMER41
		0x4001 D000 – 0x4001 D3FF	TIMER40
		0x4001 C000 – 0x4001 CFFF	CAN2(4KB)
		0x4001 B000 – 0x4001 BFFF	CAN1(4KB)
		0x4001 A000 – 0x4001 AFFF	CAN0(4KB)
		0x4001 8C00 – 0x4001 9FFF	Reserved
		0x4001 8800 – 0x4001 8BFF	EDOUT
		0x4001 8400 – 0x4001 87FF	TRIGSEL
		0x4001 8000 – 0x4001 83FF	Reserved(APB2)
		0x4001 7C00 – 0x4001 7FFF	Reserved
		0x4001 7800 – 0x4001 7BFF	Reserved
		0x4001 7400 – 0x4001 77FF	Reserved
		0x4001 7000 – 0x4001 73FF	HPDF
		0x4001 6C00 – 0x4001 6FFF	Reserved
		0x4001 6800 – 0x4001 6BFF	Reserved
		0x4001 6400 – 0x4001 67FF	Reserved
		0x4001 6000 – 0x4001 63FF	Reserved
		0x4001 5C00 – 0x4001 5FFF	Reserved
		0x4001 5800 – 0x4001 5BFF	Reserved
		0x4001 5400 – 0x4001 57FF	Reserved
		0x4001 5000 – 0x4001 53FF	SPI4
		0x4001 4C00 – 0x4001 4FFF	Reserved
		0x4001 4800 – 0x4001 4BFF	TIMER16
		0x4001 4400 – 0x4001 47FF	TIMER15
		0x4001 4000 – 0x4001 43FF	TIMER14
		0x4001 3C00 – 0x4001 3FFF	Reserved
		0x4001 3800 – 0x4001 3BFF	SPI5/I2S5

Pre-defined Regions	Bus	Address	Peripherals
		0x4001 3400 – 0x4001 37FF	SPI3
		0x4001 3000 – 0x4001 33FF	SPI0/I2S0
		0x4001 2C00 – 0x4001 2FFF	ADC2
		0x4001 2800 – 0x4001 2BFF	ADC1
		0x4001 2400 – 0x4001 27FF	ADC0
		0x4001 2000 – 0x4001 23FF	Reserved
		0x4001 1C00 – 0x4001 1FFF	Reserved
		0x4001 1800 – 0x4001 1BFF	Reserved
		0x4001 1400 – 0x4001 17FF	USART5
		0x4001 1000 – 0x4001 13FF	USART0
		0x4001 0C00 – 0x4001 0FFF	Reserved
		0x4001 0800 – 0x4001 0BFF	Reserved
		0x4001 0400 – 0x4001 07FF	TIMER7
		0x4001 0000 – 0x4001 03FF	TIMER0
	APB1	0x4000 F800 – 0x4000 FFFF	Reserved
		0x4000 F400 – 0x4000 F7FF	TIMER51
		0x4000 F000 – 0x4000 F3FF	TIMER50
		0x4000 EC00 – 0x4000 EFFF	Reserved
		0x4000 E800 – 0x4000 EBFF	Reserved
		0x4000 E400 – 0x4000 E7FF	TIMER23
		0x4000 E000 – 0x4000 E3FF	TIMER22
		0x4000 DC00 – 0x4000 DFFF	Reserved
		0x4000 D800 – 0x4000 DBFF	Reserved
		0x4000 D400 – 0x4000 D7FF	Reserved
		0x4000 D000 – 0x4000 D3FF	Reserved
		0x4000 CC00 – 0x4000 CFFF	Reserved
		0x4000 C800 – 0x4000 CBFF	Reserved
		0x4000 C400 – 0x4000 C7FF	Reserved
		0x4000 C000 – 0x4000 C3FF	I2C2
		0x4000 9800 – 0x4000 BFFF	Reserved
		0x4000 9400 – 0x4000 97FF	Reserved
		0x4000 8800 – 0x4000 93FF	Reserved
		0x4000 8400 – 0x4000 87FF	CTC
		0x4000 8000 – 0x4000 83FF	Reserved
		0x4000 7C00 – 0x4000 7FFF	UART7
		0x4000 7800 – 0x4000 7BFF	UART6
		0x4000 7400 – 0x4000 77FF	DAC
		0x4000 7000 – 0x4000 73FF	Reserved
		0x4000 6C00 – 0x4000 6FFF	Reserved
		0x4000 6800 – 0x4000 6BFF	Reserved
		0x4000 6400 – 0x4000 67FF	Reserved

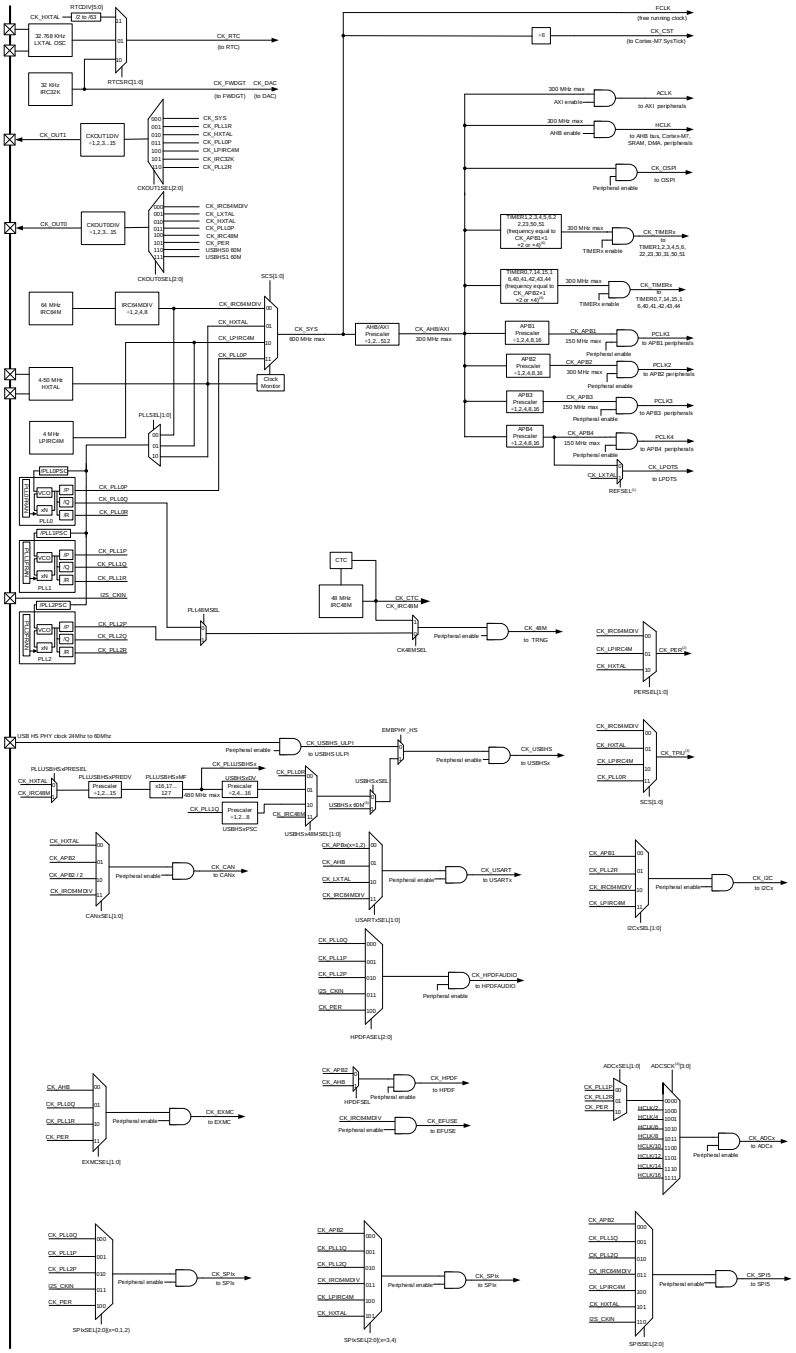
Pre-defined Regions	Bus	Address	Peripherals
		0x4000 6000 – 0x4000 63FF	Reserved
		0x4000 5C00 – 0x4000 5FFF	I2C3
		0x4000 5800 – 0x4000 5BFF	I2C1
		0x4000 5400 – 0x4000 57FF	I2C0
		0x4000 5000 – 0x4000 53FF	UART4
		0x4000 4C00 – 0x4000 4FFF	UART3
		0x4000 4800 – 0x4000 4BFF	USART2
		0x4000 4400 – 0x4000 47FF	USART1
		0x4000 4000 – 0x4000 43FF	Reserved
		0x4000 3C00 – 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 – 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 – 0x4000 37FF	Reserved
		0x4000 3000 – 0x4000 33FF	Reserved
		0x4000 2C00 – 0x4000 2FFF	Reserved
		0x4000 2800 – 0x4000 2BFF	Reserved
		0x4000 2400 – 0x4000 27FF	Reserved
		0x4000 2000 – 0x4000 23FF	Reserved
		0x4000 1C00 – 0x4000 1FFF	Reserved
		0x4000 1800 – 0x4000 1BFF	Reserved
		0x4000 1400 – 0x4000 17FF	TIMER6
		0x4000 1000 – 0x4000 13FF	TIMER5
		0x4000 0C00 – 0x4000 0FFF	TIMER4
		0x4000 0800 – 0x4000 0BFF	TIMER3
		0x4000 0400 – 0x4000 07FF	TIMER2
		0x4000 0000 – 0x4000 03FF	TIMER1
SRAM		0x3880 1000 – 0x3FFF FFFF	Reserved
		0x3880 0000 – 0x3880 0FFF	Backup SRAM
		0x3000 8000 – 0x387F FFFF	Reserved
		0x3000 4000 – 0x3000 7FFF	SRAM1(16KB)
		0x3000 0000 – 0x3000 3FFF	SRAM0(16KB)
		0x2410 0000 – 0x2FFF FFFF	Reserved
		0x2408 0000 – 0x240F FFFF	RAM(512KB) shared (ITCM/DTCM/AXI)
		0x2400 0000 – 0x2407 FFFF	AXI SRAM(512KB)
		0x2008 0000 – 0x23FF FFFF	Reserved
		0x2007 0000 – 0x2007 FFFF	DTCM RAM(from RAM shared)
		0x2006 0000 – 0x2006 FFFF	
		0x2003 0000 – 0x2005 FFFF	
		0x2002 0000 – 0x2002 FFFF	
		0x2001 C000 – 0x2001 FFFF	
		0x2001 8000 – 0x2001 BFFF	

Pre-defined Regions	Bus	Address	Peripherals
		0x2001 0000 – 0x2001 7FFF	
		0x2000 D000 – 0x2000 FFFF	
		0x2000 C000 – 0x2000 CFFF	
		0x2000 8000 – 0x2000 BFFF	
		0x2000 5000 – 0x2000 7FFF	
		0x2000 2000 – 0x2000 4FFF	
		0x2000 1000 – 0x2000 1FFF	
		0x2000 0000 – 0x2000 0FFF	
Code		0x1FFF FC10 – 0x1FFF FFFF	Reserved
		0x1FFF FC00 – 0x1FFF FC0F	Reserved
		0x1FFF F818 – 0x1FFF BFFF	Reserved
		0x1FFF F800 – 0x1FFF F817	Reserved
		0x1FFF F000 – 0x1FFF F7FF	Reserved
		0x1FFF EC00 – 0x1FFF EFFF	Reserved
		0x1FFF C010 – 0x1FFF EBFF	Reserved
		0x1FFF C000 – 0x1FFF C00F	Reserved
		0x1FFF B000 – 0x1FFF BFFF	Reserved
		0x1FFF 8000 – 0x1FFF AFFF	Reserved
		0x1FFF 7A10 – 0x1FFF 7FFF	Reserved
		0x1FFF 7800 – 0x1FFF 7A0F	Reserved
		0x1FFF 7400 – 0x1FFF 77FF	Reserved
		0x1FFF 7000 – 0x1FFF 73FF	Reserved
		0x1FFF 0000 – 0x1FFF 6FFF	Reserved
		0x1FFE C010 – 0x1FFE FFFF	Reserved
		0x1FFE C000 – 0x1FFE C00F	Reserved
		0x1FF6 0000 – 0x1FFE BFFF	Reserved
		0x1FF4 0000 – 0x1FF5 FFFF	Reserved
		0x1FF1 0000 – 0x1FF3 FFFF	Reserved
		0x1FF0 0000 – 0x1FF0 FFFF	System Memory
		0x1002 0000 – 0x1FEF FFFF	Reserved
		0x1001 0000 – 0x1001 FFFF	Reserved
		0x1000 0000 – 0x1000 FFFF	Reserved
		0x0A00 D000 – 0x0FFF FFFF	Reserved
		0x0A00 C000 – 0x0A00 CFFF	Reserved
		0x0A00 8000 – 0x0A00 BFFF	Reserved
		0x0A00 0000 – 0x0A00 7FFF	Reserved
		0x08C0 1000 – 0x09FF FFFF	Reserved
		0x08C0 0000 – 0x08C0 0FFF	Reserved
		0x0881 0000 – 0x08BF FFFF	Reserved
		0x0880 0000 – 0x0880 FFFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x0840 0000 – 0x087F FFFF	Reserved
		0x083C 0000 – 0x083F FFFF	Reserved
		0x0830 0000 – 0x083B FFFF	Flash memory
		0x0810 0000 – 0x082F FFFF	
		0x0808 0000 – 0x080F FFFF	
		0x0806 0000 – 0x0807 FFFF	
		0x0802 0000 – 0x0805 FFFF	
		0x0801 0000 – 0x0801 FFFF	
		0x0800 0000 – 0x0800 FFFF	
		0x0030 0000 – 0x07FF FFFF	Reserved
		0x0010 0000 – 0x002F FFFF	Reserved
		0x0008 0000 – 0x000F FFFF	Reserved
		0x0002 6000 – 0x0007 FFFF	ITCM RAM(from RAM shared)
		0x0002 0000 – 0x0002 5FFF	
		0x0001 0000 – 0x0001 FFFF	
		0x0000 0000 – 0x0000 FFFF	

2.5. Clock tree

Figure 2-3. GD32H75Exx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC32K: Internal 32K RC oscillator

IRC48M: Internal 48M RC oscillators

IRC64M: Internal 64M RC oscillators

2.6. Pin definitions

2.6.1. GD32H75Exx BGA240 pin definitions

Table 2 3. GD32H75Exx BGA240 pin definitions

GD32H75Exx BGA240				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
BOOT	E8	I/O		Default: BOOT
NRST	K1	-	-	Default: NRST
PA0	N5	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, TIMER14_BRKIN0, SPI5_NSS, I2S5_WS, OSPIM_P0_IO6, USART1_CTS, UART3_TX, EXMC_A19, TRIGSEL_IN0, EVENTOUT Additional: ADC0_IN16, WKUP0
PA0_C	T1	I/O		Default: PA0_C(4) Additional: ADC01_IN0
PA1	N4	I/O		Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, TIMER14_MCH0, USART1_RTS, USART1_DE, UART3_RX, OSPIM_P0_IO3, TRIGSEL_IN1, EVENTOUT Additional: ADC0_IN17
PA1_C	T2	I/O		Default: PA1_C(4) Additional: ADC01_IN1
PA2	N3	I/O		Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER14_CH0, OSPIM_P0_IO0, USART1_TX, TRIGSEL_IN7, EVENTOUT Additional: ADC01_IN14, WKUP1
PA3	U2	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER14_CH1, I2S5_MCK, OSPIM_P0_IO2, USART1_RX, USBHS0_ULPI_D0(4), OSPIM_P0_SCK, TRIGSEL_IN4, EVENTOUT Additional: ADC01_IN15
PA4	U3	I/O		Default: PA4 Alternate: TIMER4_ETI, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, USART1_CK, SPI5_NSS, I2S5_WS, EXMC_D8, EVENTOUT Additional: ADC01_IN18, DAC0_OUT0
PA5	T3	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_MCH0, SPI0_SCK, I2S0_CK, SPI5_SCK, I2S5_CK, USBHS0_ULPI_CK(4), EXMC_D9, EVENTOUT Additional: ADC01_IN19, DAC0_OUT1

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA6	R3	I/O		Default: PA6 Alternate: TIMER0_BRKIN0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, OSPIM_P0_IO3, SPI5_MISO, CMP_MUX_OUT0, EVENTOUT Additional: ADC01_IN3
PA7	R5	I/O		Default: PA7 Alternate: TIMER0_MCH0, TIMER2_CH1, TIMER7_MCH0, SPI0_MOSI, I2S0_SD, SPI5_MOSI, I2S5_SD, OSPIM_P0_IO2, EXMC_SDNWE, TRIGSEL_IN5, EVENTOUT Additional: ADC01_IN7
PA8	L16	I/O		Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, TIMER7_BRKIN2, I2C2_SCL, USART0_CK, USBHS0_SOF(4), UART6_RX, CMP_MUX_OUT1, EVENTOUT
PA9	J15	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, TRIGSEL_IN13, EVENTOUT Additional: USBHS0_VBUS(4)
PA10	L17	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, USART0_RX, TRIGSEL_IN12, USBHS0_ID(4), EVENTOUT
USBHS0_DM-PA11	J14	I/O		Default: USBHS0_DM(4) Alternate: TIMER0_CH3, SPI1_NSS, I2S1_WS, UART3_RX, USART0_CTS, CAN0_RX, TRIGSEL_IN13, EVENTOUT
USBHS0_DP-PA12	K16	I/O		Default: USBHS0_DP(4) Alternate: TIMER0_ETI, SPI1_SCK, I2S1_CK, UART3_TX, USART0_RTS, USART0_DE, CAN0_TX, TIMER0_BRKIN2, TRIGSEL_IN12, EVENTOUT
PA13	H14	I/O		Default: JTMS, SWDIO, PA13 Alternate: TIMER0_BRKIN1, TIMER7_BRKIN1, SPI1_NSS, I2S1_WS, UART3_RX, USART0_CTS, CAN0_RX, EXMC_INT, TRIGSEL_IN10, EVENTOUT
PA14	F15	I/O		Default: JTCK, SWCLK, PA14 Alternate: SPI1_SCK, I2S1_CK, UART3_TX, USART0_RTS, USART0_DE, CAN0_TX, TIMER0_BRKIN2, TRIGSEL_IN11, EVENTOUT
PA15	D15	I/O		Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, SPI5_NSS, I2S5_WS, UART3_RTS, UART3_DE, UART6_TX, TRIGSEL_OUT0, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB0	U5	I/O		Default: PB0 Alternate: TIMER0_MCH1, TIMER2_CH2, TIMER7_MCH1, OSPIM_P0_IO1, HPDF_CKOUT, UART3_CTS, USBHS0_ULPI_D1(4), TRIGSEL_OUT3, EVENTOUT Additional: ADC01_IN9, CMP0_IP0
PB1	T5	I/O		Default: PB1 Alternate: TIMER0_MCH2, TIMER2_CH3, TIMER7_MCH2, OSPIM_P0_IO0, HPDF_DATAIN1, USBHS0_ULPI_D2(4), TRIGSEL_OUT4, EVENTOUT Additional: ADC01_IN5, CMP0_IM6
PB2	R6	I/O		Default: PB2 Alternate: RTC_OUT, EXMC_D10, HPDF_CKIN1, SPI2_MOSI, I2S2_SD, OSPIM_P0_SCK, EXMC_NCE, TIMER22_ETI, EVENTOUT Additional: CMP0_IP1
PB3	B6	I/O		Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, I2S0_CK, SPI2_SCK, I2S2_CK, SPI5_SCK, I2S5_CK, CTC_SYNC, UART6_RX, TRIGSEL_OUT7, TIMER23_ETI, EVENTOUT
PB4	C5	I/O		Default: NJTRST, PB4 Alternate: TIMER15_BRKIN0, TIMER2_CH0, SPI0_MISO, SPI2_MISO, SPI1_NSS, I2S1_WS, SPI5_MISO, UART6_TX, TRIGSEL_OUT6, EVENTOUT
PB5	A3	I/O		Default: PB5 Alternate: TIMER16_BRKIN0, TIMER2_CH1, I2C0_SMBA, SPI0_MOSI, I2S0_SD, I2C3_SMBA, SPI2_MOSI, I2S2_SD, SPI5_MOSI, I2S5_SD, CAN1_RX, USBHS0_ULPI_D7(4), EXMC_SDCKE1, UART4_RX, EVENTOUT
PB6	A2	I/O		Default: PB6 Alternate: TIMER15_MCH0, TIMER3_CH0, EXMC_D11, I2C0_SCL, I2C3_SCL, USART0_TX, CAN1_TX, OSPIM_P0_CSN, HPDF_DATAIN5, EXMC_SDNE1, UART4_TX, EVENTOUT
PB7	B4	I/O		Default: PB7 Alternate: TIMER16_MCH0, TIMER3_CH1, I2C0_SDA, I2C3_SDA, USART0_RX, HPDF_CKIN5, EXMC_NL, EXMC_NADV, EVENTOUT Additional: PVD_IN
PB8	D5	I/O		Default: PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, I2C3_SCL, UART3_RX, CAN0_RX, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB9	D4	I/O		Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, SPI1_NSS, I2S1_WS, I2C3_SDA, UART3_TX, CAN0_TX, I2C3_SMBA, EVENTOUT
PB10	P11	I/O		Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, HPDF_DATAIN7, USART2_TX, OSPIM_P0_CSN, USBHS0_ULPI_D3(4), TRIGSEL_OUT2, EVENTOUT
PB11	P12	I/O		Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, HPDF_CKIN7, USART2_RX, USBHS0_ULPI_D4(4), USBHS1_SOF(4), EVENTOUT
PB12	R14	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN0, I2C1_SMBA, SPI1_NSS, I2S1_WS, HPDF_DATAIN1, USART2_CK, CAN1_RX, USBHS0_ULPI_D5(4), OSPIM_P0_IO0, CMP_MUX_OUT2, UART4_RX, EVENTOUT Additional: USBHS1_VBUS(4)
PB13	U14	I/O	5VT	Default: PB13 Alternate: RTC_REFIN, TIMER0_MCH0, OSPIM_P0_IO2, SPI1_SCK, I2S1_CK, HPDF_CKIN1, USART2_CTS, USBHS1_ID(4), CAN1_TX, USBHS0_ULPI_D6(4), UART4_TX, EVENTOUT
USBHS1_DM-PB14	T14	I/O		Default: USBHS1_DM(4) Alternate: TIMER0_MCH1, TIMER7_MCH1, USART0_TX, SPI1_MISO, HPDF_DATAIN2, USART2_RTS, USART2_DE, UART3_RTS, UART3_DE, EXMC_D10, TRIGSEL_OUT1, EVENTOUT
USBHS1_DP-PB15	T15	I/O		Default: USBHS1_DP(4) Alternate: RTC_REFIN, TIMER0_MCH2, TIMER7_MCH2, USART0_RX, SPI1_MOSI, I2S1_SD, HPDF_CKIN2, UART3_CTS, EXMC_D11, TRIGSEL_OUT5, EVENTOUT
PC0	U6	I/O		Default: PC0 Alternate: EXMC_D12, HPDF_CKIN0, HPDF_DATAIN4, TIMER40_CH0, EXMC_A25, USBHS0_ULPI_STP(4), EXMC_SDNWE, TRIGSEL_IN8, EVENTOUT Additional: ADC012_IN10
PC1	M2	I/O		Default: PC1 Alternate: TRACED0, HPDF_DATAIN0, HPDF_CKIN4, SPI1_MOSI, I2S1_SD, TIMER40_MCH0, OSPIM_P0_IO4, TRIGSEL_IN9, EVENTOUT Additional: ADC012_IN11, RTC_TAMP2, WKUP5

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC2	M3	I/O		Default: PC2 Alternate: PMU_DEEPSLEEP, HPDF_CKIN1, OSPIM_P0_IO5, SPI1_MISO, HPDF_CKOUT, OSPIM_P0_IO2, USBHS0_ULPI_DIR(4), EXMC_SDNE0, TRIGSEL_IN2, EVENTOUT Additional: ADC012_IN12
PC2_C	R1	I/O		Default: PC2_C(4) Additional: ADC2_IN0
PC3	T8	I/O		Default: PC3 Alternate: PMU_SLEEP, HPDF_DATAIN1, OSPIM_P0_IO6, SPI1_MOSI, I2S1_SD, OSPIM_P0_IO0, USBHS0_ULPI_NXT(4), EXMC_SDCKE0, EVENTOUT Additional: ADC01_IN13
PC3_C	R2	I/O		Default: PC3_C(4) Additional: ADC2_IN1
PC4	T4	I/O		Default: PC4 Alternate: PMU_DEEPSLEEP, EXMC_A22, HPDF_CKIN2, I2S0_MCK, TIMER41_CH0, EXMC_SDNE0, EVENTOUT Additional: ADC01_IN4, CMP0_IM7
PC5	U4	I/O		Default: PC5 Alternate: PMU_SLEEP, HPDF_DATAIN2, TIMER41_MCH0, EXMC_SDCKE0, CMP0_OUT, EVENTOUT Additional: ADC01_IN8
PC6	L15	I/O		Default: PC6 Alternate: TIMER0_BRKIN1, TIMER2_CH0, TIMER7_CH0, HPDF_CKIN3, I2S1_MCK, USART5_TX, EXMC_NWAIT, EVENTOUT
PC7	K15	I/O		Default: PC7 Alternate: TIMER0_CH3, TIMER2_CH1, TIMER7_CH1, HPDF_DATAIN3, I2S2_MCK, USART5_RX, EXMC_NE0, EVENTOUT
PC8	K14	I/O		Default: PC8 Alternate: TRACED1, TIMER2_CH2, TIMER7_CH2, USART5_CK, UART4_RTS, UART4_DE, EXMC_NE1, EXMC_INT, EVENTOUT
PC9	M16	I/O		Default: PC9 Alternate: CK_OUT1, TIMER0_MCH3, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, UART4_CTS, OSPIM_P0_IO0, EVENTOUT
PC10	E15	I/O		Default: PC10 Alternate: TIMER0_CH3, HPDF_CKIN5, SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, OSPIM_P0_IO1, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC11	D16	I/O		Default: PC11 Alternate: TIMER0_ETI, HPDF_DATAIN5, SPI2_MISO, USART2_RX, UART3_RX, OSPIM_P0_CSN, EXMC_NBL2, EVENTOUT
PC12	C15	I/O		Default: PC12 Alternate: TRACED3, EXMC_D6, TIMER14_CH0, SPI5_SCK, I2S5_CK, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, EVENTOUT
PC13	J5	I/O		Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_TS, WKUP3, RTC_OUT
PC14-OSC32IN	C2	I/O		Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	C1	I/O		Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PD0	E14	I/O		Default: PD0 Alternate: TIMER7_CH2, HPDF_CKIN6, UART3_RX, CAN0_RX, EXMC_D2, TRIGSEL_IN3, EVENTOUT
PD1	E13	I/O		Default: PD1 Alternate: HPDF_DATAIN6, UART3_TX, CAN0_TX, EXMC_D3, TRIGSEL_IN6, EVENTOUT
PD2	B16	I/O		Default: PD2 Alternate: TRACED2, EXMC_D7, TIMER2_ETI, TIMER14_BRKIN0, UART4_RX, EVENTOUT
PD3	B15	I/O		Default: PD3 Alternate: HPDF_CKOUT, SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, EVENTOUT
PD4	D14	I/O		Default: PD4 Alternate: TIMER7_MCH3, USART1_RTS, USART1_DE, OSPIM_P0_IO4, EXMC_NOE, EVENTOUT
PD5	A15	I/O		Default: PD5 Alternate: TIMER7_CH3, USART1_TX, OSPIM_P0_IO5, EXMC_NWE, EVENTOUT
PD6	C14	I/O		Default: PD6 Alternate: HPDF_CKIN4, HPDF_DATAIN1, SPI2_MOSI, I2S2_SD, USART1_RX, OSPIM_P0_IO6, EXMC_NWAIT, EVENTOUT
PD7	D13	I/O		Default: PD7 Alternate: HPDF_DATAIN4, SPI0_MOSI, I2S0_SD, HPDF_CKIN1, USART1_CK, OSPIM_P0_IO7, EXMC_NE0, EXMC_NCE, EVENTOUT

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PD8	T17	I/O		Default: PD8 Alternate: HPDF_CKIN3, USART2_TX, EXMC_D13, EVENTOUT
PD9	U16	I/O		Default: PD9 Alternate: HPDF_DATAIN3, USART2_RX, EXMC_D14, EVENTOUT
PD10	T16	I/O		Default: PD10 Alternate: HPDF_CKOUT, USART2_CK, EXMC_D15, EVENTOUT
PD11	R15	I/O		Default: PD11 Alternate: TIMER40_CH1, TIMER7_MCH3, I2C3_SMBA, USART2_CTS, OSPIM_P0_IO0, EXMC_A16/EXMC_CLE, EVENTOUT
PD12	R16	I/O		Default: PD12 Alternate: TIMER41_CH1, TIMER3_CH0, I2C3_SCL, CAN2_RX, EDOUT_A, USART2_RTS, USART2_DE, OSPIM_P0_IO1, EXMC_A17/EXMC_ALE, EVENTOUT
PD13	R17	I/O		Default: PD13 Alternate: TIMER42_CH1, TIMER3_CH1, I2C3_SDA, CAN2_TX, EDOUT_B, OSPIM_P0_IO3, EXMC_A18, EVENTOUT
PD14	P16	I/O		Default: PD14 Alternate: TIMER43_CH1, TIMER3_CH2, SPI3_IO2, EDOUT_Z, UART7_CTS, EXMC_D0, EVENTOUT
PD15	P15	I/O		Default: PD15 Alternate: TIMER44_CH1, TIMER3_CH3, SPI3_IO3, UART7_RTS, UART7_DE, EXMC_D1, EVENTOUT
PDR_ON	E7	P	-	Default: PDR_ON(3)
PE0	C4	I/O		Default: PE0 Alternate: TIMER3_ETI, UART7_RX, EXMC_NBL0, EVENTOUT
PE1	B3	I/O		Default: PE1 Alternate: UART7_TX, EXMC_NBL1, EVENTOUT
PE2	C3	I/O		Default: PE2 Alternate: TRACECK, SPI3_SCK, OSPIM_P0_IO2, EXMC_A23, EVENTOUT
PE3	D3	I/O		Default: PE3 Alternate: TRACED0, TIMER14_BRKIN0, EXMC_A19, EVENTOUT
PE4	D2	I/O		Default: PE4 Alternate: TRACED1 , TIMER0_BRKIN1, HPDF_DATAIN3, TIMER14_MCH0, SPI3_NSS, EXMC_A20, EVENTOUT

GD32H75Exx BGA240				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE5	D1	I/O		Default: PE5 Alternate: TRACED2 , HPDF_CKIN3, TIMER14_CH0 , SPI3_MISO, EXMC_A21, EVENTOUT
PE6	G3	I/O		Default: PE6 Alternate: TRACED3 , TIMER0_BRKIN2, TIMER14_CH1 , SPI3_MOSI, CMP_MUX_OUT3, EXMC_A22, EVENTOUT
PE7	U9	I/O		Default: PE7 Alternate: TIMER0_ETI, HPDF_DATAIN2, UART6_RX, OSPIM_P0_IO4, EXMC_D4, EVENTOUT Additional: CMP1_IM7
PE8	T9	I/O		Default: PE8 Alternate: TIMER0_MCH0, HPDF_CKIN2, UART6_TX, OSPIM_P0_IO5, EXMC_D5, CMP1_OUT, EVENTOUT
PE9	P9	I/O		Default: PE9 Alternate: TIMER0_CH0, HPDF_CKOUT, SPI3_IO2, UART6_RTS, UART6_DE, OSPIM_P0_IO6, EXMC_D6, EVENTOUT Additional: CMP1_IP0
PE10	N9	I/O		Default: PE10 Alternate: TIMER0_MCH1, HPDF_DATAIN4, SPI3_IO3, UART6_CTS, OSPIM_P0_IO7, EXMC_D7, EVENTOUT Additional: CMP1_IM6
PE11	P10	I/O		Default: PE11 Alternate: TIMER0_CH1, HPDF_CKIN4, SPI3_NSS, OSPIM_P0_CSN, EXMC_D8, EVENTOUT Additional: CMP1_IP1
PE12	R10	I/O		Default: PE12 Alternate: TIMER0_MCH2, HPDF_DATAIN5, SPI3_SCK, EXMC_D9, CMP0_OUT, EVENTOUT
PE13	T10	I/O		Default: PE13 Alternate: TIMER0_CH2, HPDF_CKIN5, SPI3_MISO, EXMC_D10, CMP1_OUT, EVENTOUT
PE14	U10	I/O		Default: PE14 Alternate: TIMER0_CH3, SPI3_MOSI, EXMC_D11, EVENTOUT
PE15	U11	I/O		Default: PE15 Alternate: TIMER0_BRKIN0, EXMC_D12, CMP_MUX_OUT4, EVENTOUT
PF5	N6	I/O		Default: PF5 Alternate: TIMER0_MCH2, TIMER7_MCH2, USART0_RX, HPDF_CKIN2, UART3_CTS, EXMC_A5, TRIGSEL_OUT5, EVENTOUT Additional: ADC2_IN4

GD32H75Exx BGA240				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PF6	T6	I/O		Default: PF6 Alternate: TIMER15_CH0, CAN2_RX, SPI4_NSS, UART6_RX, OSPIM_P0_IO3, EXMC_D24, TIMER22_CH0, EVENTOUT Additional: ADC2_IN8
PF7	P5	I/O		Default: PF7 Alternate: TIMER16_CH0, CAN2_TX, SPI4_SCK, UART6_TX, OSPIM_P0_IO2, EXMC_D25, TIMER22_CH1, EVENTOUT Additional: ADC2_IN3
PF8	P6	I/O		Default: PF8 Alternate: TIMER15_MCH0, SPI4_MISO, UART6_RTS, UART6_DE, OSPIM_P0_IO0, EXMC_D26, TIMER22_CH2, EVENTOUT Additional: ADC2_IN7
PF9	U8	I/O		Default: PF9 Alternate: TIMER16_MCH0, SPI4_MOSI, UART6_CTS, OSPIM_P0_IO1, EXMC_D27, TIMER22_CH3, EVENTOUT Additional: ADC2_IN2
PF10	U7	I/O		Default: PF10 Alternate: TIMER15_BRKIN0, OSPIM_P0_SCK, EVENTOUT Additional: ADC2_IN6
PF11	T7	I/O		Default: PF11 Alternate: SPI4_MOSI, EXMC_SDNRAS, TIMER23_CH0, EVENTOUT Additional: ADC0_IN2
PF12	R7	I/O		Default: PF12 Alternate: EXMC_A6, TIMER23_CH1, EVENTOUT Additional: ADC0_IN6
PF13	P7	I/O		Default: PF13 Alternate: HPDF_DATAIN6, I2C3_SMBA, EXMC_A7, TIMER23_CH2, EVENTOUT Additional: ADC1_IN2
PF14	P8	I/O		Default: PF14 Alternate: HPDF_CKIN6, I2C3_SCL, SPI4_IO2, EXMC_A8, TIMER23_CH3, EVENTOUT Additional: ADC1_IN6
PF15	R9	I/O		Default: PF15 Alternate: I2C3_SDA, SPI4_IO3, EXMC_A9, EVENTOUT
PG6	L14	I/O		Default: PG6 Alternate: TIMER16_BRKIN0, OSPIM_P0_CSN, EXMC_NE2, EVENTOUT

GD32H75Exx BGA240				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PG7	N16	I/O		Default: PG7 Alternate: EXMC_D28, USART5_CK, EXMC_INT, EVENTOUT
PG8	N17	I/O		Default: PG8 Alternate: TIMER7_ETI, SPI5_NSS, I2S5_WS, USART5_RTS, USART5_DE, EXMC_SDCLK, EVENTOUT
PG9	E12	I/O		Default: PG9 Alternate: EXMC_D30, CAN2_TX, TIMER7_BRKIN1, SPI0_MISO, USART5_RX, OSPIM_P0_IO6, EXMC_NE1, EVENTOUT
PG13	D9	I/O		Default: PG13 Alternate: TRACED0, SPI5_SCK, I2S5_CK, USART5_CTS, TIMER44_CH0, EXMC_A24, TIMER22_CH1, EVENTOUT
PG14	D8	I/O		Default: PG14 Alternate: TRACED1, SPI5_MOSI, I2S5_SD, USART5_TX, TIMER44_MCH0, OSPIM_P0_IO7, EXMC_A25, TIMER22_CH2, EVENTOUT
PG15	C6	I/O		Default: PG15 Alternate: USART5_CTS, TIMER44_BRKIN0, EXMC_SDNCAS, EVENTOUT
PH0-OSCIN	J2	I/O		Default: PH0 Alternate: EVENTOUT Additional: OSCIN
PH1-OSCOUT	J1	I/O		Default: PH1 Alternate: EVENTOUT Additional: OSCOUT
PH2	N2	I/O		Default: PH2 Alternate: TIMER40_CH0, USBHS1_ULPI_STP(4), OSPIM_P0_IO4, EXMC_SDCKEN0, EVENTOUT Additional: ADC2_IN13
PH3	P2	I/O		Default: PH3 Alternate: TIMER40_MCH0, USBHS1_ULPI_DIR(4), OSPIM_P0_IO5, EXMC_SDNE0, EVENTOUT Additional: ADC2_IN14
PH4	P3	I/O		Default: PH4 Alternate: I2C1_SCL, TIMER40_BRKIN0, USBHS1_ULPI_NXT(4), USBHS0_ULPI_NXT(4), EXMC_NBL3, EVENTOUT Additional: ADC2_IN15
PH5	P4	I/O		Default: PH5 Alternate: I2C1_SDA, SPI4_NSS, TIMER41_CH0, USBHS1_ULPI_CK(4), EXMC_SDNWE, EVENTOUT Additional: ADC2_IN16

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Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PH6	T12	I/O		Default: PH6 Alternate: I2C1_SMBA, SPI4_SCK, TIMER41_MCH0, USBHS1_ULPI_D0(4), EXMC_SDNE1, EVENTOUT
PH7	P13	I/O		Default: PH7 Alternate: EDOUT_A, I2C2_SCL, SPI4_MISO, TIMER41_BRKIN0, USBHS1_ULPI_D1(4), EXMC_SDCKE1, EVENTOUT
PH8	R13	I/O		Default: PH8 Alternate: TIMER4_ETI, EDOUT_B, I2C2_SDA, SPI4_IO2, TIMER42_CH0, USBHS1_ULPI_D2(4), EXMC_D16, EVENTOUT
PH9	U12	I/O		Default: PH9 Alternate: EDOUT_Z, I2C2_SMBA, SPI4_IO3, TIMER42_MCH0, USBHS1_ULPI_D3(4), EXMC_D17, EVENTOUT
PH10	T13	I/O		Default: PH10 Alternate: TIMER4_CH0, I2C3_SMBA, TIMER42_BRKIN0, USBHS1_ULPI_D4(4), EXMC_D18, EVENTOUT
PH11	U13	I/O		Default: PH11 Alternate: TIMER4_CH1, I2C3_SCL, TIMER43_CH0, USBHS1_ULPI_D5(4), EXMC_D19, EVENTOUT
PH12	P14	I/O		Default: PH12 Alternate: TIMER4_CH2, I2C3_SDA, TIMER43_MCH0, USBHS1_ULPI_D6(4), EXMC_D20, EVENTOUT
PH13	G15	I/O		Default: PH13 Alternate: TIMER7_MCH0, TIMER43_BRKIN0, UART3_TX, CAN0_TX, EXMC_D21, EVENTOUT
VBAT	B1	P	-	Default: VBAT
VCAP	E3	P	-	Default: VCAP
VCAP	H15	P	-	Default: VCAP
VCAP	T11	P	-	Default: VCAP
VDD	F3	P	-	Default: VDD
VDD	F4	P	-	Default: VDD
VDD	G4	P	-	Default: VDD
VDD	G13	P	-	Default: VDD
VDD	H4	P	-	Default: VDD
VDD	H5	P	-	Default: VDD
VDD	H13	P	-	Default: VDD
VDD	J3	P	-	Default: VDD
VDD	J13	P	-	Default: VDD
VDD	K5	P	-	Default: VDD
VDD	K13	P	-	Default: VDD
VDD	L5	P	-	Default: VDD

GD32H75Exx BGA240				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VDD	L13	P	-	Default: VDD
VDD	M5	P	-	Default: VDD
VDD	M13	P	-	Default: VDD
VDD	N7	P	-	Default: VDD
VDD	N8	P	-	Default: VDD
VDD	N10	P	-	Default: VDD
VDD	N11	P	-	Default: VDD
VDD	N12	P	-	Default: VDD
VDD	N13	P	-	Default: VDD
VSS	A1	P	-	Default: VSS
VSS	A16	P	-	Default: VSS
VSS	A17	P	-	Default: VSS
VSS	B2	P	-	Default: VSS
VSS	C12	P	-	Default: VSS
VSS	C16	P	-	Default: VSS
VSS	E2	P	-	Default: VSS
VSS	E16	P	-	Default: VSS
VSS	G16	P	-	Default: VSS
VSS	H1	P	-	Default: VSS
VSS	J16	P	-	Default: VSS
VSS	L2	P	-	Default: VSS
VSS	L3	P	-	Default: VSS
VSS	M4	P	-	Default: VSS
VSS	P17	P	-	Default: VSS
VSS	R4	P	-	Default: VSS
VSS	R8	P	-	Default: VSS
VSS	U1	P	-	Default: VSS
VSS	U15	P	-	Default: VSS
VSS	U17	P	-	Default: VSS
VDD33USB(5)	K17	P	-	Default: VDD33USB(5)
VDD50USB	M17	P	-	Default: VDD50USB
VDDLDO	G5	P	-	Default: VDDLDO
VDDLDO	R11	P	-	Default: VDDLDO
VDDLDO	R12	P	-	Default: VDDLDO
VDDSMPS	F1	P	-	Default: VDDSMPS
VDDA	L1	P	-	Default: VDDA
VFBSMPS	G2	P	-	Default: VFBSMPS
VLXSMPS	E1	P	-	Default: VLXSMPS
VREFN	N1	P	-	Default: VREFN

GD32H75Exx BGA240				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VREFP	M1	P	-	Default: VREFP
VSSSMPS	G1	P	-	Default: VSSSMPS
VSSA	P1	P	-	Default: VSSA
IO4	A4	I/O	5VT	Default: IO4 Alternate: PDI_GPIO4, MII0_TX_EN, MII2_TX_EN
IO6	A5	I/O	5VT	Default: IO6 Alternate: PDI_GPIO6, MII0_TXD1, MII2_TXD1
VDDIO	A6	P		Default: VDDIO
VDDIO	A7	P		Default: VDDIO
IO7	A8	I/O	5VT	Default: IO7 Alternate: PDI_GPIO7, MII0_TXD2, MII2_TXD2, TX_SHIFT0
RSTN	A9	-		Default: RSTN Additional: RSTN
REG_EN	A10	I/O		Default: REG_EN Additional: REG_EN
OSCI	A11	I/O		Default: OSCI Additional: OSCI
OSCVDD11	A12	P		Default: OSCVDD11
VDD1A2	A13	P		Default: VDD1A2
VDD1A1	A14	P		Default: VDD1A1
IO5	B5	I/O	5VT	Default: IO5 Alternate: PDI_GPIO5, MII0_TXD0, MII2_TXD0
SYNC1_LATCH1	B7	I/O	5VT	Default: SYNC1_LATCH1 Alternate: SYNC1, LATCH1
IO8	B8	I/O	5VT	Default: IO8 Alternate: PDI_GPIO8, MII0_TXD3, MII2_TXD3, TX_SHIFT1
IO16	B9	I/O	5VT	Default: IO16 Alternate: MCU_PDI_TYPE Additional: VBG11
VDD33	B10	P		Default: VDD33
OSCO	B11	I/O		Default: OSCO Additional: OSCO
VDD3A2	B12	P		Default: VDD3A2
RTXB	B13	I/O		Default: RTXB
IO3	B14	I/O	5VT	Default: IO3 Alternate: PDI_GPIO3, MII2_LINK, MII0_LINK
RXNB	B17	I/O		Default: RXNB
VCORE	C7	P		Default: VCORE
VDDIO	C8	P		Default: VDDIO
IO17	C9	I/O	5VT	Default: IO17 Alternate: EFUSE_LDO_BYP
VCORE	C10	P		Default: VCORE

GD32H75Exx BGA240				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
OSCVSS	C11	P		Default: OSCVSS
RTXA	C13	I/O		Default: RTXA Additional: RTX_P1
RXPB	C17	I/O		Default: RXPB Additional: RTX_P2
IO11	D6	I/O	5VT	Default: IO11 Alternate: PDI_GPIO11, MII2_RX_DV, MII0_RX_DV
OE_EXT	D7	I/O	5VT	Default: OE_EXT Alternate: MII_CLK25
IO18	D10	I/O	5VT	Default: IO18 Alternate: PHYRST_MODE
VCORE	D11	P		Default: VCORE
VDD3A1	D12	P		Default: VDD3A1
TXNB	D17	I/O		Default: TXNB Additional: TXN_P2
IO12	E4	I/O	5VT	Default: IO12 Alternate: PDI_GPIO12, MII0_RXD0, MII2_RXD0
IO13	E5	I/O	5VT	Default: IO13 Alternate: PDI_GPIO13, MII0_RXD1, MII2_RXD1
IO15	E6	I/O	5VT	Default: IO15 Alternate: PDI_GPIO15, MII0_RXD3, MII2_RXD3
VDDIO	E9	P		Default: VDDIO
VDDIO	E10	P		Default: VDDIO
LINKACTLED0	E11	I/O	5VT	Default: LINKACTLED0 Alternate: LINKACTLED0, CHIP_MODE0
TXPB	E17	I/O		Default: TXPB Additional: TXP_P2
IO10	F2	I/O	5VT	Default: IO10 Alternate: PDI_GPIO10, MII0_LINKPOL, LINKACTLED2
IO14	F5	I/O	5VT	Default: IO14 Alternate: PDI_GPIO14, MII0_RXD2, MII2_RXD2
LINKACTLED1	F13	I/O	5VT	Default: LINKACTLED1 Alternate: LINKACTLED1, CHIP_MODE1
EESIZE	F14	I/O	5VT	Default: EESIZE Alternate: EEPROM_SIZE, RUNLED
SOF	F16	I/O	5VT	Default: SOF
RXNA	F17	I/O		Default: RXNA Additional: RXN_P1
TESTMODE	G14	I/O	5VT	Default: TESTMODE Alternate: TESTMODE
RXPA	G17	I/O		Default: RXPA Additional: RXP_P1
IO9	H2	I/O	5VT	Default: IO9

GD32H75Exx BGA240				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: PDI_GPIO9, MII0_RX_ER, MII2_RX_ER
SYNC0_LATCH0	H3	I/O	5VT	Default: SYNC0_LATCH0 Alternate: SYNC0, LATCH0
EOF	H16	I/O	5VT	Default: EOF
TXNA	H17	I/O		Default: TXNA Additional: TXN_P1
IO1	J4	I/O	5VT	Default: IO1 Alternate: PDI_GPIO1, MII_CLK
TXPA	J17	I/O		Default: TXPA Additional: TXP_P1
IO0	K2	I/O	5VT	Default: IO0 Alternate: PDI_GPIO0, MII0_RX_CLK, MII2_RX_CLK
IO2	K3	I/O	5VT	Default: IO2 Alternate: PDI_GPIO2, MII_DATA
EESCL	K4	I/O	5VT	Default: EESCL Alternate: EEPROM_CLK
EESDA	L4	I/O	5VT	Default: EESDA Alternate: EEPROM_DATA
LATCH_IN	M14	I/O	5VT	Default: LATCH_IN
WD_STATE	M15	I/O	5VT	Default: WD_STATE
WD_TRIG	N14	I/O	5VT	Default: WD_TRIG
OUTVALID	N15	I/O	5VT	Default: OUTVALID

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) PDR_ON pin should be pulled up to V_{DD}.

(4) The USBHS includes an embedded USB PHY internally, but only supports Full-Speed. If users wish to utilize High-Speed mode, an external PHY is needed.

The voltage difference between VDD and VDD33USB should not exceed 0.3V.

2.6.2. GD32H75Exx pin alternate functions

Table 2-3. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		TIMER1_CH0/TIMER1_ETI	TIMER4_CH0	TIMER7_ETI	TIMER14_BRKIN0	SPI5_NSS/I2S5_WS	OSPIM_P0_IO6	USART1_CTS	UART3_TX				EXMC_A19	TRIGSEL_IN0		EVENTOUT
PA1		TIMER1_CH1	TIMER4_CH1		TIMER14_MCH0			USART1_RTS/USART1_DE	UART3_RX	OSPIM_P0_IO3				TRIGSEL_IN1		EVENTOUT
PA2		TIMER1_CH2	TIMER4_CH2		TIMER14_CH0		OSPIM_P0_IO0	USART1_TX						TRIGSEL_IN7		EVENTOUT
PA3		TIMER1_CH3	TIMER4_CH3		TIMER14_CH1	I2S5_MCK	OSPIM_P0_IO2	USART1_RX			USBHS0_ULPI_D0		OSPIM_P0_SCK	TRIGSEL_IN4		EVENTOUT
PA4			TIMER4_ETI			SPI0_NSS/I2S0_WS	SPI2_NSS/I2S2_WS	USART1_CK	SPI5_NSS/I2S5_WS				EXMC_D8			EVENTOUT
PA5		TIMER1_CH0/TIMER1_ETI		TIMER7_MCH0		SPI0_SCK/I2S0_CK			SPI5_SCK/I2S5_CK		USBHS0_ULPI_CK		EXMC_D9			EVENTOUT
PA6		TIMER0_BRKIN0	TIMER2_CH0	TIMER7_BRKIN0		SPI0_MISO	OSPIM_P0_IO3		SPI5_MISO		CMP_MUX_OUT0					EVENTOUT
PA7		TIMER0_MCH0	TIMER2_CH1	TIMER7_MCH0		SPI0_MOSI/I2S0_SD			SPI5_MOSI/I2S5_SD		OSPIM_P0_IO2		EXMC_SDNWE	TRIGSEL_IN5		EVENTOUT
PA8	CK_OUT0	TIMER0_CH0		TIMER7_BRKIN2	I2C2_SCL			USART0_CK			USBHS0_SOF	UART6_RX	CMP_MUX_OUT1			EVENTOUT
PA9		TIMER0_CH1			I2C2_SMBA	SPI1_SCK/I2S1_CK		USART0_TX		TRIGSEL_IN13						EVENTOUT
PA10		TIMER0_CH2						USART0_RX			USBHS0_ID					EVENTOUT
PA11		TIMER0_CH3				SPI1_NSS/I2S1_WS	UART3_RX	USART0_CTS		CAN0_RX				TRIGSEL_IN13		EVENTOUT
PA12		TIMER0_ETI				SPI1_SCK/I2S1_CK	UART3_TX	USART0_RTS/USART0_DE		CAN0_TX			TIMER0_BRKIN2	TRIGSEL_IN12		EVENTOUT
PA13	JTMS/SWDIO	TIMER0_BRKIN1		TIMER7_BRKIN1		SPI1_NSS/I2S1	UART3_RX	USART0_CTS		CAN0_RX			EXMC_INT	TRIGSEL_IN10		EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
						_WS										
PA14	JTCK/SWCLK					SPI1_SCK/I2S1_CK	UART3_TX	USART0_RTS/USART0_DE		CAN0_TX			TIMER0_BRKIN2	TRIGSEL_IN11		EVENTOUT
PA15	JTDI	TIMER1_CH0/TIMER1_ETI				SPI0_NSS/I2S0_WS	SPI2_NSS/I2S2_WS	SPI5_NSS/I2S5_WS	UART3_RTS/UART3_DE			UART6_TX		TRIGSEL_OUT0		EVENTOUT

Table 2-4. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER0_MCH1	TIMER2_CH2	TIMER7_MCH1	OSPIM_P0_IO1		HPDF_CKOUT		UART3_CTS		USBHS0_ULPI_D1			TRIGSEL_OUT3		EVENTOUT
PB1		TIMER0_MCH2	TIMER2_CH3	TIMER7_MCH2	OSPIM_P0_IO0		HPDF_DATAIN1				USBHS0_ULPI_D2			TRIGSEL_OUT4		EVENTOUT
PB2	RTC_OUT			EXMC_D10	HPDF_CKIN1			SPI2_MOSI/I2S2_SD		OSPIM_P0_SCK		EXMC_NCE		TIMER22_ETI		EVENTOUT
PB3	JTDO/TRACESWO	TIMER1_CH1				SPI0_SCK/I2S0_CK	SPI2_SCK/I2S2_CK		SPI5_SCK/I2S5_CK		CTC_SYNC	UART6_RX		TRIGSEL_OUT7	TIMER23_ETI	EVENTOUT
PB4	NJTRST	TIMER15_BRKIN0	TIMER2_CH0			SPI0_MISO	SPI2_MISO	SPI1_NSS/I2S1_WS	SPI5_MISO			UART6_TX		TRIGSEL_OUT6		EVENTOUT
PB5		TIMER16_BRKIN0	TIMER2_CH1		I2C0_SMBA	SPI0_MOSI/I2S0_SD	I2C3_SMBA	SPI2_MOSI/I2S2_SD	SPI5_MOSI/I2S5_SD	CAN1_RX	USBHS0_ULPI_D7		EXMC_SDCKE1		UART4_RX	EVENTOUT
PB6		TIMER15_MCH0	TIMER3_CH0	EXMC_D11	I2C0_SCL		I2C3_SCL	USART0_TX		CAN1_TX	OSPIM_P0_CSN	HPDF_DATAIN5	EXMC_SDNE1		UART4_TX	EVENTOUT
PB7		TIMER16_MCH0	TIMER3_CH1		I2C0_SDA		I2C3_SDA	USART0_RX				HPDF_CKIN5	EXMC_NL/EXMC_NADV,			EVENTOUT
PB8		TIMER15_CH0	TIMER3_CH2	HPDF_CKIN7	I2C0_SCL		I2C3_SCL		UART3_RX	CAN0_RX						EVENTOUT
PB9		TIMER16_CH0	TIMER3_CH3	HPDF_DATAIN7	I2C0_SDA	SPI1_NSS/I2S1_WS	I2C3_SDA		UART3_TX	CAN0_TX		I2C3_SMBA				EVENTOUT
PB10		TIMER1_CH2			I2C1_SCL	SPI1_SCK/I2S1_CK	HPDF_DATAIN7	USART2_TX		OSPIM_P0_CSN	USBHS0_ULPI_D3			TRIGSEL_OUT2		EVENTOUT
PB11		TIMER1_CH3			I2C1_SDA		HPDF_CKIN7	USART2_RX			USBHS0_ULPI_D4		USBHS1_SOF			EVENTOUT
PB12		TIMER0_BRKIN0			I2C1_SMBA	SPI1_NSS/I2S1_WS	HPDF_DATAIN1	USART2_CK		CAN1_RX	USBHS0_ULPI_D5		OSPIM_P0_IO0	CMP_MUX_OUT2	UART4_RX	EVENTOUT
PB13	RTC_REFIN	TIMER0_MCH0			OSPIM_P0_IO2	SPI1_SCK/I2S1_CK	HPDF_CKIN1	USART2_CTS	USBHS1_ID	CAN1_TX	USBHS0_ULPI_D6				UART4_TX	EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB14		TIMER0_MCH1		TIMER7_MCH1	USART0_TX	SPI1_MISO	HPDF_DATAIN2	USART2_RTS/USART2_DE	UART3_RTS/UART3_DE				EXMC_D10	TRIGSEL_OUT1		EVENTOUT
PB15	RTC_REFIN	TIMER0_MCH2		TIMER7_MCH2	USART0_RX	SPI1_MOSI/I2S1_SD	HPDF_CKIN2		UART3_CTS				EXMC_D11	TRIGSEL_OUT5		EVENTOUT

Table 2-5. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0		EXMC_D12		HPDF_CKIN0			HPDF_DATAIN4	TIMER40_CH0		EXMC_A25	USBHS0_ULPI_STP		EXMC_SDNWE	TRIGSEL_IN8		EVENTOUT
PC1	TRACED0			HPDF_DATAIN0	HPDF_CKIN4	SPI1_MOSI/I2S1_SD		TIMER40_MCH0			OSPIM_P0_IO4			TRIGSEL_IN9		EVENTOUT
PC2	PMU_DEEPSLEEP			HPDF_CKIN1	OSPIM_P0_IO5	SPI1_MISO	HPDF_CKOUT			OSPIM_P0_IO2	USBHS0_ULPI_DIR		EXMC_SDNE0	TRIGSEL_IN2		EVENTOUT
PC3	PMU_SLEEP			HPDF_DATAIN1	OSPIM_P0_IO6	SPI1_MOSI/I2S1_SD				OSPIM_P0_IO0	USBHS0_ULPI_NXT		EXMC_SDCKE0			EVENTOUT
PC4	PMU_DEEPSLEEP	EXMC_A22		HPDF_CKIN2		I2S0_MCK		TIMER41_CH0					EXMC_SDNE0			EVENTOUT
PC5	PMU_SLEEP			HPDF_DATAIN2				TIMER41_MCH0					EXMC_SDCKE0	CMP0_OUT		EVENTOUT
PC6		TIMER0_BRKIN1	TIMER2_CH0	TIMER7_CH0	HPDF_CKIN3	I2S1_MCK		USART5_TX		EXMC_NWAIT						EVENTOUT
PC7		TIMER0_CH3	TIMER2_CH1	TIMER7_CH1	HPDF_DATAIN3		I2S2_MCK	USART5_RX		EXMC_NE0						EVENTOUT
PC8	TRACED1		TIMER2_CH2	TIMER7_CH2				USART5_CK	UART4_RTS/UART4_DE	EXMC_NE1	EXMC_INT					EVENTOUT
PC9	CK_OUT1	TIMER0_MCH3	TIMER2_CH3	TIMER7_CH3	I2C2_SDA	I2S_CKIN			UART4_CTS	OSPIM_P0_IO0						EVENTOUT
PC10		TIMER0_CH3		HPDF_CKIN5			SPI2_SCK/I2S2_CK	USART2_TX	UART3_TX	OSPIM_P0_IO1						EVENTOUT
PC11		TIMER0_ETI		HPDF_DATAIN5			SPI2_MISO	USART2_RX	UART3_RX	OSPIM_P0_CSN	EXMC_NBL2					EVENTOUT
PC12	TRACED3	EXMC_D6	TIMER14_CH0			SPI5_SCK/I2S5_CK	SPI2_MOSI/I2S2_SD	USART2_CK	UART4_TX							EVENTOUT
PC13																EVENTOUT
PC14																EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC15																EVENTOUT

Table 2-6. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0			TIMER7_CH2	HPDF_CKIN6					UART3_RX	CAN0_RX			EXMC_D2	TRIGSEL_IN3		EVENTOUT
PD1				HPDF_DATAIN6					UART3_TX	CAN0_TX			EXMC_D3	TRIGSEL_IN6		EVENTOUT
PD2	TRACED2	EXMC_D7	TIMER2_ETI		TIMER14_BRKIN0				UART4_RX							EVENTOUT
PD3				HPDF_CKOUT		SPI1_SCK/I2S1_CK		USART1_CTS					EXMC_CLK			EVENTOUT
PD4				TIMER7_MCH3				USART1_RTS/USART1_DE			OSPIM_P0_IO4		EXMC_NOE			EVENTOUT
PD5				TIMER7_CH3				USART1_TX			OSPIM_P0_IO5		EXMC_NWE			EVENTOUT
PD6				HPDF_CKIN4	HPDF_DATAIN1	SPI2_MOSI/I2S2_SD		USART1_RX			OSPIM_P0_IO6		EXMC_NWAIT			EVENTOUT
PD7				HPDF_DATAIN4		SPI0_MOSI/I2S0_SD	HPDF_CKIN1	USART1_CK			OSPIM_P0_IO7		EXMC_NE0/EXMC_NCE			EVENTOUT
PD8				HPDF_CKIN3				USART2_TX					EXMC_D13			EVENTOUT
PD9				HPDF_DATAIN3				USART2_RX					EXMC_D14			EVENTOUT
PD10				HPDF_CKOUT				USART2_CK					EXMC_D15			EVENTOUT
PD11	TIMER40_CH1			TIMER7_MCH3	I2C3_SMBA			USART2_CTS		OSPIM_P0_IO0			EXMC_A16/EXMC_CLE			EVENTOUT
PD12	TIMER41_CH1		TIMER3_CH0		I2C3_SCL	CAN2_RX	EDOUT_A	USART2_RTS/USART2_DE		OSPIM_P0_IO1			EXMC_A17/EXMC_ALE			EVENTOUT
PD13	TIMER42_CH1		TIMER3_CH1		I2C3_SDA	CAN2_TX	EDOUT_B			OSPIM_P0_IO3			EXMC_A18			EVENTOUT
PD14	TIMER43_CH1		TIMER3_CH2			SPI3_IO2	EDOUT_Z		UART7_CTS				EXMC_D0			EVENTOUT
PD15	TIMER44_CH1		TIMER3_CH3			SPI3_IO3			UART7_RTS/UART7				EXMC_D1			EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
									_DE							

Table 2-7. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0			TIMER3_ETI						UART7_RX				EXMC_NBL0			EVENTOUT
PE1									UART7_TX				EXMC_NBL1			EVENTOUT
PE2	TRACECK					SPI3_SCK				OSPIM_P0_IO2			EXMC_A23			EVENTOUT
PE3	TRACED0				TIMER14_BRKIN0								EXMC_A19			EVENTOUT
PE4	TRACED1	TIMER0_BRKIN1		HPDF_DATAIN3	TIMER14_MCH0	SPI3_NSS							EXMC_A20			EVENTOUT
PE5	TRACED2			HPDF_CKIN3	TIMER14_CH0	SPI3_MISO							EXMC_A21			EVENTOUT
PE6	TRACED3	TIMER0_BRKIN2			TIMER14_CH1	SPI3_MOSI						CMP_MUX_OUT3	EXMC_A22			EVENTOUT
PE7		TIMER0_ETI		HPDF_DATAIN2				UART6_RX			OSPIM_P0_IO4		EXMC_D4			EVENTOUT
PE8		TIMER0_MCH0		HPDF_CKIN2				UART6_TX			OSPIM_P0_IO5		EXMC_D5	CMP1_OUT		EVENTOUT
PE9		TIMER0_CH0		HPDF_CKOUT		SPI3_IO2		UART6_RTS/UART6_DE			OSPIM_P0_IO6		EXMC_D6			EVENTOUT
PE10		TIMER0_MCH1		HPDF_DATAIN4		SPI3_IO3		UART6_CTS			OSPIM_P0_IO7		EXMC_D7			EVENTOUT
PE11		TIMER0_CH1		HPDF_CKIN4		SPI3_NSS						OSPIM_P0_CSN	EXMC_D8			EVENTOUT
PE12		TIMER0_MCH2		HPDF_DATAIN5		SPI3_SCK							EXMC_D9	CMP0_OUT		EVENTOUT
PE13		TIMER0_CH2		HPDF_CKIN5		SPI3_MISO							EXMC_D10	CMP1_OUT		EVENTOUT
PE14		TIMER0_CH3				SPI3_MOSI							EXMC_D11			EVENTOUT
PE15		TIMER0_BRKIN0											EXMC_D12	CMP_MUX_OUT4		EVENTOUT

Table 2-8. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF5		TIMER0_MCH2,		TIMER7_MCH2	USART0_RX		HPDF_CKIN2		UART3_CTS				EXMC_A5	TRIGSEL_OUT5		EVENTOUT
PF6		TIMER15_CH0	CAN2_RX			SPI4_NSS		UART6_RX			OSPIM_P0_IO3		EXMC_D24	TIMER22_CH0		EVENTOUT
PF7		TIMER16_CH0	CAN2_TX			SPI4_SCK		UART6_TX			OSPIM_P0_IO2		EXMC_D25	TIMER22_CH1		EVENTOUT
PF8		TIMER15_MCH0				SPI4_MISO		UART6_RTS/UART6_DE			OSPIM_P0_IO0		EXMC_D26	TIMER22_CH2		EVENTOUT
PF9		TIMER16_MCH0				SPI4_MOSI		UART6_CTS			OSPIM_P0_IO1		EXMC_D27	TIMER22_CH3		EVENTOUT
PF10		TIMER15_BRKIN0								OSPIM_P0_SCK						EVENTOUT
PF11						SPI4_MOSI							EXMC_SDNRAS		TIMER23_CH0	EVENTOUT
PF12													EXMC_A6		TIMER23_CH1	EVENTOUT
PF13				HPDF_DATAIN6	I2C3_SMBA								EXMC_A7		TIMER23_CH2	EVENTOUT
PF14				HPDF_CKIN6	I2C3_SCL	SPI4_IO2							EXMC_A8		TIMER23_CH3	EVENTOUT
PF15					I2C3_SDA	SPI4_IO3							EXMC_A9			EVENTOUT

Table 2-9. Port G alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG6		TIMER16_BRKIN0									OSPIM_P0_CSN		EXMC_NE2			EVENTOUT
PG7		EXMC_D28						USART5_CK					EXMC_INT			EVENTOUT
PG8				TIMER7_ETI		SPI5_NSS/I2S5_WS		USART5_RTS/USART5_DE					EXMC_SDCLK			EVENTOUT
PG9		EXMC_D30	CAN2_TX	TIMER7_BRKIN1		SPI0_MISO		USART5_RX		OSPIM_P0_IO6			EXMC_NE1			EVENTOUT
PG13	TRACED0					SPI5_SCK/I2S5_CK		USART5_CTS	TIMER44_CH0				EXMC_A24	TIMER22_CH1		EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG14	TRACED1					SPI5_MOSI /I2S5_SD		USART5_ TX	TIMER44_ MCH0	OSPIM_P 0_IO7			EXMC_A2 5	TIMER22 _CH2		EVENTOUT
PG15								USART5_ CTS	TIMER44_ BRKIN0				EXMC_SD NCAS			EVENTOUT

Table 2-10. Port H alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0																EVENTOUT
PH1																EVENTOUT
PH2								TIMER40_C H0	USBHS1_U LPI_STP	OSPIM_P0 _IO4			EXMC_SD CKE0			EVENTOUT
PH3								TIMER40_ MCH0	USBHS1_U LPI_DIR	OSPIM_P0 _IO5			EXMC_SD NE0			EVENTOUT
PH4					I2C1_SCL			TIMER40_B RKIN0	USBHS1_U LPI_NXT		USBHS0_U LPI_NXT		EXMC_NB L3			EVENTOUT
PH5					I2C1_SDA	SPI4_NS S		TIMER41_C H0	USBHS1_U LPI_CK				EXMC_SD NWE			EVENTOUT
PH6					I2C1_SMB A	SPI4_SC K		TIMER41_ MCH0	USBHS1_U LPI_D0				EXMC_SD NE1			EVENTOUT
PH7				EDOUT_A	I2C2_SCL	SPI4_MI SO		TIMER41_B RKIN0	USBHS1_U LPI_D1				EXMC_SD CKE1			EVENTOUT
PH8			TIMER4_ ETI	EDOUT_B	I2C2_SDA	SPI4_IO2		TIMER42_C H0	USBHS1_U LPI_D2				EXMC_D16			EVENTOUT
PH9				EDOUT_Z	I2C2_SMB A	SPI4_IO3		TIMER42_ MCH0	USBHS1_U LPI_D3				EXMC_D17			EVENTOUT
PH10			TIMER4_ CH0		I2C3_SMB A			TIMER42_B RKIN0	USBHS1_U LPI_D4				EXMC_D18			EVENTOUT
PH11			TIMER4_ CH1		I2C3_SCL			TIMER43_C H0	USBHS1_U LPI_D5				EXMC_D19			EVENTOUT
PH12			TIMER4_ CH2		I2C3_SDA			TIMER43_ MCH0	USBHS1_U LPI_D6				EXMC_D20			EVENTOUT
PH13				TIMER7_M CH0				TIMER43_B RKIN0	UART3_TX	CAN0_TX			EXMC_D21			EVENTOUT

Table 2-11. BGA240 package ESC port alternate functions summary

Pin Name	OSPI +gpio	OSPI +MII(3 port downstream mode)	OSPI +MII(3 port upstream mode)
IO4	PDI_GPIO4	MII2_TX_EN	MII0_TX_EN
IO6	PDI_GPIO6	MII2_TXD1	MII0_TXD1
IO7	PDI_GPIO7	MII2_TXD2 / TX_SHIFT0	MII0_TXD2 / TX_SHIFT0
IO5	PDI_GPIO5	MII2_TXD0	MII0_TXD0
SYNC1_LATCH1	SYNC1 / LATCH1	SYNC1 / LATCH1	SYNC1 / LATCH1
IO8	PDI_GPIO8	MII2_TXD3 / TX_SHIFT1	MII0_TXD3 / TX_SHIFT1
IO16	MCU_PDITYPE	MCU_PDITYPE	MCU_PDITYPE
IO3	PDI_GPIO13	MII2_LINK	MII0_LINK
IO17	EFUSE_LDO_BYP	EFUSE_LDO_BYP	EFUSE_LDO_BYP
IO11	PDI_GPIO11	MII2_RX_DV	MII0_RX_DV
OE_EXT	MII_CLK25	MII_CLK25	MII_CLK25
IO18	PHYRST_MODE	PHYRST_MODE	PHYRST_MODE
IO12	PDI_GPIO12	MII2_RXD0	MII0_RXD0
IO13	PDI_GPIO13	MII2_RXD1	MII0_RXD1
IO15	PDI_GPIO15	MII2_RXD3	MII0_RXD3
LINKACTLED0	LINKACTLED0 / CHIP_MODE0	LINKACTLED0 / CHIP_MODE0	LINKACTLED0 / CHIP_MODE0
IO10	PDI_GPIO10	MII_LINKPOL/LINKACTLED2	MII_LINKPOL / LINKACTLED2
IO14	PDI_GPIO14	MII2_RXD2	MII0_RXD2
LINKACTLED1	LINKACTLED1 / CHIP_MODE1	LINKACTLED1 / CHIP_MODE1	LINKACTLED1 / CHIP_MODE1
EESIZE	EEPROM_SIZE / RUNLED	EEPROM_SIZE / RUNLED	EEPROM_SIZE / RUNLED
TESTMODE	TESTMODE	TESTMODE	TESTMODE
IO9	PDI_GPIO9	MII2_RX_ER	MII0_RX_ER
SYNC0_LATCH0	SYNC0 / LATCH0	SYNC0 / LATCH0	SYNC0 / LATCH0
IO1	PDI_GPIO1	MII_CLK	MII_CLK

Pin Name	OSPI +gpio	OSPI +MII(3 port downstream mode)	OSPI +MII(3 port upstream mode)
IO0	PDI_GPIO0	MII2_RX_CLK	MII0_RX_CLK
IO2	PDI_GPIO2	MII_DATA	MII_DATA
EESCL	EEPROM_CLK	EEPROM_CLK	EEPROM_CLK
EESDA	EEPROM_DATA	EEPROM_DATA	EEPROM_DATA
RSTN	RSTN	RSTN	RSTN
IRQ(1)	IRQ	IRQ	IRQ

(1) The PJ10 and IRQ have no external pins and are connected inside the chip

3. Functional description

3.1. Arm® Cortex®-M7 core

The Arm® Cortex®-M7 processor is a highly efficient high-performance, embedded processor that features low interrupt latency, low-cost debug, and has backwards compatibility with existing Cortex-M profile processors. The processor has an in-order super-scalar pipeline that means many instructions can be dual-issued, including load/load and load/store instruction pairs because of multiple memory interfaces. The Cortex-M7 is a high-performance processor, which features a 6-stage superscalar pipeline with branch prediction and an optional FPU capable of single-precision and optionally double-precision operations. The instruction and data buses have been enlarged to 64-bit wide over the previous 32-bit buses.

The interfaces that the processor supports include:

- 64-bit AXI4 interface.
- 32-bit AHB master interface.
- 32-bit AHB slave interface.
- 64-bit instruction TCM interface.
- 2x32-bit data TCM interfaces.

The processor contains the following external interfaces:

- AHBP interface.
- AHBS interface.
- AHBD interface.
- External Private Peripheral Bus.
- ATB interfaces.
- TCM interface.
- Cross Trigger interface.
- MBIST interface.
- AXIM interface.

32-bit Arm® Cortex®-M7 processor core

- Up to 600 MHz operation frequency.
- Single-cycle multiplication and hardware divider.
- Integrated DSP instructions.
- 24-bit SysTick timer.

The Cortex®-M7 processor is based on the ARMv7-M architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations, DSP and floating point instructions. Some system peripherals listed below are also provided by Cortex®-M7:

- Nested Vectored Interrupt Controller (NVIC).

- Flash Patch and Breakpoint (FPB).
- Data Watchpoint and Trace (DWT).
- Instrumentation Trace Macrocell (ITM).
- Embedded Trace Macrocell (ETM).
- JTAG or SWD Debug Port.
- Trace Port Interface Unit (TPIU).
- Memory Protection Unit (MPU).
- Floating Point Unit (FPU), double-precision.
- Load Store Unit (LSU).
- Data Processing Unit (DPU).
- Prefetch Unit (PFU).

3.2. On-chip memory

- Up to 3840KB of main flash memory for instruction and data.
- Up to 512 KB of configurable SRAM for ITCM/DTCM/AXI SRAM.
- Up to 512 KB of on-chip SRAM (AXI SRAM).
- 4KB of backup SRAM.
- RAM ECC monitor for each Region.

The GD32H75Exx has up to 3840KB of mian flash memory for instruction and data. The flash memory consists of 3840KB main flash organized into 960 sectors with 4KB and 64KB information block. Each sector can be erased individually.

The GD32H75Exx series contain up to 512KB of on-chip SRAM (AXI SRAM), 4KB of backup SRAM and up to 512KB RAM shared by ITCM/DTCM/AXI SRAM. All of AHB SRAM support byte, half-word (16 bits), and word (32 bits) accesses. The on-chip SRAM (AXI SRAM) support byte, half-word (16 bits), word (32 bits) and double words (64 bits) accesses. SRAM0 and SRAM1 can be accessed by almost all AHB masters. The backup SRAM (BKPSRAM) is implemented in the backup domain, which can keep its content even when the V_{DD} power supply is down.

Table 2-2. Memory map of GD32H75Exx devices shows the memory map of the GD32H75Exx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 64 MHz factory-trimmed RC and external 4 to 50 MHz crystal oscillator.
- Internal 48 MHz RC oscillator.
- Low power internal 4 MHz RC oscillator.
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- Integrated system clock PLL.
- 1.71 to 3.6V application supply and I/Os.
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage

detector (LVD).

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AXI, three AHB and four APB domains. The maximum frequency of the system clock can be up to 600 MHz. The maximum frequency of the three AHB domains are 300 MHz. The maximum frequency of the four APB domains including APB1 = APB3 = PAB4 is 150 MHz and APB2 is 300 MHz. See ***Figure 2-3. GD32H75Exx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components except for the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.53V and down to 1.48V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.71V to 3.6V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} range: 1.71V to 3.6V, external analog power supplies for ADC, reset blocks, RCs and PLL.
- V_{BAT} range: 1.71V to 3.6V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

GD32H75EXX supports four BOOT modes, including:

- USER BOOT
- SECURITY BOOT
- SYSTEM BOOT
- SRAM BOOT

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDR0/1 in Boot address, allowing to program any boot memory address from 0x0000 0000 to to 0x9000 0000.

The boot loader is located in non-user System memory. It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART1 (PA2 and PA3), USART2 (PB10 and PB11), USBHS0 (USBHS0_DP and USBHS0_DM) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating

modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt / event can wake up the system.
- **Deep-sleep mode**
  In deep-sleep mode, all clocks in the 0.9V domain are off, and all of LPIRC4M, IRC64M, HXTAL and PLLs are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC tamper and timestamp event, LXTAL clock stuck, the LVD \ LVD \ OVD, CMP output, LPDTS wakeup, RTC wakeup, CAN wakeup, I2C wakeup, USART0 wakeup and USBHS wakeup. When exiting the deep-sleep mode, the IRC64M is selected as the system clock.
- **Standby mode**
  In standby mode, the whole 0.9V domain is power off, the LDO is shut down, and all of LPIRC4M, IRC64M, HXTAL and PLLs are disabled. The contents of SRAM and registers in 0.9V power domain are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, WKUP pins and LCKMD.

3.6. Electronic fuse (EFUSE)

- One-time programmable nonvolatile 51ddres storage cells organized as 32*32 bits.
- Double-bit redundant backup mechanism.
- All bits in the 51ddres cannot be rollback from 1 to 0.
- Each bit in 51ddres macro can only be programmed once, and software must avoid reprogramming.
- Voltage range for program: 1.71~1.98 V.
- Voltage range for read: 0.72~1.05 V.

The Efuse controller has 51ddres macro that store system parameters. As a non-volatile unit of storage, the bit of 51ddres macro cannot be restored to 0 once it is programmed to 1.

3.7. Trigger selection controller (TRIGSEL)

- Supports different optional trigger inputs.
- Trigger input source could be external input signal or output of peripheral.
- Trigger selection output could be for external output or peripheral.

The trigger selection controller (TRIGSEL) allows software to select the trigger input signal for various peripherals. TRIGSEL provides a flexible mechanism for a peripheral to select different trigger inputs. It’s up to 3 trigger selection outputs could be selected for each peripheral. And every output could select from different trigger input signal.

3.8. General-purpose and alternate-function I/Os (GPIO and AFIO)

- GPIOs mappable on 16 external interrupt lines, each pin weak pull-up/pull-down function.
- Output push-pull/open drain enable control.
- Analog input/output configuration.
- Alternate function input/output configuration.

GD32H75Exx is up to 116 general purpose I/O pins (GPIO), named PA0~PA15, PB0~PB15, PC0~PC15, PD0~PD15, PE0~PE15, PF5~PF15, PG6~PG9, PG13~PG15, PH0~PH13, PA0_C, PA1_C, PC2_C, PC3_C for the device to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (Afs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog mode.

3.9. CRC calculation unit (CRC)

- Supports 7/8/16/32 bit data input.
- For 7(8)/16/32 bit input data length, the calculation cycles are 1/2/4 AHB clock cycles.
- User configurable polynomial value and size.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. The CRC calculation unit can be used to calculate 7/8/16/32 bit CRC code within user configurable polynomial.

3.10. True random number generator (TRNG)

- LFSR mode and NIST mode to generate random number (National Institute of Standards and Technology) mode to generate random number.
- About 40 periods of TRNG_CLK are needed between two consecutive random numbers in LFSR mode.
- 32-bit random numbers are generated each time in LFSR mode.
- TRNG NIST mode follows the NIST SP800-90B.
- Support health tests recommended by the NIST SP800-90B.
- 32-bit*4 or 32-bit*8 random numbers are generated each time in NIST mode.
- TRNG has the functions of startup and in-service self-check, associated with specific

error flags.

- 128-bit random value seed is generated from analog noise.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise and it has been pre-certified NIST SP800-90B.

3.11. Trigonometric Math Unit (TMU)

- 10 kinds of functions.
- The fixed point format is configurable.
- Programmable precision.
- CORDIC-algorithm core: circular system and hyperbolic system, rotation pattern and vectoring pattern.

The Trigonometric Math Unit (TMU) is a fully configurable block that execute common trigonometric and arithmetic operations. It can be used to calculate total 10 kinds of functions. The input/output data meet q1.31 or q1.15 fixed point format.

3.12. Direct memory access controller (DMA)

- Two AHB master interface for transferring data, and one AHB slave interface for programming DMA.
- 16 channels (8 for DMA0 and 8 for DMA1) and each channel are configurable.
- Support independent single, 4, 8, 16-beat incrementing burst memory and peripheral transfer.
- Support independent 8, 16, 32-bit memory and peripheral transfer.
- Peripherals supported: Timers, ADC, HPDF, SPI, I2C, USART, UART, DAC, I2S, FAC, TMU and CAN.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Two AHB master interfaces and eight four-word depth 32-bit width FIFOs are presented in each DMA controller, which achieves a high DMA transmission performance. There are 16 independent channels in the DMA controller (8 for DMA0 and 8 for DMA1). Each channel is assigned a specific or multiple target peripheral devices for memory access request management. Two arbiters respectively for memory and peripheral are implemented inside to handle the priority among DMA requests.

3.13. Master direct memory access controller (MDMA)

- 16 channels, each channel supports software triggering and requests can be selected

among any request source.

- Support independent single, 2, 4, 8, 16, 32, 64, 128-beat incrementing burst source and destination transfer.
- Support three transfer modes:
  - Read from memory and write to memory (software triggered).
  - Read from peripheral and write to memory (or memory mapped peripherals).
  - Read from memory (or memory mapped peripherals) and write to peripheral.
- Automatic pack / unpack of data to optimize bandwidth when the data width of the source and destination are different.
- 34 hardware trigger sources, all channels can be connected to any hardware trigger source.
- Two FIFOs of 16 double word depth to maximize data bandwidth and bus utilization.

The master direct memory access (MDMA) controller provides a hardware method of transferring data between peripherals and/or memory without intervention from the MCU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data. MDMA can be used in combination with a DMA controller (DMA0 or DMA1) to provide up to 16 channels. Each channel request can be selected among any request source. The built-in arbiter is used to handle priority among MDMA requests.

3.14. DMA request multiplexer (DMAMUX)

- 16 channels for DMAMUX request multiplexer.
- 8 channels for DMAMUX request generator.
- Support 35 trigger inputs and 29 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.15. Analog to digital converter (ADC)

- 14-bit ADC0 and ADC1 conversion rate is up to 4 MSPS.
- 12-bit ADC2 conversion rate is up to 5.3 MSPS.
- 14-bit,12-bit, 10-bit, 8-bit configurable resolution for ADC0 and ADC1.
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution for ADC2.
- In ADC0 and ADC1, Oversampling ratio arbitrarily adjustable from 2x to 1024X.
- ADC2, Oversampling ratio arbitrarily adjustable from 2x to 256X.
- ADC0 and ADC1 supply requirements: 1.8V to 3.6V, and typical power supply voltage is

3.3V, ADC2 supply requirements: 1.71V to 3.6V, typical power supply voltage is 3.3V.

- ADC input voltage range: $V_{REFN} \leq V_{IN} \leq V_{REFP}$.
- Temperature sensor.
- Start-of-conversion can be initiated by software or TRIGSEL.

A 12 / 14-bit successive approximation analog-to-digital converter module (ADC) is integrated on the MCU chip. ADC0 has 20 external channels, 1 internal channel (DAC_OUT0 channel), ADC1 has 18 external channels, 3 internal channels (the battery voltage, V_{REFINT} inputs channel and DAC_OUT1 channel), ADC2 has 17 external channels, 4 internal channels (the battery voltage, V_{REFINT} inputs channel, tempeture sensor and high-precision tempeture sensor). After sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit(LSB) alignment or the most significant(MSB) bit alignment (ADC0 / 1 are 32-bit data register, ADC2 is 16-bit data register). An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU.

3.16. Digital to analog converter (DAC)

- 8-bit or 12-bit resolution. Left or right data alignment.
- Conversion update synchronously.
- Conversion trigged by external triggers.
- Input voltage reference, V_{REFP}.
- Output buffer calibration.
- Using sample and keep mode to reduce the power consumption.
- Noise wave generation (LFSR noise mode and Triangle noise mode).
- Two DAC channels in concurrent mode.

The Digital-to-analog converter converts 12-bit digital data to a voltage on the external pins. The digital data can be set to 8-bit or 12-bit mode, left-aligned or right-aligned mode. DMA can be used to update the digital data on external triggers. The output voltage can be optionally buffered for higher drive capability, and DAC output buffer can be calibrated to improve output accuracy. The sample and keep mode can reduce the power consumption of DAC.

3.17. Real time clock (RTC) and backup registers

- Support calendar function, which can support year, month, date, day, hours, minutes, seconds and subseconds (date is the day of week and day is the day of month).
- Daylight saving compensation supported, which is realized through software.
- External high-accurate low frequency (50Hz or 60Hz) clock used to achieve higher calendar accuracy performed by reference clock detection option function.
- Atomic clock adjust (max adjust accuracy is 0.95PPM) for calendar calibration performed by digital calibration function.
- Sub-second adjustment by shift function.

The RTC provides a time which includes hour/minute/second/sub-second and a calendar includes year/month/day/week day. The time and calendar are expressed in BCD code except sub-second. Sub-second is expressed in binary code. Hour adjust for daylight saving time.

The RTC is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.18. Timers and PWM generation

- Two 16-bit Advanced timer (TIMER0 & TIMER7), two16-bit General-L0 timers (TIMER2, TIMER3), four 32-bit General-L0 timers (TIMER1, TIMER4, TIMER22, TIMER23), six 16-bit General-L3 timers (TIMER14, TIMER40, TIMER41, TIMER42, TIMER43, TIMER44), two16-bit General-L4 timers (TIMER15, TIMER16), two 32-bit Basic timer (TIMER5 & TIMER6) and two 64-bit Basic timer (TIMER50 & TIMER51).
- Up to 62 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match.
- Encoder interface controller with two inputs using quadrature decoder and non-quadrature decoder mode.
- 24-bit SysTick timer down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 8 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general level 0 timer, can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1/4/22/23 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2/3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The general level 0 timer also supports an encoder interface with two inputs using quadrature decoder mode and non-quadrature decoder mode.

The general level3 timer module (TIMER14/40/41/42/43/44) is a three-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level3 timer has a 16-bit counter that can be used as an unsigned counter.

The general level4 timer module (TIMER15/16) is a two-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level4 timer has a 16-bit counter that can be used as an unsigned counter.

The basic timer module(TIMER5/6/50/51) has a 32-bit or 64-bit counter that can be used as an unsigned counter. The basic timer can be configured to generate a DMA request and a TRGO0 to connect to DAC.

The GD32H75Exx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter.
- Auto reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source.

3.19. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Programmable baud-rate generator allowing speed up to 37.5 Mbits/s when the clock frequency is 300 MHz and oversampling is by 8.
- Supports both asynchronous and clocked synchronous serial communication modes.
- IrDA SIR encoder and decoder support.
- LIN break generation and detection.
- ISO 7816-3 compliant smart card interface.

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4, UART6, UART7) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for

the USART/UART transmitter and receiver.

3.20. Inter-integrated circuit (I2C)

- Up to four I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus).
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.
- SMBus 3.0 and PMBus 1.3 compatible.
- Wakeup from sleep mode and Deep-sleep mode on I2C address match.

The I2C (inter-integrated circuit) module provides an I2C interface which is an industry standard two-line serial interface for MCU to communicate with external I2C interface. I2C bus uses two serial lines: a serial data line, SDA, and a serial clock line, SCL. The I2C interface implements standard I2C protocol with standard mode (up to 100KHz), fast mode (up to 400KHz) and fast mode plus (up to 1MHz) as well as CRC calculation and checking, SMBus (system management bus), and PMBus (power management bus).

3.21. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex, half-duplex or simplex mode.
- Separate transmit and receive 32-bit FIFO.
- Data frame size can be 4 to 32 bits.
- Hardware CRC calculation, transmission and checking.
- SPI TI mode supported.
- Multi-master or multi-slave mode function.
- Protect configurations and settings.
- Adjustable main device receiver sampling time.
- Configurable FIFO thresholds (data packing).
- Quad-SPI configuration available in master mode (in SPI3 / 4).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI3 and SPI4.

3.22. Inter-IC sound (I2S)

- Master or slave operation for transmission/reception.
- Four I2S standards supported: Phillips, MSB justified, LSB justified and PCM standard.

- Data length can be 16 bits, 24 bits or 32 bits.
- Channel length can be 16 bits or 32 bits.
- Transmission and reception use a 32 bits wide buffer.
- Audio sample frequency can be 8 kHz to 192 kHz using I2S clock divider.
- Programmable idle state clock polarity.
- Separate transmit and receive 32-bit FIFO.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32H75Exx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequencies from 8 KHz to 192 KHz is supported.

3.23. OSPI I/O manager(OSPIM)

- Supports two OSPI (single-line, two-lines, four-lines, eight-lines) interfaces.
- Support two port for pin assignment.
- Fully programmable IO matrix, can assign pins according to function.

OSPIM supports OSPI pin assignment with full matrix.

3.24. Octal-SPI interface(OSPI)

- Three functional modes: indirect mode, status polling mode, memory-mapped mode.
- Support read in memory-mapped mode.
- Support single, dual, quad and octal communication.
- Fully programmable command format for both indirect and memory-mapped mode.
- Support SDR (signal data rate) and DTR (double transfer rate, only for GD25LX512ME).
- Integrated FIFO for transmission/reception.
- 8, 16 and 32-bits data access.

The OSPI is a specialized interface that communicate with external memories. The interface support single, dual, quad and octal SPI flash (PSRAMS, NAND, NOR Flash, etc).

3.25. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM, NOR-Flash, 8/16-bit NAND Flash and Synchronous DRAM(SDRAM).
- Embedded ECC hardware for NAND Flash access.
- Two SDRAM banks with independent configuration, up to 13-bits Row Address, 11-bits Column Address, 2-bits internal banks address.
- SDRAM Memory size: 4x16Mx32bit (256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB).

The external memory controller EXMC, is used as a translator for CPU to access a variety of

external memory, it automatically converts AXI memory access protocol into a specific memory access protocol defined in the configuration register, such as SRAM, ROM, NOR Flash, PSRAM, NAND Flash and SDRAM. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.26. EtherCAT SubDevice Controller(ESC)

- Port support: 2 internal phy port and 1 external MII.
- 8 Fieldbus Memory Management Units (FMMUs).
- 8KB DPRAM.
- Distributed clock 64-bit, support allows synchronization with other EtherCAT devices.
- 8 Syncmanager entities.
- DC synchronization less than 1us.

The EtherCAT SubDevice Controller (ESC), licensed from Beckhoff Automation, It takes care of the EtherCAT communication as an interface between the EtherCAT fieldbus and the sub application.

3.27. VREF

- Stable voltage, and product calibrated.
- Connects to VREFP pin to source off-chip circuits.
- 1.5V, 1.8V, 2.048V or 2.5V configurable reference voltage output.

A precision internal reference circuit is inside. The internal voltage reference unit is used to provide voltage reference for ADC / DAC, or used by off-chip circuit connecting to VREFP pin.

3.28. Low power digital temperature sensor (LPDTS)

- The trigger source of measurement can be set to software or hardware.
- Programmable sampling time.
- Temperature window watchdog.
- The interrupt can be generated when the temperature is below a low threshold or above a high threshold and at the end of measurement.
- The generation of asynchronous wakeup signal in LXTAL mode indicates that the measurement result is higher or lower than the specified threshold.

Low power digital tempearature sensor(LPDTS) is used to transmit square wave, which is converted by temperature and the frequency is proportional to the absolute temperature. The frequency measurement is based on the PCLK or the LXTAL clock.

3.29. Encoder Divided-Output controller (EDOUT)

- Support for changing the activation polarity of B.
- Support configuration of Z-phase output location and pulse width.
- Number of edges per rotation: 16 to 65536 (must be the multiple of four).
- Support for the input of update period event signals from the TRIGSEL.

The encoder divided-output controller (EDOUT) is used to output location information obtained from the encoder in the form of A-phase, B-phase, and Z-phase pulses.

3.30. Controller area network (CAN)

- Supports CAN protocol version 2.0A/B.
- Compliant with the ISO 11898-1:2015 standard.
- Supports CAN FD frame with up to 64 data bytes, baudrate up to 8 Mbit/s.
- Supports CAN classical frame with up to 8 data bytes, baudrate up to 1 Mbit/s.
- Supports time stamp based on 16-bit free running counter.
- Supports transmitter delay compensation for CAN FD frames at faster data rates.
- Maskable interrupts.
- Supports four communication mode: normal mode, Inactive mode, Loopback and silent mode, and Monitor mode.
- Supports two power saving modes: CAN_Deepsleep mode, and CAN_sleep mode.
- Support two wakeup methods for waking up from Pretended Networking mode: wakeup matching event, and wakup timeout event.
- Global network time, synchronized by a specific message.

CAN bus (Controller Area Network) is a bus standard designed to allow microcontrollers and devices to communicate with each other without a host computer. The CAN interface supports the CAN 2.0A/B protocol, ISO 11898-1:2015 and BOSCH CAN FD specification.

The CAN module is a CAN Protocol controller with a very flexible mailbox system for transmitting and receiving CAN frames. The mailbox system consists of a set of mailboxes that store configuration and control data, timestamp, message ID, and data. The space of up to 32 mailboxes can also be configured as Rx FIFO with ID filtering against up to 104 extended IDs or 208 standard IDs or 416 partial 8-bit IDs, and configure receive FIFO/mailbox private filter register for up to 32 ID filter table elements.

3.31. Comparator (CMP)

- Rail-to-rail comparators.
- Configurable hysteresis.
- Configurable speed and consumption.
- Each comparator has configurable analog input source.
- Outputs with blanking source.

- Outputs to I/O.
- Outputs to timers for capture.
- Outputs to EXTI and NVIC.

The general purpose comparators, CMP0 and CMP1, can work either standalone (all terminal are available on I/Os) or together with the timers. It could be used to wake up the MCU from low-power mode by an analog signal, provide a trigger source when an analog signal is in a certain condition, achieves some current control by working together with a PWM output of a timer and the DAC. It blanking function can be used for false overcurrent detection in motor control applications.

3.32. High-Performance Digital Filter (HPDF)

- 8 multiplex digital serial input channels.
  - configurable SPI and Manchester interfaces.
- 8 internal digital parallel input channels.
  - input with up to 16-bit resolution.
  - internal source: ADC data or memory (CPU/DMA write) data stream.
- Configurable Sinc filter and integrator.
  - the order and oversampling rate (decimation rate) of Sinc filter can be configured.
  - sampling rate of configurable integrator.
- Threshold monitor function.
  - independent Sinc filter, configurable order and oversampling rate (decimation rate).
  - configurable data input source: serial channel input data or HPDF output data.
- Malfunction monitor function.
  - A counter with 8 bits is used to monitor the continuous 0 or 1 in the serial channel input data stream.
- Extreme monitor function.
  - store minimum and maximum values of output data values of HPDF.
- Up to 24-bit output data resolution.
- Clock signal can be provided to external sigma delta modulator.
  - provide configurable clock signal by the CKOUT pin.
- HPDF output data is in signed format.

A high performance digital filter module (HPDF) for external sigma delta (Σ-Δ) modulator is integrated in GD32H75Exx. HPDF supports SPI interface and Manchester-coded single-wire interface. The external sigma delta modulator can be connected with MCU by the serial interface, and the serial data stream output by sigma delta modulator can be filtered. In addition, HPDF also supports the parallel data stream input, which can be selected from internal ADC peripherals or from MCU memory.

3.33. Filter arithmetic accelerator (FAC)

- Fixed or float multiplier and accumulator.

- 256 x 32-bit local memory.
- 16-bit fixed-point or 32-bit float point input and output.
- Up to three buffers, two input buffers and one output buffer.
- Buffer can be circular.
- FIR and IIR can be realized.
- Vector functions support convolution, Dot product, correlation functions.
- Data can be read and written through DMA.

The filter arithmetic accelerator unit consist of multiplier, accumulator and address generation logic, so as to index vector elements stored in local memory. Circular buffering is valid for both input and output, which allows to realize finite impulse response (FIR) filters and infinite impulse response (IIR) filters. The unit support CPU to be free from frequent or lengthy filtering operations, compared with software implementation, it can accelerate calculations and the processing speed of time critical tasks.

3.34. Universal serial bus high-speed interface (USBHS)

- Supports USB 2.0 Host mode at High-Speed(480Mb/s), Full-Speed(12Mb/s) or Low-Speed(1.5Mb/s).
- Supports USB 2.0 device mode at High-Speed(480Mb/s) or Full-Speed(12Mb/s).
- Supports OTG protocol with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol).
- An external PHY device connected to the ULPI is required when using in HS mode

USB High-Speed (USBHS) controller provides a USB-connection solution for portable devices. USBHS supports both host and device modes, as well as OTG mode with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol). USBHS contains an embedded USB PHY internal which can be configured as Full-Speed. USBHS supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system. For Full-Speed operation, battery charging detection (BCD), attach detection protocol (ADP), and link power management (LPM) are also supported.

3.35. Debug mode

- JTAG and SWD Debug Port.

The GD32H75Exx series provide a large variety of debug, trace and test features. They are implemented with a standard configuration of the Arm® CoreSight™ module together with a daisy chained standard TAP controller. Debug and trace functions are integrated into the ARM® Cortex®-M7. The debug system supports serial wire debug (SWD) and trace functions in addition to standard JTAG debug.

4. Electrical characteristics

To better understand this chapter, read the following before moving on to the rest of this chapter.

- A + or no sign before the current value indicates that the current is output from the MCU.
- A – before the current value indicates that the current is input to the MCU.
- T_A (Ambient temperature) tested condition.
- T_J (Junction temperature) tested condition.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from simulation of IC designers.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from random test.
- Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_J = 25 °C.
- The devices will be damaged or work abnormally if the electrical parameters beyond the range of maximum and minimum values.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
USB	Universal Serial Bus
SPI	Serial Peripheral Interface
RMII	Reduced Media Independent Interface

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings(1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} – 0.3	V_{SS} + 3.6	V

Symbol	Parameter	Min	Max	Unit
V_{DDA}	External analog supply voltage(3)	V_{SSA} – 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} – 0.3	V_{SS} + 3.6	V
$V_{DD50USB}$	$V_{DD50USB}$ supply voltage	V_{SS} – 0.3	V_{SS} + 5.6	V
V_{DD1Ax}	Analog 1.1V power for Ethernet PHY	V_{SS} – 0.3	V_{SS} + 1.21	V
$V_{OSCVDD11}$	Internal 1.1V oscillator of ESC supply voltage	V_{SS} – 0.3	V_{SS} + 1.21	V
V_{CORE}	Digital core supply voltage for ESC	V_{SS} – 0.3	V_{SS} + 1.21	V
V_{DD3Ax}	Analog 3.3V power for Ethernet PHY(2)	V_{SS} – 0.3	V_{SS} + 3.6	V
V_{DD33}	Supply voltage for the ESC internal regulators(2)	V_{SS} – 0.3	V_{SS} + 3.6	V
V_{DDIO}	IO of ESC supply voltage(2)	V_{SS} – 0.3	V_{SS} + 3.6	V
V_{OSCI}	oscillator of ESC supply voltage	V_{SS} – 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5VT I/O(4)	V_{SS} – 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} – 0.3	V_{DD} + 0.3	
$\|\Delta V_{DDX}\|$	Variations between different V_{DD} power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	25	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	—	120	
I_{DD}	Maximum current into each V_{DD} pin	—	120	
I_{SS}	Maximum current into each V_{SS} pin	—	120	
$I_{INJ(PIN)}$	Injected current on IO	—	0	
T_A(6)	Operating temperature range for grade 6 device(7)	-40	+85	°C
	Operating temperature range for grade 7 device(7)	-40	+105	
P_D	Power dissipation at T_A = 85°C of BGA240	—	TBD	mW
	Power dissipation at T_A = 105°C of BGA240	—	TBD	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

(4) The device junction temperature must be kept below maximum T_J. More information could be found in ***AN166 Design Guide for Thermal Characteristics of GD32H7xx series.***

(5) V_{IN} maximum value cannot exceed 5.5 V.

(6) If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.

(7) For grade 7 devices, the parameter of T_A = 105°C, For grade 3 device, the parameter of T_A = 125°C.

4.2. Recommended DC characteristics

Table 4-3. DC operating conditions

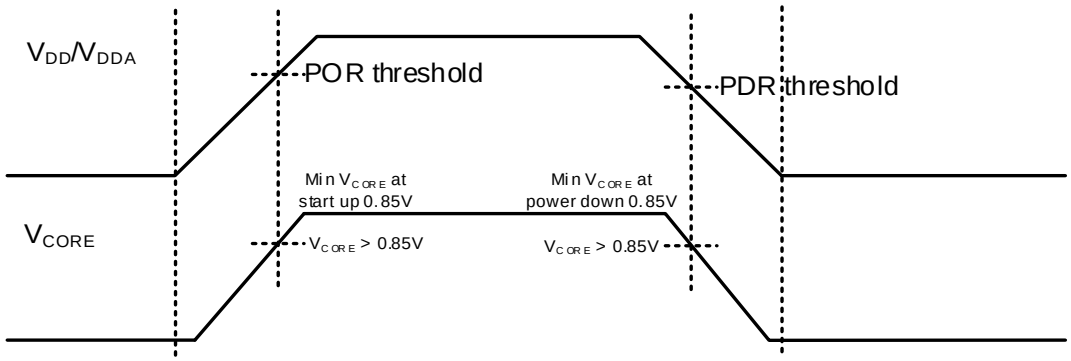
Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	1.71	3.3	3.6	V
V_{DDLDO}	Supply voltage for the internal regular	$V_{DDLDO} \leq V_{DD}$	1.71	—	3.6	V
V_{DDSMPS}	Supply voltage for the internal SMPS Step-down converter	$V_{DDSMPS} = V_{DD}$	1.71	—	3.6	V

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
$V_{DD50USB}$	—	USB regulator ON	4.0	5.0	5.5	V
		USB regulator OFF	—	$V_{DD33USB}$	—	V
$V_{DD33USB}$	Standard operating voltage, USB domain	USB used	3.0	—	3.6	V
		USB not used	0	—	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	1.71	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.71	—	3.6	V
V_{CAP}(2)	V_{CAP} supply voltage	Bypass mode	0.873	0.9	0.955	V

(1) Value guaranteed by characterization, not 100% tested in production.

(2) The power-up and power-down sequence for the power bypass mode should meet the requirements as illustrated in ***Figure 4-1. Bypass Mode Power-up and Power-down Timing Diagram*** **(1)(2)(3)**.

Figure 4-1. Bypass Mode Power-up and Power-down Timing Diagram (1)(2)(3)

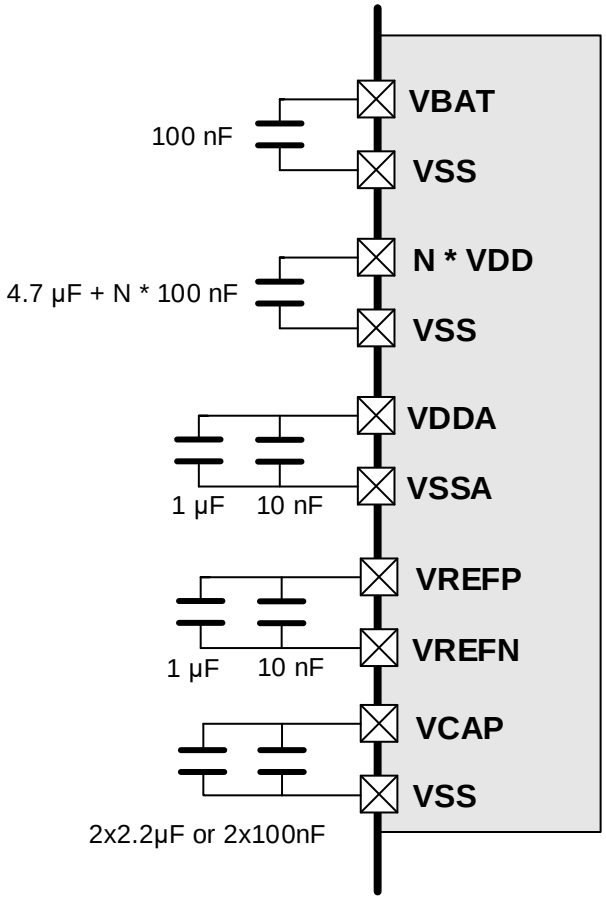


(1) Before the MCU's VDD/VDDA voltage rises to the POR (Power-On Reset) threshold, ensure that the VCAP voltage is greater than 0.85 V.

(2) Before the MCU's VDD/VDDA voltage drops to the PDR (Power-Down Reset) threshold, ensure that the VCAP voltage is greater than 0.85 V

(3) Under any operating condition, ensure that the VDD/VDDA voltage is greater than the VCAP voltage.

Figure 4-2. Recommended power supply decoupling capacitors(1)(2)(3)



(1) The VREFP and VREFN pins are only available on no less than 100-pin packages, or else the VREFP and VREFN pins are not available and internally connected to VDDA and VSSA pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

(3) When voltage regulator is enabled the two 2.2 µF Vcap capacitors are required , if bypassing the voltage regulator ,two 100 nF decoupling capacitors are required.

Table 4-4. Vcap operating conditions(1)(2)(3)

Symbol	Parameter	Conditions
C_{EXT}	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 100 mΩ

(1) When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

(2) This value corresponds to C_{EXT} typical value. A variation of +/-20% is tolerated.

(3) If a third V_{CAP} pin is available on the package, it must be connected to the other V_{CAP} pins but no additional capacitor is required.

Table 4-5. Clock frequency(1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	core clock frequency	Supply voltage < 3.6V	—	600	MHz
		Supply voltage < 2.3V	—	400	
f_{AHB}	AHB clock frequency	Supply voltage < 3.6V	—	300	
		Supply voltage < 2.3V	—	200	

f_{APB1}	APB1 clock frequency	—	—	150(2)	
f_{APB2}	APB2 clock frequency	—	—	300(2)	
f_{APB3}	APB3 clock frequency	—	—	150(2)	
f_{APB4}	APB4 clock frequency	—	—	150(2)	

(1) Value guaranteed by design, not 100% tested in production.

(2) APBx clocks are divided from AHB clock.

Table 4-6. TCM interface frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{TWW}	TCM without wait	—	—	350	MHz

(1) Value guaranteed by design, not 100% tested in production.

Table 4-7. Operating conditions at Power up / Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	μs/V
	V_{DD} fall time rate		100	∞	
t_{VDDA}	V_{DDA} rise time rate	—	0	∞	
	V_{DDA} fall time rate		100	∞	
$t_{VDD(USB)}$	$V_{DD(USB)}$ rise time rate	—	0	∞	
	$V_{DD(USB)}$ fall time rate		100	∞	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-8. Power saving mode wakeup timings characteristics(1)(2)

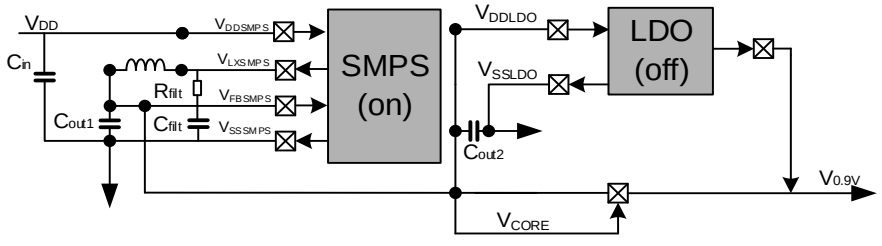
Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	408.6	ns
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode	5.1	μs
$t_{Standby}$	Wakeup from Standby mode	543.5	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC64M = System clock = 64 MHz, and SMPS supply ldo power mode is used.

4.3. SMPS step-down converter

Figure 4-3. External components for SMPS step-down converter



Direct SMPS supply

Table 4-9. Characteristics of SMPS step-down converter external components

Symbol	Parameter	Conditions

C_{in}	Capacitance of external capacitor on V_{DDSMPS}	4.7 µF
	ESR of external capacitor	100 mΩ
C_{filt}	Capacitance of external capacitor on V_{LXSMPS} pin	220 pF
R_{filt}	Resistor of external capacitor on V_{LXSMPS} pin	50 Ω
C_{OUT}	Capacitance of external capacitor on V_{FBSMPS} pin	10 µF
	ESR of external capacitor	20 mΩ
L	Inductance of external Inductor on V_{LXSMPS} pin	2.2 µH
	Serial DC resistor	150 mΩ
I_{SAT}	DC current at which the inductance drops 30% from its value without current	1.7 A
I_{RMS}	Average current for a 40 °C rise: rated current for which the temperature of the inductor is raised 40 °C by DC current	1.4 A

Table 4-10. SMPS step-down converter characteristics for external usage

Symbol	Conditions	Min	Typ	Max	Unit
V_{DDSMPS}(1)	V_{OUT} = 1.8 V	2.3	—	3.6	V
	V_{OUT} = 2.5 V	3	—	3.6	
V_{OUT}(2)	I_{out}=600 mA	—	1.8	—	V
		—	2.5	—	
I_{OUT}(3)	internal and external usage	—	—	600	mA
	External usage only	—	—	600	
$R_{DS(ON)}$(3)	—	—	110	—	mΩ
I_{DDSMPS_Q}(4)	Quiescent current	—	450	—	µA
T_{SMPS_START}(3)	V_{OUT} = 1.8 V/2.5 V	—	100	—	µS
I_{INRUSH}(3)	V_{OUT} = 0.9/1.8/2.5V, POR, Wake from Standby	—	850	—	mA

(1) The switching frequency is 2 MHz ± 10%
(2) Including line transient and load transient.
(3) Value guaranteed by characterization, not 100% tested in production.
(4) Value guaranteed by design, not 100% tested in production.

4.4. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications. The power consumption does not include systems EtherCAT SubDevice Controller (ESC) and EtherCAT PHY.

Table 4-11. Power consumption characteristics(1)(2)(3)(4)

Symbol	Parameter	Conditions	Min	Typ LDO regulator ON	Max	Unit
$I_{DD}+I_{DDA}$	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals enabled, code run in ITCM	—	161	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals enabled, code run in Flash and cache on	—	151	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals enabled, code run in Flash and cache off	—	151	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals disabled, code run in ITCM	—	47.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals disabled, code run in Flash and cache on	—	52.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals disabled, code run in Flash and cache off	—	52.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals enabled, code run in ITCM	—	110	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals enabled, code run in Flash and cache on	—	103	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals enabled, code run in Flash and cache off	—	103	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals disabled, code run in ITCM	—	36.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals disabled, code run in Flash and cache on	—	39.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals disabled, code run in Flash and cache off	—	39.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 64 MHz, All peripherals enabled, code run in ITCM	—	44.6	—	mA

Symbol	Parameter	Conditions	Min	Typ LDO regulator ON	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, System clock = 64 MHz, All peripherals enabled, code run in Flash and cache on	—	43.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 64 MHz, All peripherals disabled, code run in ITCM	—	20.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 64 MHz, All peripherals disabled, code run in Flash and cache on	—	20.5	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals enabled	—	151	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals disabled	—	49.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals enabled	—	104	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals disabled	—	37.5	—	mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO=0.6V, IRC32K off, RTC off, All GPIOs analog mode	—	4.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO=0.7V, IRC32K off, RTC off, All GPIOs analog mode	—	5.98	—	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO=0.8V, IRC32K off, RTC off, All GPIOs analog mode	—	7.97	—	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO=0.9V, IRC32K off, RTC off, All GPIOs analog mode	—	10.86	—	mA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, FWDGT off, Backup SRAM off, RTC and LXTAL off	—	15.6	—	µA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT off, Backup SRAM on, RTC and LXTAL off	—	91.3	—	µA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT off, Backup SRAM off, RTC and LXTAL on	—	16.3	—	µA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT off, Backup SRAM on, RTC and LXTAL on	—	91.9	—	µA

Symbol	Parameter	Conditions	Min	Typ LDO regulator ON	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, FWDGT on, Backup SRAM off, RTC and LXTAL off	—	15.8	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT on, Backup SRAM on, RTC and LXTAL off	—	91.5	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT on, Backup SRAM off, RTC and LXTAL on	—	16.6	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT on, Backup SRAM on, RTC and LXTAL on	—	92.2	—	μA
I_{BAT}	Battery supply current (Backup mode)	V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, Backup SRAM off, RTC and LXTAL off	—	3.9	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, Backup SRAM off, RTC and LXTAL off	—	1.1	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3 V, Backup SRAM off, RTC and LXTAL off	—	0.3	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, Backup SRAM on, RTC and LXTAL off	—	79.4	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, Backup SRAM on, RTC and LXTAL off	—	77.1	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3 V, Backup SRAM on, RTC and LXTAL off	—	76.3	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, Backup SRAM off, RTC and LXTAL on	—	3.9	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, Backup SRAM off, RTC and LXTAL on	—	1.1	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3 V, Backup SRAM off, RTC and LXTAL on	—	0.3	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, Backup SRAM on, RTC and LXTAL on	—	79.5	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, Backup SRAM on, RTC and LXTAL on	—	77.1	—	μA

Symbol	Parameter	Conditions	Min	Typ LDO regulator ON	Max	Unit
		V_{DD} off, V_{DDA} off, V_{BAT} = 3 V, Backup SRAM on, RTC and LXTAL on	—	76.2	—	μA

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Unless otherwise specified, all values given for T_J = 25 °C and test result is mean value.
(3) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTALor IRC32K are ON, an additional power consumption should be considered.
(4) During power consumption test, GPIO needs to be configure as Analog Input mode.

4.5. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-12. System level ESD and EFT characteristics(1)***. System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-12. System level ESD and EFT characteristics(1)

Symbol	Description	Conditions	Package	Class	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 3.3 V, T_J = 25 °C, f_{HCLK} = 600 MHz IEC 61000-4-2	BGA240	TBD	TBD
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_J = 25 °C, f_{HCLK} = 600 MHz IEC 61000-4-4	BGA240	TBD	TBD

(1) Value guaranteed by characterization, not 100% tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-13. EMI characteristics(1)***, The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-13. EMI characteristics(1)

Symbol	Parameter	Conditions	Package	Mode	Max vs. [f_{HXTAL}/f_{HCLK}] 8/600 MHz				Unit
					0.1-30MHz	30-130MHz	130MHz-1GHz	1-3GHz	
				SMPS supply	TBD	TBD	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing

in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-14. Component level ESD and latch-up characteristics(1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_J = 25 °C; JS-001-2017	BGA240	TBD	V	TBD
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_J = 25 °C; JS-002-2018	BGA240	TBD	V	TBD
LU	I-test	T_A = 125 °C, JESD78F	BGA240	TBD	mA	TBD
	V_{supply} over voltage			TBD	V	

(1) Value guaranteed by characterization, not 100% tested in production.

4.6. Power supply supervisor characteristics

Table 4-15. Power supply supervisor characteristics

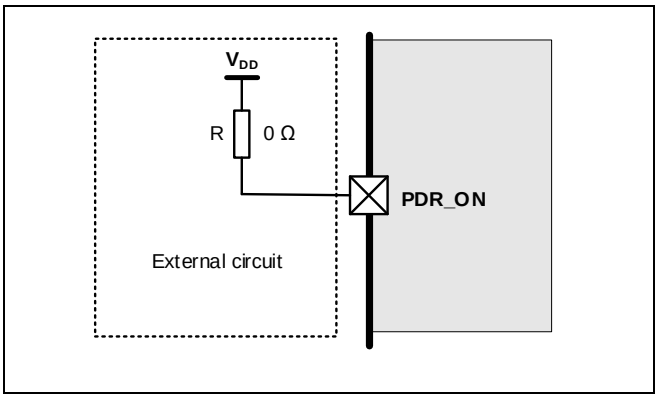
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low voltage Detector level selection	LVDT<2:0> = 000(rising edge)	—	1.95	—	V
		LVDT<2:0> = 000(falling edge)	—	1.85	—	
		LVDT<2:0> = 001(rising edge)	—	2.10	—	
		LVDT<2:0> = 001(falling edge)	—	2.00	—	
		LVDT<2:0> = 010(rising edge)	—	2.25	—	
		LVDT<2:0> = 010(falling edge)	—	2.15	—	
		LVDT<2:0> = 011(rising edge)	—	2.40	—	
		LVDT<2:0> = 011(falling edge)	—	2.30	—	
		LVDT<2:0> = 100(rising edge)	—	2.56	—	
		LVDT<2:0> = 100(falling edge)	—	2.46	—	
		LVDT<2:0> = 101(rising edge)	—	2.70	—	
		LVDT<2:0> = 101(falling edge)	—	2.60	—	
		LVDT<2:0> = 110(rising edge)	—	2.86	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		LVDT<2:0> = 110(falling edge)	—	2.75	—	
$V_{LVDhyst}$(2)	LVD hystersis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	1.53	—	V
V_{PDR}(1)	Power down reset threshold	—	—	1.48	—	V
$V_{PDRhyst}$(2)	PDR hysteresis	—	—	50	—	mV
V_{BOR3}(2)	Brownout level 3 threshold	Falling edge	—	2.6	—	V
		Rising edge	—	2.70	—	V
V_{BOR2}(2)	Brownout level 2 threshold	Falling edge	—	2.3	—	V
		Rising edge	—	2.4	—	V
V_{BOR1}(2)	Brownout level 1 threshold	Falling edge	—	2.0	—	V
		Rising edge	—	2.1	—	V
$V_{BORhyst}$(2)	BOR hysteresis	—	—	100	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization	—	—	520	—	µs
V_{AVD_0}(1)	Analog voltage detector for V_{DDA} threshold 0	Rising edge	—	1.70	—	V
		Falling edge	—	1.60	—	
V_{AVD_1}(1)	Analog voltage detector for V_{DDA} threshold 1	Rising edge	—	2.10	—	
		Falling edge	—	2.00	—	
V_{AVD_2}(1)	Analog voltage detector for V_{DDA} threshold 2	Rising edge	—	2.49	—	
		Falling edge	—	2.40	—	
V_{AVD_3}(1)	Analog voltage detector for V_{DDA} threshold 3	Rising edge	—	2.79	—	
		Falling edge	—	2.70	—	
V_{hyst_AVD}(2)	Hysteresis of V_{DDA} voltage detector	—	—	100	—	mV

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

Figure 4-4. Recommended PDR_ON pin circuit(1)



(1) PDR_ON pin should be pulled up to V_{DD}.

(2) The PDR_ON pin must be kept at high level. The user can flexibly adjust the value of the pull-up resistor R according to the specific scenario for a better performance.

4.7. Embedded USB regulator characteristics

Table 4-16. USB regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD50USB}$(1)	Supply voltage	—	4	5	5.5	V
$I_{DD50USB}$(2)	Current consumption	—	—	25	—	µA
$V_{REGOUT(V3.3V)}$ (1)	Regulated output voltage	—	3	—	3.6	V
I_{OUT}(2)	Output current load sinked by USB block	—	—	—	80	mA
T_{WKUP}(2)	V_{REGOUT} setting time	—	—	75	—	µs

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

4.8. Typical SMPS efficiency versus load current and temperature

Figure 4-5. Typical SMPS efficiency (%) vs load current(A) in Run mode at T_J = 25°C when V_{FBSMPS} = 0.9V

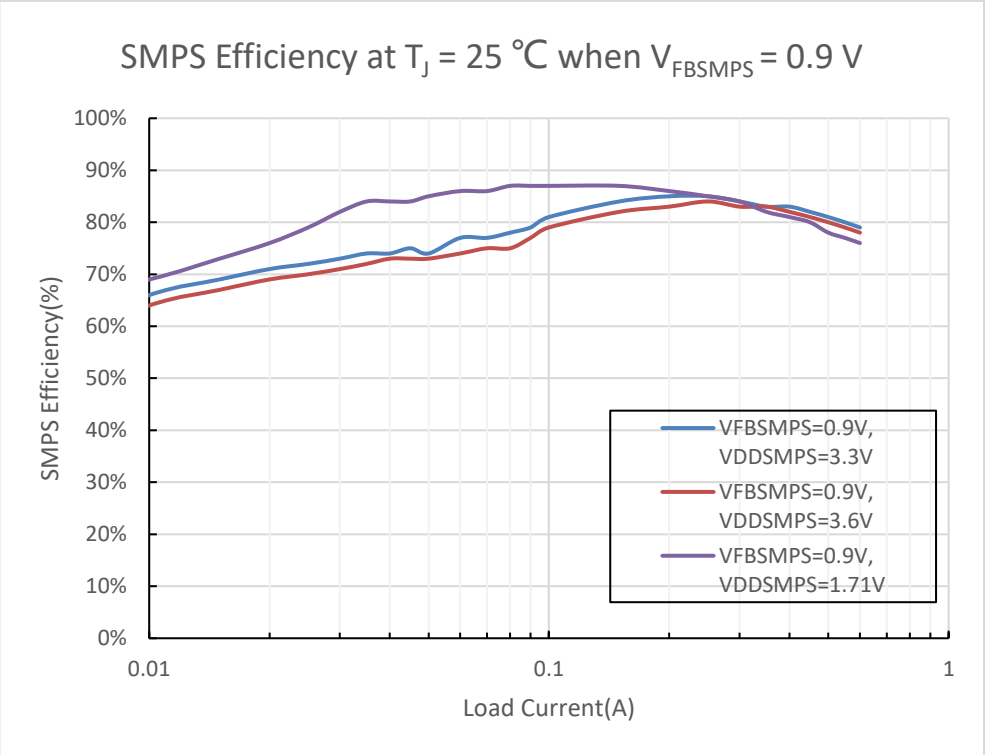


Figure 4-6. Typical SMPS efficiency (%) vs load current(A) in Run mode at T_J = -40 °C

when V_{FBSMPS} = 0.9V

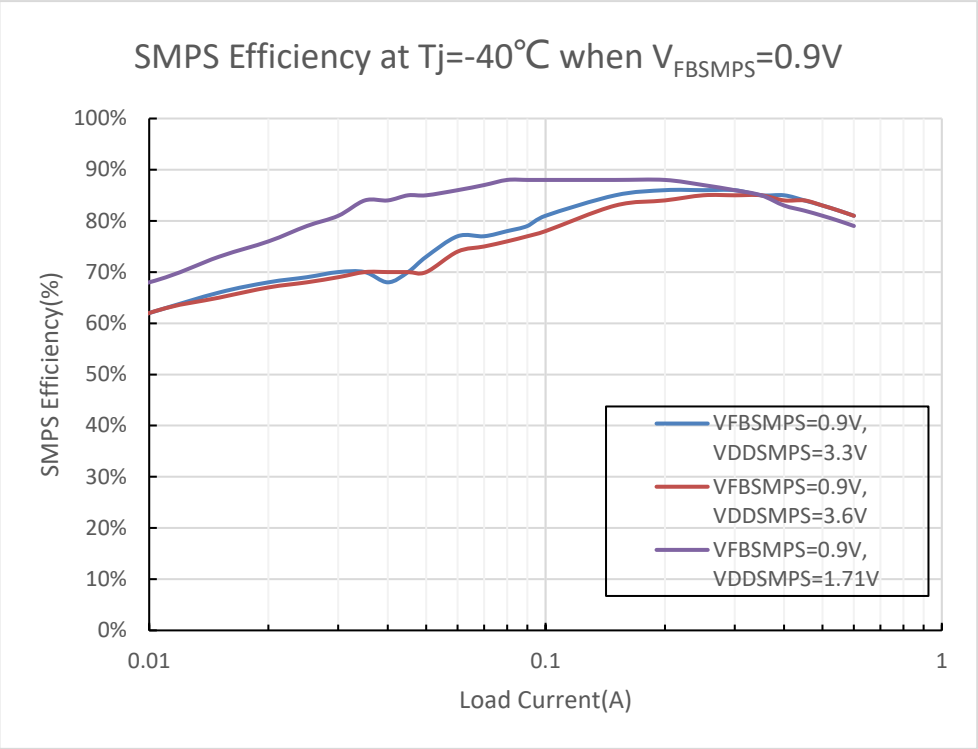
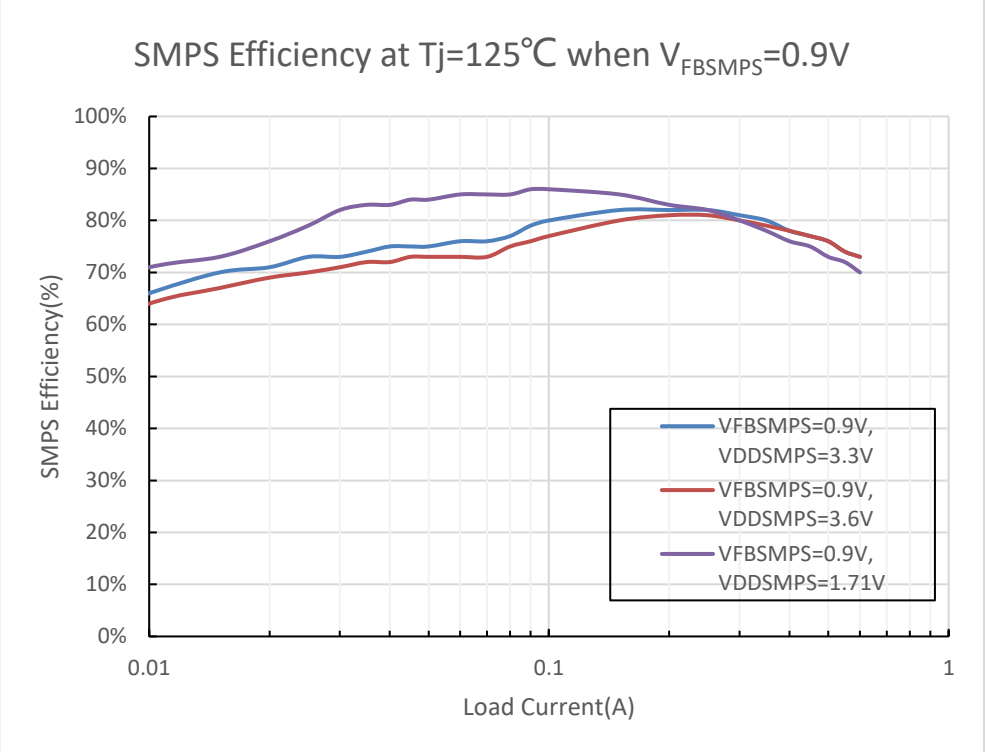


Figure 4-7. Typical SMPS efficiency (%) vs load current(A) in Run mode at T_J = 125 °C when V_{FBSMPS} = 0.9 V



4.9. External clock characteristics

Table 4-17. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	1.71 V ≤ V_{DD} ≤ 3.6 V	4	25	50	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2) (3)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Duty_{HXTAL}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(2)	Oscillator transconductance	Startup	—	27	—	mA/V
$I_{DD(HXTAL)}$ (1)	Crystal or ceramic operating current	HXTAL = 25 MHz	—	0.58	—	mA
$t_{ST(HXTAL)}$(1)	Crystal or ceramic startup time	HXTAL = 25 MHz	—	334	—	us

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

(3) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-18. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	1.71 V ≤ V_{DD} ≤ 3.6 V	1	—	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$(2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$(2)	OSCIN rise or fall time	—	—	—	10	ns
$Duty_{HXTAL}$(2)	Duty cycle	—	40	—	60	%

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

Table 4-19. Low speed external clock (LXTAL) generated from a crystal/ceramic

characteristics(5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	—	—	32.768	—	kHz
C_{LXTAL}(2) (3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	15	—	pF
$Duty_{LXTAL}$(2)	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(2)	Oscillator transconductance	LXTALDRI[1:0] = 00	—	4.88	—	μA/V
		LXTALDRI[1:0] = 01	—	7.32	—	
		LXTALDRI[1:0] = 10	—	14.61	—	
		LXTALDRI[1:0] = 11	—	21.94	—	
$I_{DD(LXTAL)}$(1)	Crystal or ceramic operating current	LXTALDRI[1:0] = 00	—	480	—	nA
		LXTALDRI[1:0] = 01	—	590	—	
		LXTALDRI[1:0] = 10	—	900	—	
		LXTALDRI[1:0] = 11	—	1210	—	
$t_{ST(LXTAL)}$(1)(4)	Crystal or ceramic startup time	LXTALDRI[1:0] = 00	—	453.9	—	ms
		LXTALDRI[1:0] = 01	—	322.7	—	
		LXTALDRI[1:0] = 10	—	220.4	—	
		LXTALDRI[1:0] = 11	—	192.4	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4) $t_{ST(LXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is set. This value varies significantly with the crystal manufacturer.

(5) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-20. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	—	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$ (2)	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$ (2)	OSC32IN rise or fall time	—	—	—	50	
$Duty_{LXTAL}$	Duty cycle	—	30	50	70	%

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

Figure 4-8. Recommended external OSCIN and OSCOUT pins circuit for crystal

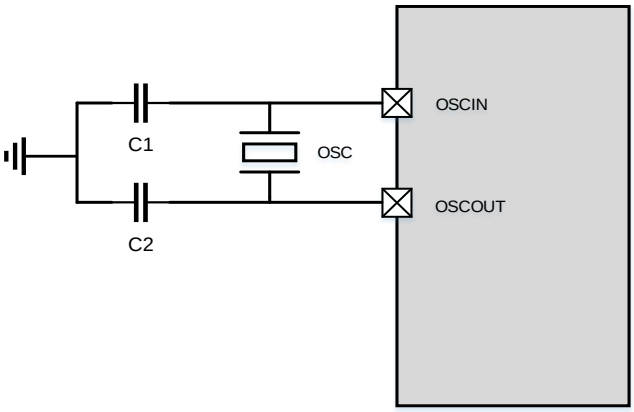
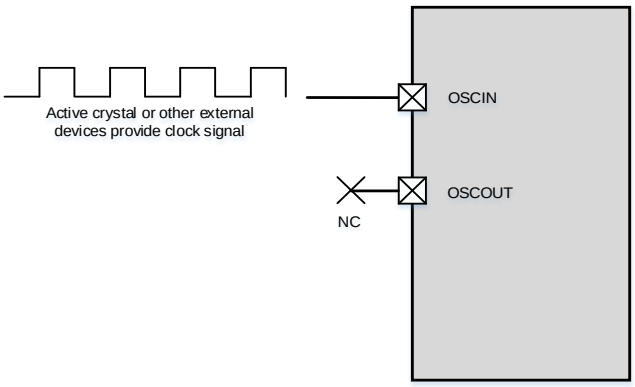


Figure 4-9. Recommended external OSCIN and OSCOUT pins circuit for oscillator



4.10. Internal clock characteristics

Table 4-21. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = 3.3 V	—	48	—	MHz
$Drift_{IRC48M}$	IRC48M oscillator Frequency Drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_J = -40 °C ~ +85 °C for grade 6 devices (1)	—	-0.64 ~ +0.55	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_J = 25 °C	47.5	—	48.5	MHz
	IRC48M oscillator Frequency accuracy, User trimming step(1)	—	—	0.7	—	%
$Duty_{IRC48M}$(2)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC48M)}$(1)	IRC48M oscillator operating current	—	—	330	—	μA
$t_{ST(IRC48M)}$(1)	IRC48M oscillator startup time	—	—	2.85	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

Table 4-22. High speed internal clock (IRC64M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC64M}	High Speed Internal Oscillator (IRC64M) frequency	V_{DD} = 3.3 V	—	64	—	MHz
$Drift_{IRC64M}$	IRC64M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_J = -40 °C ~ +85 °C for grade 6 devices (1)	—	-0.19 ~ +0.85	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_J = 25 °C	63.68	—	64.32	MHz
	IRC64M oscillator Frequency accuracy, User trimming step(1)	—	—	0.23	—	%
$Duty_{IRC64M}$(2)	IRC64M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC64M)}$(1)	IRC64M oscillator operating current	—	—	500	—	μA
$t_{ST(IRC64M)}$(1)	IRC64M oscillator startup time	—	—	1.95	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

Table 4-23. Low power internal clock (LPIRC4M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LPIRC4M}$	High Speed Internal Oscillator (LPIRC4M) frequency	V_{DD} = 3.3 V	—	4	—	MHz
$ACC_{LPIRC4M}$	LPIRC4M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_J = -40 °C ~ +85 °C for grade 6 devices (1)	—	-0.96~ +1.02	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_J = 25 °C	3.96	—	4.04	MHz
	LPIRC4M oscillator Frequency accuracy, User trimming step(1)	—	—	0.4	—	%
$D_{LPIRC4M}$(2)	LPIRC4M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDALPIRC4M}$(1)	LPIRC4M oscillator operating current	—	—	30	—	μA
$t_{SULPIRC4M}$(1)	LPIRC4M oscillator startup time	—	—	1.64	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-24. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}(1)	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_J = -40 °C ~ +85 °C	20	32(1)	40	kHz
$t_{SUIRC32K}$(2)	IRC32K oscillator startup time	—	—	50.72	—	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

4.11. PLL characteristics

Table 4-25. PLL0/1/2 characteristics (wide VCO frequency range)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	2	—	16	MHz
	PLL input clock duty cycle	—	10	—	90	%
f_{VCO}(1)	PLL VCO output clock frequency	—	100	—	850	MHz
t_{LOCK}(2)	PLL lock time	—	—	200	500	μs
I_{DD}(2)	Current consumption on V_{DD}	VCO freq = 800 MHz	—	1.5	—	mA
		VCO freq = 100 MHz	—	0.3	—	
$Jitter_{PLL}$(2)	Cycle to cycle Jitter(rms)	f_{PLL_OUT} = f_{VCO_OUT} = 100	—	100	—	ps

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		f_{VCO_OUT}/10	MHz				
			f_{VCO_OUT} = 400 MHz	—	19	—	
			f_{VCO_OUT} = 800 MHz	—	16	—	
	Period jitter(rms)		f_{VCO_OUT} = 100 MHz	—	80	—	
			f_{VCO_OUT} = 400 MHz	—	12	—	
			f_{VCO_OUT} = 800 MHz	—	10	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-26. PLL0/1/2 characteristics (narrow VCO frequency range)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—		1	—	2	MHz
	PLL input clock duty cycle	—		10	—	90	%
f_{VCO}(1)	PLL VCO output clock frequency	—		100	—	500	MHz
t_{LOCK}(2)	PLL lock time	—		—	200	500	μs
I_{PLL}(2)	Current consumption on V_{DD}	VCO freq = 500 MHz		—	1.2	—	mA
$Jitter_{PLL}$(2)	Cycle to cycle Jitter(rms)	f_{PLL_OUT} = f_{VCO_OUT}/10	f_{VCO_OUT} = 500 MHz	—	16	—	±ps
			f_{VCO_OUT} = 500 MHz	—	10	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-27. PLLUSBHS0/1 characteristics(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	4	—	30	MHz
f_{PLLOUT}(1)	PLL output clock frequency	—	—	480	—	MHz
f_{VCO}(1)	PLL VCO output clock frequency	—	—	480	—	MHz
t_{LOCK}(1)	PLL lock time	—	—	100	150	μs
I_{DDA}(2)	Current consumption on V_{DDA}	—	—	1.7	—	mA
$Jitter_{PLL}$	Cycle to cycle Jitter(rms)	System clock	—	40	—	ps
	Cycle to cycle Jitter（peak to peak）		—	400	—	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

(3) Value given with main PLL running.

4.12. Memory characteristics

Table 4-28. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(2)	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	—	100	—	—	kcycles
t_{RET}	Data retention time	—	—	20	—	years
t_{PROG}	Word programming time	T_A = -40°C ~ +105 °C	—	1	—	ms
$t_{ERASE4kB}$	Sector(4kB) erase time	T_A = -40°C ~ +105 °C	—	100	—	ms
$t_{MERASE(1MB)}$	Mass erase time	T_A = -40°C ~ +105 °C	—	8	—	s
$t_{MERASE(2MB)}$	Mass erase time	T_A = -40°C ~ +105 °C	—	16	—	s
$t_{MERASE(3840kB)}$	Mass erase time	T_A = -40°C ~ +105 °C	—	30	—	s

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

4.13. NRST pin characteristics

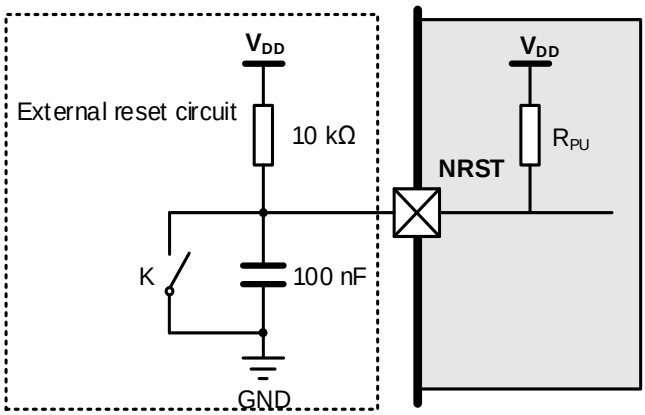
Table 4-29. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(2)	NRST Input low level voltage	V_{DD} = V_{DDA} = 1.71 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(2)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	300	—	mV
$V_{IL(NRST)}$(2)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(2)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	310	—	mV
$V_{IL(NRST)}$(2)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.6 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(2)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	320	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

Figure 4-10. Recommended external NRST pin circuit



4.14. GPIO characteristics

Table 4-30. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	1.71 V<V_{DD}<3.6 V	—	—	0.3V_{DD}	V
V_{IH}(1)	I/O input high level voltage	1.71 V<V_{DD}<3.6 V	0.7V_{DD}	—	—	V
V_{HYS}(1)	input hysteresis	V_{DD} =3.3 V	—	360	—	mV
I_{leak}	Input leakage current	0< V_{IN} ≤ V_{DD}	—	—	±2	μA
R_{PU}(1)	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	—	40	—	kΩ
R_{PD}(1)	Weak pull-down equivalent resistor	V_{IN} = V_{DD}	—	40	—	kΩ

(1) Value guaranteed by design, not 100% tested in production.

Table 4-31. Output voltage characteristics for all I/Os except PC13, PC14, PC15(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL} (IO_speed=max)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	0.094	—	V
		V_{DD} = 3.3 V	—	0.058	—	
		V_{DD} = 3.6 V	—	0.057	—	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	0.253	—	
		V_{DD} = 3.3 V	—	0.15	—	
		V_{DD} = 3.6 V	—	0.147	—	
V_{OH} (IO_speed=max)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	1.6	—	
		V_{DD} = 3.3 V	—	3.226	—	
		V_{DD} = 3.6 V	—	3.529	—	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	1.423	—	
		V_{DD} = 3.3 V	—	3.114	—	
		V_{DD} = 3.6 V	—	3.416	—	
V_{OL} (IO_speed=85MHz)	Low level output voltage for an IO Pin	V_{DD} = 1.71 V	—	0.139	—	V
		V_{DD} = 3.3 V	—	0.083	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	(I_{IO} = +8 mA)	V_{DD} = 3.6 V	—	0.08	—	
	Low level output	V_{DD} = 1.71 V	—	0.404	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	0.209	—	
	(I_{IO} = +20 mA)	V_{DD} = 3.6 V	—	0.204	—	
	High level output	V_{DD} = 1.71 V	—	1.547	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	3.197	—	
V_{OH}	(I_{IO} = +8 mA)	V_{DD} = 3.6 V	—	3.5	—	
(IO_speed=85MHz)	High level output	V_{DD} = 1.71 V	—	1.254	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	3.037	—	
	(I_{IO} = +20 mA)	V_{DD} = 3.6 V	—	3.342	—	
	Low level output	V_{DD} = 1.71 V	—	0.162	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	0.092	—	
V_{OL}	(I_{IO} = +8 mA)	V_{DD} = 3.6 V	—	0.091	—	
(IO_speed=60MHz)	Low level output	V_{DD} = 1.71 V	—	0.359	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	0.188	—	
	(I_{IO} = +16 mA)	V_{DD} = 3.6 V	—	0.184	—	V
	High level output	V_{DD} = 1.71 V	—	1.523	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	3.181	—	
V_{OH}	(I_{IO} = +8 mA)	V_{DD} = 3.6 V	—	3.484	—	
(IO_speed=60MHz)	High level output	V_{DD} = 1.71 V	—	1.298	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	3.060	—	
	(I_{IO} = +16 mA)	V_{DD} = 3.6 V	—	3.367	—	
	Low level output	V_{DD} = 1.71 V	—	0.052	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	0.029	—	
V_{OL}	(I_{IO} = +1 mA)	V_{DD} = 3.6 V	—	0.028	—	
(IO_speed=12MHz)	Low level output	V_{DD} = 1.71 V	—	0.235	—	V
	voltage for an IO Pin	V_{DD} = 3.3 V	—	0.119	—	
	(I_{IO} = +4 mA)	V_{DD} = 3.6 V	—	0.116	—	
	High level output	V_{DD} = 1.71 V	—	1.647	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	3.26	—	
V_{OH}	(I_{IO} = +1 mA)	V_{DD} = 3.6 V	—	3.562	—	
(IO_speed=12MHz)	High level output	V_{DD} = 1.71 V	—	1.437	—	
	voltage for an IO Pin	V_{DD} = 3.3 V	—	3.142	—	
	(I_{IO} = +4 mA)	V_{DD} = 3.6 V	—	3.451	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current.

Table 4-32. Output timing characteristics (IOSPDOP OFF) (1)(3)(4)

Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	tr/tf(2)	Output high to low level fall time and output low to high level rise time	2.5 V ≤ VDD ≤ 3.6 V, C_L = 50 pF	—	7.66	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	17.38	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 30 pF	—	3.98	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	13.72	—	

Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 10 pF	—	2.79	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	9.33	—	
01	tr/tf(2)	Output high to low level fall time and output low to high level rise time	2.5 V ≤ VDD ≤ 3.6 V, C_L = 50 pF	—	3.6	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	4.5	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 30 pF	—	2.6	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	3.38	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 10 pF	—	1.64	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	2.43	—	
10	tr/tf(2)	Output high to low level fall time and output low to high level rise time	2.5 V ≤ VDD ≤ 3.6 V, C_L = 50 pF	—	3.3	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	3.5	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 30 pF	—	2.5	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.6	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 10 pF	—	1.5	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	1.7	—	
11	tr/tf(2)	Output high to low level fall time and output low to high level rise time	2.5 V ≤ VDD ≤ 3.6 V, C_L = 50 pF	—	3.3	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	3.5	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 30 pF	—	2.5	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.6	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 10 pF	—	1.5	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	1.7	—	

(1) The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3 T Skew ≤ 1/20 T 45% < Duty cycle < 55%

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by characterization, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

Table 4-33. Output timing characteristics (IOSPDOP ON) (3)(4)

Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	16.5	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	11.1	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	8.1	—	
01	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	4	—	n
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.9	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	2	—	
10	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	3.8	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.8	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	1.8	—	
11	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	3.5	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.6	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	1.6	—	

(1) The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3 T Skew ≤ 1/20 T 45% < Duty cycle < 55%

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by characterization, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

4.15. 14-bit ADC characteristics

Table 4-34. 14-bit ADC characteristics

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—				1.8	—	3.6	V
V_{REFP}(2)(3)	Positive Reference Voltage	V_{DDA} ≥ 2.4 V				2.4	—	V_{DDA}	V
		V_{DDA} < 2.4 V				1.8	—	V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage	—				V_{SSA}			V
f_{ADC}(1)	ADC clock	2.7 V ≤ V_{DDA} ≤ 3.6 V 2.7 V ≤ V_{REFP} ≤ V_{DDA}				0.1	—	72	MHz
		2.4 V ≤ V_{DDA} ≤ 2.7 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}				0.1	—	54	MHz
		1.8 V ≤ V_{DDA} ≤ 2.4 V 1.8 V ≤ V_{REFP} ≤ V_{DDA}				0.1	—	36	MHz
f_S(1)	Sampling rate	Resolution = 14 bits	2.7 V ≤ V_{DDA} ≤ 3.6 V 2.7 V ≤ V_{REFP} ≤V_{DDA}	f_{ADC} = 72 MHz	SMP = 3.5	—	—	4	MSPS
			2.4 V ≤ V_{DDA} ≤ 2.7 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 54 MHz	SMP = 3.5	—	—	3	
			1.8 V ≤ V_{DDA} ≤ 2.4 V 1.8 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 36 MHz	SMP = 3.5	—	—	2	
		Resolution = 12 bits	2.7 V ≤ V_{DDA} ≤ 3.6 V 2.7 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 72 MHz	SMP = 3.5	—	—	4.5	
			2.4 V ≤ V_{DDA} ≤ 2.7 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 54 MHz	SMP = 3.5	—	—	3.37	
			1.8 V ≤ V_{DDA} ≤ 2.4 V 1.8 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 36 MHz	SMP = 3.5	—	—	2.25	
		Resolution = 10 bits	2.7 V ≤ V_{DDA} ≤ 3.6 V 2.7 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 72 MHz	SMP = 3.5	—	—	5.14	
			2.4 V ≤ V_{DDA} ≤ 2.7 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 54 MHz	SMP = 3.5	—	—	3.85	
			1.8 V ≤ V_{DDA} ≤ 2.4 V 1.8 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 36 MHz	SMP = 3.5	—	—	2.57	

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
		Resolution = 8 bits	2.7 V ≤ V_{DDA} ≤ 3.6 V 2.7 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 72 MHz	SMP = 3.5	—	—	6	
			2.4 V ≤ V_{DDA} ≤ 2.7 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 54 MHz	SMP = 3.5	—	—	4.5	
			1.8 V ≤ V_{DDA} ≤ 2.4 V 1.8 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 36 MHz	SMP = 3.5	—	—	3	
t_{TRIG}(1)	External trigger period	Resolution = 14 bits				—	—	18	1/f_{ADC}
V_{AIN}(1)	Conversion voltage range	—				0	—	V_{REFP}	V
V_{CMIV}(1)	Common mode input voltage	—				V_{REFP}/2-10%	V_{REFP}/2	V_{REFP}/2+10%	V
R_{AIN}(1)	External input impedance	Resolution = 14 bits				—	—	84.4	kΩ
		Resolution = 12 bits				—	—	96.5	
		Resolution = 10 bits				—	—	112	
		Resolution = 8 bits				—	—	135	
R_{ADC}(1)	Internal resistance					—	150	—	Ω
C_{ADC}(1)	Input sampling capacitance	—				—	12	—	pF
t_{STAB}	ADC Power-up time	—				1	—	—	μs
t_{CAL}(1)	Offset and linearity calibration time	—				TBD			1/f_{ADC}
t_{OFF_CAL}(1)	Offset calibration time	—				TBD			1/f_{ADC}
t_s(1)	Sampling time	—				3.5	—	810.5	1/f_{ADC}
t_{CONV}(1)	Total conversion time (including sampling time)	Resolution = N bits				N+4	—	—	1/ f_{ADC}

(1) Value guaranteed by design, not 100% tested in production.

(2) Depending on the package, V_{REFP} can be internally connected to V_{DDA} and V_{REFN} to V_{SSA}.

(3) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Equation 1: R_{AIN} max formula $$R_{AIN} < \frac{T_S}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above ***Equation 1*** is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 14 (from 14-bit resolution).

Table 4-35. ADC R_{AIN} max for f_{ADC} = 72 MHz (14-bit ADC) (1)(2)

Resolution	Sampling cycles @ 72 MHz	R_{AIN} max (kΩ)
14 bits	3.5	0.21

Resolution	Sampling cycles @ 72 MHz	R_{AIN} max (kΩ)
	6.5	0.52
	12.5	1.15
	24.5	2.40
	47.5	4.80
	92.5	9.50
	247.5	25.6
	810.5	84.4
12 bits	3.5	0.26
	6.5	0.62
	12.5	1.34
	24.5	2.77
	47.5	5.51
	92.5	10.8
	247.5	29.3
	810.5	96.5
10 bits	3.5	0.33
	6.5	0.75
	12.5	1.58
	24.5	3.25
	47.5	6.45
	92.5	12.7
	247.5	34.2
	810.5	112
8 bits	3.5	0.43
	6.5	0.93
	12.5	1.93
	24.5	3.94
	47.5	7.78
	92.5	15.2
	247.5	41.1
	810.5	135

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-36. 14-bit ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Max	Unit
EO	Offset error	Single ended	±1	—	LSB
		Differential	±2	—	
DNL	Differential linearity error	Single ended	-1/+2	—	
		Differential	-1/+2	—	
INL	Integral linearity error	Single ended	±2	—	

Symbol	Parameter	Test conditions	Typ	Max	Unit
		Differential	±2	—	
ENOB	Effective number of bits	Single ended	12.7	—	Bits
		Differential	13.3	—	
SNDR	Signal-to-noise and distortion ratio	Single ended	78.6	—	dB
		Differential	82	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Test condition: VDD=VDDA=VREFP=3.3V,ADC_CLK=25MHz, CALMOD=1, external VREF and mode 6 power supply were adopted.

(3) To obtain better ADC performance, especially when in SMPS power supply mode, please refer to the application note ***AN180 User guide of 14-bit ADC in GD32H7xx Series.***

4.16. 12-bit ADC characteristics

Table 4-37. 12-bit ADC characteristics

Symbol	Parameter	Conditions					Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—					1.71	—	3.6	V
V_{REFP}(2)(3)	Positive Reference Voltage	$V_{DDA} \geq V_{REFP}$					1.71	—	V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage	—					V_{SSA}			V
f_{ADC}(1)	ADC clock	1.71 V ≤ V_{DDA} ≤ 3.6 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}					0.1	—	80	MHz
		1.71 V ≤ V_{DDA} ≤ 2.4 V 1.71 V ≤ V_{REFP} ≤ V_{DDA}					0.1	—	60	MHz
f_S(1)	—	Resolution = 12 bits	2.4 V ≤ V_{DDA} ≤ 3.6 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	–40 °C ≤ T_J ≤ 125 °C	f_{ADC} = 80 MHz	SMP = 2.5	—	—	5.3	MSPS
			1.71 V ≤ V_{DDA} ≤ 2.4 V 1.71 V ≤ V_{REFP} ≤ V_{DDA}		f_{ADC} = 60 MHz		—	—	4	
		Resolution = 10 bits	2.4 V≤V_{DDA}≤3.6 V 2.4	–40 °C ≤ T_J ≤ 125 °C	f_{ADC} = 80 MHz	SMP = 2.5	—	—	6.1	

Symbol	Parameter	Conditions					Min	Typ	Max	Unit
			$V \le V_{REFP} \le V_{DDA}$							
			1.71 V ≤ V_{DDA} ≤ 2.4 V 1.71 V ≤ V_{REFP} ≤ V_{DDA}		f_{ADC} = 60 MHz		—	—	4.6	
		Resolution = 8 bits	2.4 V ≤ V_{DDA} ≤ 3.6 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	–40 °C ≤ T_J ≤ 125 °C	f_{ADC} = 80 MHz	SMP = 2.5	—	—	7.2	
			1.71 V ≤ V_{DDA} ≤ 2.4 V 1.71 V ≤ V_{REFP} ≤ V_{DDA}		f_{ADC} = 60 MHz		—	—	5.4	
		Resolution = 6 bits	2.4 V ≤ V_{DDA} ≤ 3.6 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	–40 °C ≤ T_J ≤ 125 °C	f_{ADC} = 80 MHz	SMP = 2.5	—	—	8.8	
			1.71 V ≤ V_{DDA} ≤ 2.4 V 1.71 V ≤ V_{REFP} ≤ V_{DDA}		f_{ADC} = 60 MHz		—	—	6.6	
t_{TRIG}(1)	External trigger period	Resolution = 12 bits					—	—	15	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	—					0	—	V_{REFP}	V
V_{CMIV}	Common mode input voltage	—					V_{REFP}/2-10%	V_{REFP}/2	V_{REFP}/2-10%	
R_{AIN}	External input	Resolution = 12 bits					—	—	109	kΩ
		Resolution = 10 bits					—	—	128	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	impedance	Resolution = 8 bits	—	—	153	
		Resolution = 6 bits	—	—	192	
R_{ADC}	Internal resistance	—	—	250	—	Ω
C_{ADC}	Input capacitance	—	—	7.5	—	pF
t_{STAB}	ADC Power-up time	—	-	1	—	μs
t_{OFF_CAL}	Offset calibration time	—	46	—	—	$1/f_{ADC}$
t_s	Sampling time	—	2.5	—	640.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits	3+N	—	—	$1/f_{ADC}$

(1) Value guaranteed by design, not 100% tested in production.

(2) Depending on the package, V_{REFP} can be internally connected to V_{DDA} and V_{REFN} to V_{SSA}.

(3) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Table 4-38. ADC R_{AIN} max for f_{ADC} = 80 MHz (12-bit ADC) (1)(2)

Resolution	Sampling cycles @ 80 MHz	R_{AIN} max (kΩ)
12 bits	2.5	0.17
	6.5	0.86
	12.5	1.89
	24.5	3.95
	47.5	7.90
	92.5	15.6
	247.5	42.2
	640.5	109
10 bits	2.5	0.25
	6.5	1.05
	12.5	2.25
	24.5	4.65
	47.5	9.26
	92.5	18.2
	247.5	49.3

Resolution	Sampling cycles @ 80 MHz	R_{AIN} max (kΩ)
	640.5	128
8 bits	2.5	0.35
	6.5	1.31
	12.5	2.75
	24.5	5.64
	47.5	11.1
	92.5	21.9
	247.5	59.2
	640.5	153
6 bits	2.5	0.50
	6.5	1.70
	12.5	3.50
	24.5	7.11
	47.5	14.0
	92.5	27.5
	247.5	74.1
	640.5	192

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-39. ADC dynamic accuracy at f_{ADC} = 60 MHz V_{REFP} = 1.8 V(1)(2)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 60 MHz V_{REFP} = 1.8 V Input Frequency = 20 kHz	Single ended	—	10.9	—	bits
			Differential	—	11.4	—	
SNDR	Signal-to-noise and distortion ratio		Single ended	—	67.5	—	dB
			Differential	—	70.7	—	
SNR	Signal-to-noise ratio		Single ended	—	67.6	—	
			Differential	—	70.8	—	
THD	Total harmonic distortion		Single ended	—	-83.1	—	
			Differential	—	-86.6	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) The test was carried out under the LDO power supply mode.

Table 4-40. ADC dynamic accuracy at f_{ADC} = 80 MHz V_{REFP} = 2.4 V(1)(2)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 80 MHz V_{REFP} = 2.4 V Input Frequency = 20 kHz	Single ended	—	11.1	—	bits
			Differential	—	11.6	—	
SNDR	Signal-to-noise and distortion ratio		Single ended	—	68.7	—	dB
			Differential	—	71.6	—	
SNR	Signal-to-noise ratio		Single ended	—	68.8	—	
			Differential	—	71.7	—	
THD	Total harmonic		Single ended	—	-83.6	—	

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
	distortion		Differential	—	-86.8	—	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) The test was carried out under the LDO power supply mode.

Table 4-41. ADC dynamic accuracy at f_{ADC} = 80 MHz V_{REFP} = 3.3 V(1)(2)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 80 MHz V_{REFP} = 3.3 V Input Frequency = 20 kHz	Single ended	—	11.1	—	bits
			Differential	—	11.5	—	
SNDR	Signal-to-noise and distortion ratio		Single ended	—	68.5	—	dB
			Differential	—	71.5	—	
SNR	Signal-to-noise ratio		Single ended	—	68.6	—	
			Differential	—	71.6	—	
THD	Total harmonic distortion		Single ended	—	-83.3	—	
			Differential	—	-85.9	—	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) The test was carried out under the LDO power supply mode.

Table 4-42. ADC static accuracy at f_{ADC} = 60 MHz V_{REFP} = 1.8 V(1)(2)

Symbol	Parameter	Test conditions		Typ	Max	Unit
EO	Offset error	f_{ADC} = 60 MHz V_{REFP} = 1.8 V Input Frequency = 1 kHz	Single ended	±1.5	—	LSB
			Differential	±0.5	—	
DNL	Differential linearity error		Single ended	+1.1 / -1	—	
			Differential	±0.9	—	
INL	Integral linearity error		Single ended	±0.8	—	
			Differential	±1	—	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) The test was carried out under the LDO power supply mode.

Table 4-43. ADC static accuracy at f_{ADC} = 80 MHz V_{REFP} = 2.4 V(1)(2)

Symbol	Parameter	Test conditions		Typ	Max	Unit
EO	Offset error	f_{ADC} = 80 MHz V_{REFP} = 2.4 V Input Frequency = 1 kHz	Single ended	±1	—	LSB
			Differential	±0.5	—	
DNL	Differential linearity error		Single ended	±0.7	—	
			Differential	±0.5	—	
INL	Integral linearity error		Single ended	±1.2	—	
			Differential	±1.2	—	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) The test was carried out under the LDO power supply mode.

Table 4-44. ADC static accuracy at f_{ADC} = 80 MHz V_{REFP} = 3.3 V(1)(2)

Symbol	Parameter	Test conditions		Typ	Max	Unit
EO	Offset error	f_{ADC} = 80 MHz V_{REFP} = 3.3 V Input Frequency = 1 kHz	Single ended	±1	—	LSB
			Differential	±0.5	—	
DNL	Differential linearity error		Single ended	±0.5	—	
			Differential	±0.5	—	
INL	Integral linearity error		Single ended	±1.5	—	

			Differential	±0.9	—	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) The test was carried out under the LDO power supply mode.

4.17. High-precision temperature sensor characteristics

Table 4-45. High-precision temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{25}(1)	Uncalibrated Offset	T_J = 25°C	—	1005.62	—	mV
E_{OFF}(1)	Uncalibrated Offset Error	T_J = 25°C	—	1.5	—	mV
Avg_Slope(1)	Average slope	—	—	3.3	—	mV/°C
E_M(1)	Slope Error	—	—	30	—	μV/°C
LIN(2)	Linearity	T_J = -40 °C to 125 °C	—	1.5	—	°C
t_{s_temp}	ADC sampling time when reading the temperature	—	10	—	—	μs
t_{ON}(1)	Turn-on Time	f_{ADC} = 5 MHz, t_{s_temp} = 10 μs	—	37.8	—	μs
ETOT(1)(3)(4)(5)	Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset	T_J = -40 °C to 125 °C	—	-2~4	—	°C

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) The error is the average result of 100 times and represents the temperature error of chip junction at the location where it is placed on die. The chip self-heating shall be considered when testing ambient temperature.
(4) The error caused by ADC conversion and provided temperature calculation formula is not included.
(5) Note: ADC2 clock should not be configured greater than 5MHz and the sampling time should greater than ts_temp when use the high precision temperature sensor by ADC conversion.

Table 4-46. High-precision temperature sensor calibration values

Symbol	Parameter	Memory address
HPTS_CAL	High-precision temperature sensor raw data acquired value at 25°C,V_{REFP} = 3.3 V	0x1FF0F7C4

4.18. Temperature sensor characteristics

Table 4-47. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±3.5	—	°C
Avg_Slope	Average slope	—	1.84	—	mV/°C
V_{25}	Voltage at T_J = 25 °C	—	0.66	—	V
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	17.1	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

Table 4-48. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 25 °C,V_{REFP} = 3.3V	0x1FF0F7C0
TS_CAL2	Temperature sensor raw data acquired value at -40 °C,V_{REFP} = 3.3V	0x1FF0F7C2

4.19. Low power digital temperature sensor characteristics

Table 4-49. Low power digital temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(2)	Supply voltage	—	1.71	3.3	3.6	V
f_{DTS}(1)	Output Clock frequency	—	626	798	1030	kHz
T_{LC}(1)	Temperature linearity coefficient	—	1307	2340	2744	Hz/°C
$T_{TOTAL(ERROR)}$(1)	Temperature offset measurement	T_J = -40 °C to 25 °C	-6.4	—	2.4	°C
		T_J = 25 °C to $T_J$max	-10.6	—	1.3	
t_{WAKE_UP}(2)	Wake-up time from off state until DTS ready bit is set	—	—	352	—	μs
I_{LPDTS}(1)	LPDTS consumption	—	—	26	—	μA

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

4.20. Voltage reference buffer characteristics

Table 4-50. Voltage reference buffer characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Supply voltage	Normal mode, V_{DDA} = 3.3V	VREFS = 00	2.8	3.3	3.6	V
			VREFS = 01	2.4	—	3.6	
			VREFS = 10	2.1	—	3.6	
			VREFS = 11	1.8	—	3.6	
		Degraded mode	VREFS = 00	1.71	—	2.8	
			VREFS = 01	1.71	—	2.4	
			VREFS = 10	1.71	—	2.1	
			VREFS = 11	1.71	—	1.8	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode, at 3.3 V, -40 ~ 85 °C(2)	VREFS = 00	2.493	2.5	2.507	
			VREFS = 01	2.052	2.0585	2.065	
			VREFS = 10	1.801	1.8072	1.814	
			VREFS = 11	1.502	1.5065	1.512	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		Degraded mode	VREFS = 00	V_{DDA}-50mV	—	V_{DDA}	
			VREFS = 01	V_{DDA}-50mV	—	V_{DDA}	
			VREFS = 10	V_{DDA}-50mV	—	V_{DDA}	
			VREFS = 11	V_{DDA}-210mV	—	V_{DDA}	
TRIM	Trim step resolution	—		—	0.14	0.152	%
C_L	Load capacitor	—		0.5	1	1.5	µF
ESR	Equivalent Serial Resistor of CL	—		—	—	2	Ω
I_{LOAD}	Load current	—		—	—	4	mA
t_{START}	Start-up time	C_L = 0.5 µF	—	—	546	—	µs
		C_L = 1 µF	—	—	546	—	
		C_L = 1.5 µF	—	—	546	—	
I_{DDA} (V_{REFBUF})	V_{REFBUF} consumption from V_{DDA}	I_{LOAD} = 0 µA	—	—	75.4	88.4	µA
		I_{LOAD} = 500 µA	—	—	75.7	88.8	
		I_{LOAD} = 4 mA	—	—	75.8	89.1	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase	—		—	11	—	mA
$Regu_{(LINE)}$	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	—	236	—	ppm /V
			I_{load} = 4 mA	—	264	—	
$Regu_{(LOAD)}$	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal mode	—	66	—	ppm / mA
T_{COEFF}	Temperature drift	−40 °C < T_J < +125 °C		—	—	$T_{COEFF(VREFINT)}$ +30	ppm / °C
PSRR	Power supply rejection	DC	—	—	65	—	dB
		100 kHz	—	—	35	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

4.21. CMP characteristics

Table 4-51. CMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	1.71	3.3	3.6	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Input voltage range	—		0	—	V_{DDA}	V
V_{SC}	Scaler offset voltage	—		—	3.5	11	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		—	200	226	µA
		BRG_EN=1 (bridge enable)		—	800	942	
t_{START_SCALER}	Scaler startup time	—		—	—	120	µs
t_D(2)	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		—	612	1217	ns
		Medium power mode		—	102	165	ns
		High speed power mode		—	32.4	54	ns
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	Ultra-low power mode		—	930	1650	ns
		Medium power mode		—	127	178	ns
		High speed power mode		—	35.4	58	ns
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode		—	—	1.4	µs
		Medium mode		—	—	2.1	
		Ultra-low-power mode		—	—	11.6	
$I_{DDA(CMP)}$	Current consumption from V_{DDA}	Ultra-low power mode	Static	—	419	434	nA
			With 50 kHz ±100 mV overdrive square signal	—	1890	—	
		Medium power mode	Static	—	4.25	4.30	µA
			With 50 kHz ±100 mV overdrive square signal	—	3.95	—	
		High speed power mode	Static	—	45.4	46.2	
			With 50 kHz ±100 mV overdrive square signal	—	40.5	—	
V_{offset}	Offset error	—		—	4	18	mV
V_{hyst}	Hysteresis Voltage	No Hysteresis		—	0	—	mV
		Low Hysteresis		7	10	17	
		Medium Hysteresis		15	20	34	
		High Hysteresis		23	30	52	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

4.22. Temperature and V_{BAT} monitoring

Table 4-52. VBAT monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit

R	Resistor bridge for V_{BAT}	—	25	—	kΩ
Q	Ratio on V_{BAT} measurement	—	4	—	—
Er	Error on Q	-10	—	+10	%
$t_{SAMPLE(VBAT)}$	ADC sampling time when reading V_{BAT} input	10	—	—	μs
$V_{BAT(high)}$	High supply monitoring	—	3.56	—	V
$V_{BAT(low)}$	Low supply monitoring	—	1.36	—	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-53. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VCRSEL = 0	—	5	—	kΩ
		VCRSEL = 1	—	1.5	—	

Table 4-54. Temperature monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	—	120	—	°C
$TEMP_{low}$	Low temperature monitoring	—	-27	—	

(1) Value guaranteed by design, not 100% tested in production.

4.23. DAC characteristics

Table 4-55. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—		1.8	3.3	3.6	V
V_{REFP}	Positive Reference Voltage	—		1.8	—	V_{DDA}	V
V_{REFN}	Negative Reference Voltage	—		—	V_{SSA}	—	V
R_{LOAD}(1)	Resistive load	Resistive load with buffer ON	connected to V_{SSA}	5	—	—	kΩ
			connected to V_{DDA}	5	—	—	
Ro(1)	Impedance output	Impedance output with buffer OFF		—	—	15	kΩ
R_{BON}(1)	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON		—	—	1.5	kΩ
R_{BOFF}(1)	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF		—	—	1.5	
C_{LOAD}(1)	Capacitive load	DAC output buffer ON		—	—	50	pF
C_{SH}(1)		Sample and Hold mode		—	0.1	1	μF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	—	V_{DDA}-0.2	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		DAC output buffer OFF		0	—	V_{DDA}-1LSB	V
$t_{SETTLING}$(1)	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5 LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode, DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ	±1 LSB	—	1.06	—	µs
			±2 LSB	—	0.38	—	
			±4 LSB	—	0.33	—	
			±8 LSB	—	0.30	—	
		Normal mode, DAC output buffer OFF, ±1LSB CL = 10 pF		—	1.95	2.5	
t_{WAKEUP}(1)	Wakeup time from off state (setting the Enx bit in the DAC Control register) until the final value of ±1 LSB is reached	Normal mode, DAC output buffer ON, CL ≤ 50 pF, RL = 5 kΩ		—	5	10	µs
		Normal mode, DAC output buffer OFF, CL ≤ 10 pF		—	2	5	
PSRR	Power supply rejection ratio(to V_{DDA})	No R_{Load}, C_{LOAD} = 50 pF		50	70	—	dB
t_{SAMP}(1)	Sampling time in Sample and Hold mode C_L = 100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1 LSB final value)	MODE<2:0>_V12 = 100 / 101 (BUFFER ON)		—	0.8	1.1	ms
		MODE<2:0>_V12 = 110 (BUFFER OFF)		—	9.20	10.5	
		MODE<2:0>_V12 = 111 (INTERNAL BUFFER OFF)		—	1.75	2.30	µs
C_{lint}	Internal sample and hold capacitor	—		5.5	7	8.5	pF
t_{TRIM}	Middle code offset trim time	Minimum time to verify the each code		100	—	—	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REFP} = 3.6 V		—	870	—	µV
		V_{REFP} = 1.8 V		—	435	—	
I_{DDA}(1)(2)	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	—	330	—	µA
			No load, worst code (0xF1C)	—	330	—	
		DAC output buffer OFF	No load, middle/ worst code (0x800)	—	1	—	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		Sample and Hold mode, C_{SH} = 100 nF		—	330*T_{ON}/(T_{ON}+T_{OFF})	—	
$I_{DDVREFP}$(1)	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	—	100	—	μA
			No load, worst code (0xF1C)	—	300	—	
		DAC output buffer OFF	No load, middle code (0x800)	—	85	—	
		Sample and Hold mode, Buffer ON, C_{SH} = 100 nF (middle code)		—	100*T_{ON}/(T_{ON}+T_{OFF})	—	
		Sample and Hold mode, Buffer OFF, C_{SH} = 100 nF (middle code)		—	85*T_{ON}/(T_{ON}+T_{OFF})	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) T_{ON} is the refresh phase duration, while T_{OFF} is the hold phase duration. Refer to the product reference manual for more details.

Table 4-56. DAC accuracy

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
DNL(2)	Differential non linearity	DAC output buffer ON		—	—	±2	LSB
		DAC output buffer OFF		—	—	±2	
INL(2)	Integral non linearity	DAC output buffer ON		—	—	±4	LSB
		DAC output buffer OFF		—	—	±4	
Offset(1)	Offset error at code 0x800	DAC output buffer ON	V_{REFP} = 3.6 V	—	—	±15	LSB
			V_{REFP} = 1.8 V	—	—	±30	
		DAC output buffer OFF		—	—	±8	
OffsetCal(2)	Offset error at code 0x800 after factory calibration	DAC output buffer ON	V_{REFP} = 3.6 V	—	—	±6	
			V_{REFP} = 1.8 V	—	—	±8	
Gain(2)	Gain error	DAC output buffer ON		—	—	±0.5	%
		DAC output buffer OFF		—	—	±0.5	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

4.24. I2C characteristics

Table 4-57. I2C characteristics(1)(2)

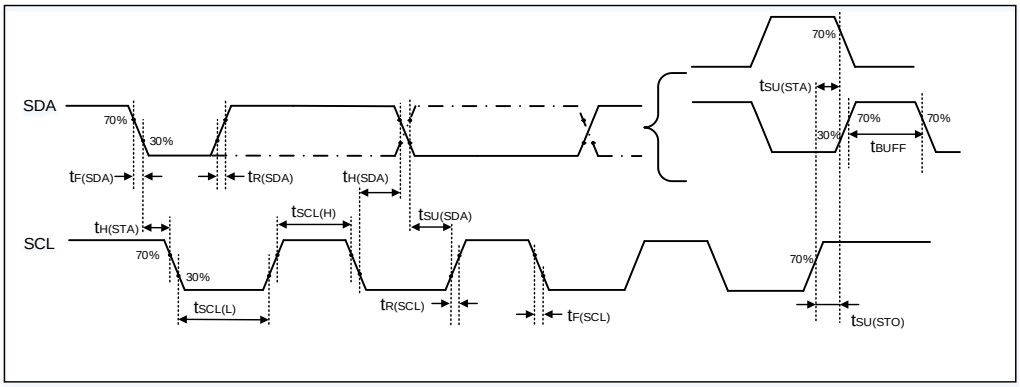
Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-11. I2C bus timing diagram



4.25. SPI characteristics

Table 4-58. Standard SPI characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	125	MHz
$t_{SCK(H)}$	SCK clock high time	—	3	4	5	ns
$t_{SCK(L)}$	SCK clock low time	—	3	4	5	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	1	—	ns
$t_{H(MO)}$	Data output hold time	—	—	1	—	ns
$t_{SU(MI)}$	Data input setup time	—	3	—	—	ns
$t_{H(MI)}$	Data input hold time	—	3	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	2	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	13	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	1	—	ns
$t_{V(SO)}$	Data output valid time	—	—	8	—	ns
$t_{H(SO)}$	Data output hold time	—	—	7	—	ns
$t_{SU(SI)}$	Data input setup time	—	2	—	—	ns
$t_{H(SI)}$	Data input hold time	—	2	—	—	ns

(1) Value guaranteed by characterization, not 100% tested in production.

Table 4-59. I2C analog filter delay characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{AF}	Analog filter delay time	—	50	80	130	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-12. SPI timing diagram – master mode

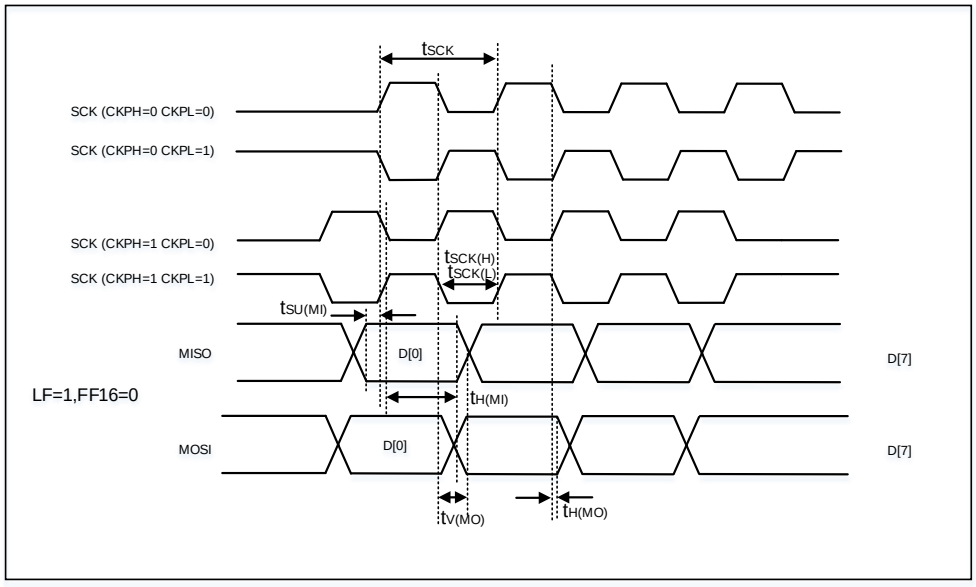
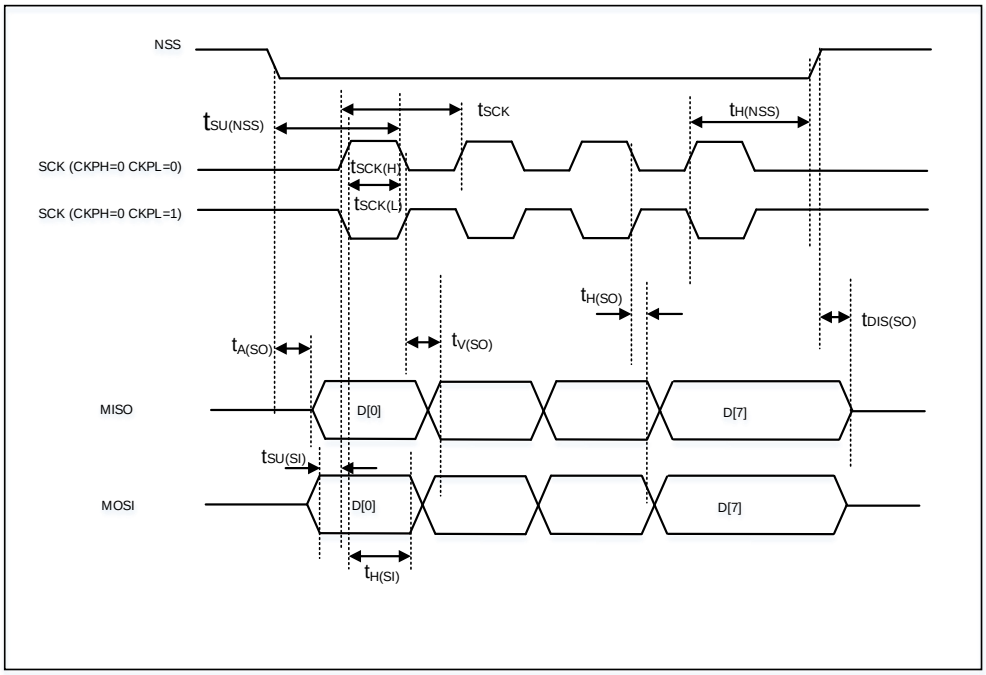


Figure 4-13. SPI timing diagram – slave mode



4.26. OSPI characteristics

Table 4-60. Standard OSPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SDR mode						
f_{SCK}	SCK clock frequency	—	—	—	100	MHz
$t_{SCK(H)}$	SCK clock high time, even division	—	$t_{(CK)}/2$	—	$t_{(CK)}/2+1$	ns
	SCK clock high time, odd division	—	$(n/2)*t_{(CK)}/(n+1)$	—	$(n/2)*t_{(CK)}/(n+1)+1$	ns
$t_{SCK(L)}$	SCK clock low time, even division	—	$t_{(CK)}/2–1$	—	$t_{(CK)}/2$	ns
	SCK clock low time, odd division	—	$(n/2+1)*t_{(CK)}/(n+1)–1$	—	$(n/2+1)*t_{(CK)}/(n+1)$	ns
$t_{V(MO)}$	Data output valid time	—	—	0.5	1	ns
$t_{H(MO)}$	Data output hold time	—	0	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	3.0	—	—	ns
$t_{H(MI)}$	Data input hold time	—	1.5	—	—	ns
DTR mode(no DQS)						
f_{SCK}	SCK clock frequency	—	—	—	57	MHz
$t_{SCK(H)}$	SCK clock high time, even division	—	$t_{(CK)}/2$	—	$t_{(CK)}/2+1$	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	SCK clock high time, odd division	—	(n/2)*$t_{(CK)}$/(n+1)	—	(n/2)*$t_{(CK)}$/(n+1)+1	ns
$t_{SCK(L)}$	SCK clock high time, even division	—	$t_{(CK)}$/2–1	—	$t_{(CK)}$/2	ns
	SCK clock high time, odd division	—	(n/2+1)*$t_{(CK)}$/(n+1)–1	—	(n/2+1)*$t_{(CK)}$ /(n+1)	ns
$t_{VR(SO)}$ $t_{VF(SO)}$	Data output valid time	DHQC = 0	—	6	7	ns
		DHQC = 1, Prescaler = 1,2 ...	—	t_{pclk}/4 + 1	t_{pclk}/4+1.25 (6)	
$t_{HR(SO)}$ $t_{HF(SO)}$	Data output hold time	DHQC = 0	4.5	—	—	ns
		DHQC = 1, Prescaler = 1,2 ...	t_{pclk}/4	—	—	
$t_{SUR(SI)}$ $t_{SUF(SI)}$	Data input setup time	—	3.0	—	—	ns
$t_{HR(SI)}$ $t_{HF(SI)}$	Data input hold time	—	1.50	—	—	ns

(1) Value guaranteed by characterization, not 100% tested in production.

Figure 4-14. OSPI timing diagram – SDR mode

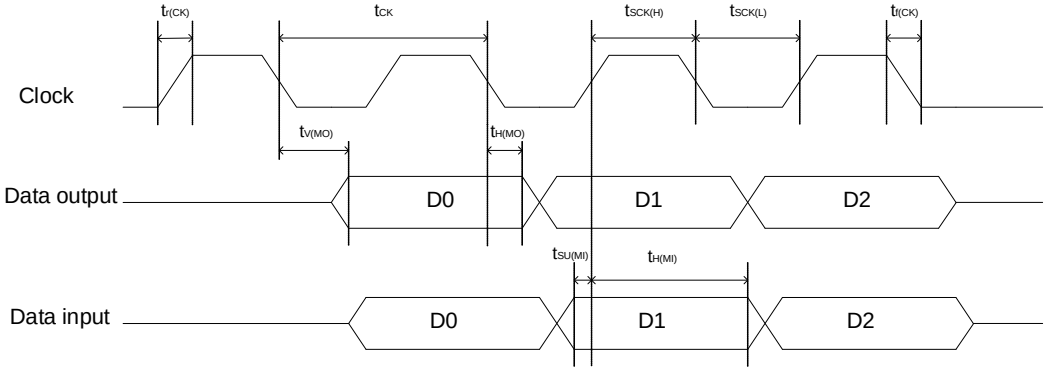
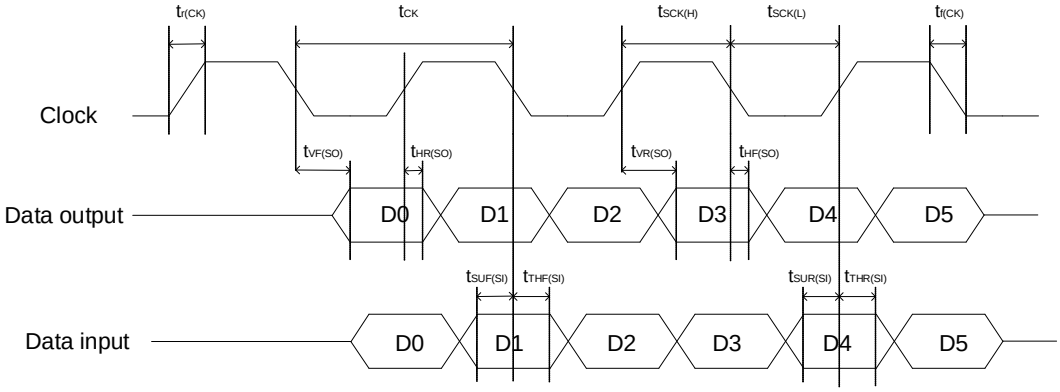


Figure 4-15. OSPI timing diagram – DTR mode



4.27. HPDF characteristics

Table 4-61. HPDF characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HPDFCLK}$	HPDF clock	—	—	f_{APB2}	f_{SYSCLK}	MHz
f_{CKIN} ($1 / T_{CKIN}$)	Input clock frequency	SPI mode(SITYP[1:0] = 01)	—	—	20 ($f_{HPDFCLK}$ / 4)	
f_{CKOUT}	Output clock frequency	—	—	—	20	
$Duty_{CKOUT}$	Output clock frequency duty cycle	—	30	50	75	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode(SITYP[1:0] = 01), External clock mode(SPICKSS[1:0] = 0)	T_{CKIN} / 2-0.5	T_{CKIN} / 2	—	ns
t_{SU}	Data input setup time	SPI mode(SITYP[1:0] = 01), External clock mode(SPICKSS[1:0] = 0)	1	—	—	
t_h	Data input hold time	SPI mode(SITYP[1:0] = 01), External clock mode(SPICKSS[1:0] = 0)	1	—	—	
$T_{Manchester}$	Manchester data period(recovered clock period)	Manchester mode(SITYP[1:0] = 10 or 11), Internal clock mode(SPICKSS[1:0] ≠ 0)	(CKOUTDIV+1)*$T_{HPDFCLK}$	—	(2*CKOUTDIV)*$T_{HPDFCLK}$	

(1) Value guaranteed by design, not 100% tested in production.

(2) Output speed is set to OSPEEDRy[1:0] = 10； Capacitive load C = 30 pF； Measurement points are done at COMS levels: 0.5 * V_{DD}.

4.28. I2S characteristics

Table 4-62. I2S characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 32 bits, Audio frequency = 96 kHz)	—	6.25	—	MHz
		Slave mode	—	—	12.5	
t_H	Clock high time	—	—	80	—	ns
t_L	Clock low time		—	80	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	0	—	—	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	1	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	3	—	—	ns
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	9	ns
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6	—	—	ns
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	6	ns
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

Figure 4-16. I2S timing diagram – master mode

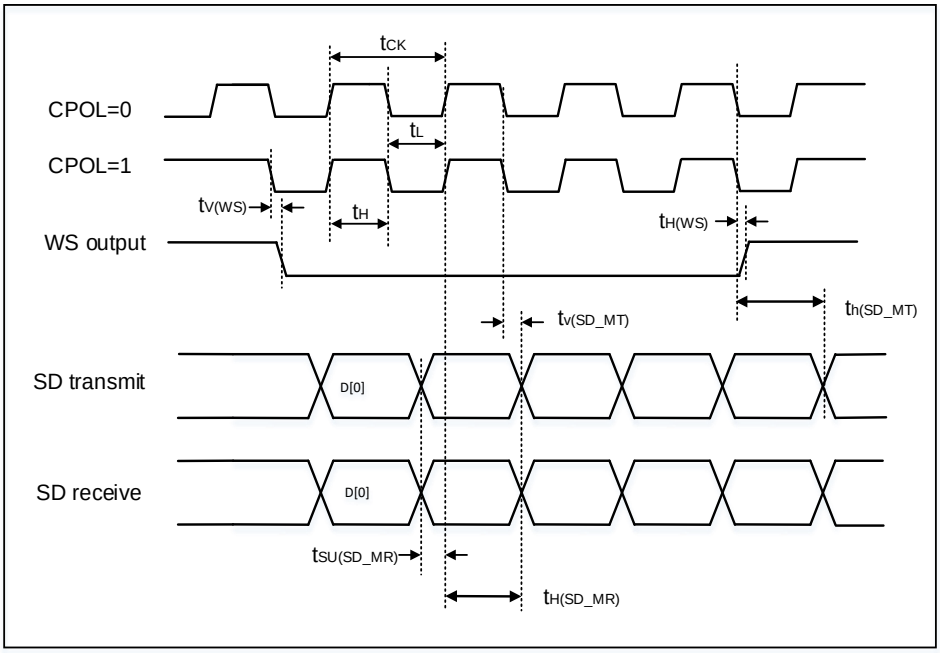
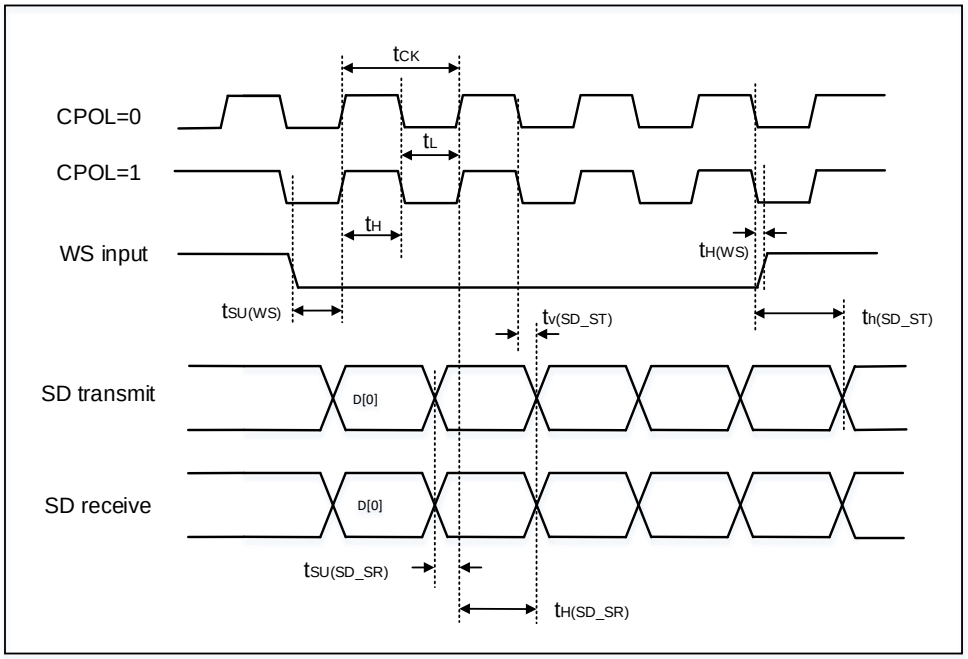


Figure 4-17. I2S timing diagram – slave mode



4.29. USART characteristics

Table 4-63. USART characteristics in Synchronous mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Fplckx = 300 MHz	—	—	37.5	MHz
$t_{SCK(H)}$	SCK clock high time	Fplckx = 300 MHz	13.3	—	—	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SCK(L)}$	SCK clock low time	Fplckx = 300 MHz	13.3	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-64. USART characteristics in Smartcard mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Fplckx = 300 MHz	—	—	150	MHz
$t_{SCK(H)}$	SCK clock high time	Fplckx = 300 MHz	3.33	—	—	ns
$t_{SCK(L)}$	SCK clock low time	Fplckx = 300 MHz	3.33	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.30. CAN characteristics

Refer to ***Table 4-30. I/O static characteristics*** for more details on the input/output alternate function characteristics (CANTX and CANRX).

4.31. USBHS characteristics

Table 4-65. USBHS DC electrical characteristics(1)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}		USB operating voltage	—	3	—	3.6	V
LS/FS FUNCTIONALITY							
Input levels	V_{DIFS}	Differential input sensitivity(FS / LS)	—	0.2	—	—	V
	V_{CMFS}	Differential common mode range(FS / LS)	Includes V_{DI} range	0.8	—	2.5	
	V_{ILSE}	Single ended receiver low level input voltage(FS / LS)	—	—	—	0.8	
	V_{IHSE}	Single ended receiver high level input voltage(FS / LS)	—	2.0	—	—	
Output levels	V_{OLFS}	Static output level low(FS / LS)	R_L of 1.0 kΩ to 3.63 V	—	—	0.3	V
	V_{OHFS}	Static output level high(FS / LS)	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.6	
R_{PD}		USBHS_DM/DP	V_{IN} = V_{DD}	17.6	21	24.7	kΩ
		PA9(USBHS_VBUS)		0.77	0.9	1.1	
R_{PU}		USBHS_DM/DP	V_{IN} = V_{SS}	1.3	1.5	1.83	
		PA9(USBHS_VBUS)		0.28	0.3	0.42	
Z_{HSDRV}		Driver Output Impedance	Steady state drive	40.5	45	49.5	Ω
HS FUNCTIONALITY							
Input levels	V_{DIHS}	Differential input sensitivity(HS)	—	0.1	—	—	V
	V_{CMHS}	Differential common mode range(HS)	—	-50	—	500	mV
	V_{HSSQ}	HS Squelch Detection Threshold	—	100	—	150	mV
	V_{HSDSC}	HS Disconnect Threshold	—	525	—	625	mV
Output levels	V_{OLHS}	High speed low level output voltage	45 Ω load	-10	—	10	mV
	V_{OHHS}	High speed high level output voltage	45 Ω load	360	400	440	mV

(1) Value guaranteed by design, not 100% tested in production.

Table 4-66. USBHS dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{FR}	Rise time(FS / LS)	C_L = 50 pF	4	5	20	ns
T_{HSR}	Differential Rise Time(HS)	—	500	600	—	ps
T_{FF}	Fall time(FS / LS)	C_L = 50 pF	4	5	20	ns
T_{HSF}	Differential Fall Time(HS)	—	500	600	—	ps
t_{RFM}	Rise/ fall time matching(FS / LS)	t_R / t_F	90	—	110	%
v_{CRS}	Output signal crossover voltage(FS / LS)	—	1.3	—	2.0	V

(1) Value guaranteed by design, not 100% tested in production.

Table 4-67. USBHS Charger Detection characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DAT_SRC}	Data Source Voltage	—	0.5	—	0.7	V
I_{DP_SRC}	Data Connect Current	—	7	—	13	uA
V_{DAT_REF}	Data Detect Voltage	—	0.25	—	0.4	V

(1) Value guaranteed by design, not 100% tested in production.

Table 4-68. USBHS clock timing parameters(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	USBHS operating voltage	3.0	—	3.63	V
f_{HCLK}	f_{HCLK} value to guarantee proper operation of USBHS interface	30	—	—	MHz
F_{START_8BIT}	Frequency (first transition) 8-bit ± 10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm	59.97	60	60.63	MHz
D_{START_8BIT}	Duty cycle (first transition) 8-bit ± 10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm	49.975	50	50.025	%

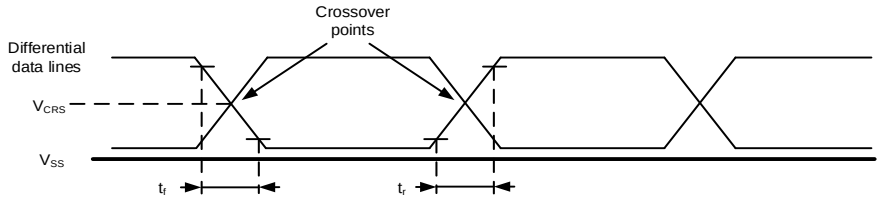
(1) Value guaranteed by design, not 100% tested in production.

Table 4-69. USB-ULPI Dynamic characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	—	—	2	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0.5	—	—	ns
t_{SD}	Data in setup time	—	—	2	ns
t_{HD}	Data in hold time	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-18. USBFS timings: definition of data signal rise and fall time



4.32. EXMC characteristics

Table 4-70. Asynchronous non-multiplexed SRAM / PSRAM / NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	5*Tfclk-1	5*Tfclk+1	ns
$t_{V(NOE\_NE)}$	EXMC_Nex low to EXMC_NOE low	0	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	5*Tfclk-1	5*Tfclk+1	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_Nex low to EXMC_A valid	0	—	ns
$t_{v(BL\_NE)}$	EXMC_Nex low to EXMC_BL valid	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_Nex high setup time	4*Tfclk-1	—	ns

Symbol	Parameter	Min	Max	Unit
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	4*Tfclk-1	—	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_Nex high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_Nex low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	Tfclk-1	Tfclk+1	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

Table 4-71. Asynchronous non-multiplexed SRAM / PSRAM / NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	3*Tfclk-1	3*Tfclk+1	ns
$t_{V(NWE\_NE)}$	EXMC_Nex low to EXMC_NWE low	Tfclk-1	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	Tfclk-1	Tfclk+1	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	Tfclk-1	Tfclk+1	ns
$t_{v(A\_NE)}$	EXMC_Nex low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_Nex low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	Tfclk-1	Tfclk+1	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	2*Tfclk-1	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	Tfclk-1	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	Tfclk-1	—	ns
$t_{v(BL\_NE)}$	EXMC_Nex low to EXMC_BL valid	0	—	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	0	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	Tfclk-1	—	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

Table 4-72. Asynchronous multiplexed PSRAM / NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	7*Tfclk-1	7*Tfclk+1	ns
$t_{V(NOE\_NE)}$	EXMC_Nex low to EXMC_NOE low	3*Tfclk-1	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	4*Tfclk-1	4*Tfclk+1	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_Nex low to EXMC_A valid	0	—	ns
$t_{v(A\_NOE)}$	Address hold time after EXMC_NOE high	0	—	ns
$t_{v(BL\_NE)}$	EXMC_Nex low to EXMC_BL valid	0	—	ns
$t_{h(BL\_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_Nex high setup time	4*Tfclk-1	—	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	4*Tfclk-1	—	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_Nex high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_Nex low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	Tfclk-1	Tfclk+1	ns

Symbol	Parameter	Min	Max	Unit
$T_{h(AD\_NADV)}$	EXMC_AD(114ddress) valid hold time after EXMC_NADV high	Tfclk-1	Tfclk+1	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-73. Asynchronous multiplexed PSRAM / NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	5*Tfclk-1	5*Tfclk+1	ns
$t_{V(NWE\_NE)}$	EXMC_Nex low to EXMC_NWE low	Tfclk-1	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	3*Tfclk-1	3*Tfclk+1	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	Tfclk-1	—	ns
$t_{v(A\_NE)}$	EXMC_Nex low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_Nex low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	Tfclk-1	Tfclk+1	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	Tfclk-1	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	Tfclk-1	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	Tfclk-1	—	ns
$t_{v(BL\_NE)}$	EXMC_Nex low to EXMC_BL valid	0	—	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	Tfclk-1	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	Tfclk-1	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-74. Synchronous multiplexed PSRAM / NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	Texmc_clk	—	ns
$t_{d(CLKL-NexL)}$	EXMC_CLK low to EXMC_Nex low	0	—	ns
$t_{d(CLKH-NexH)}$	EXMC_CLK high to EXMC_Nex high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	2*Tfclk-1	—	ns
$t_{d(CLKL-ADV)}$	EXMC_CLK low to EXMC_AD valid	0	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-75. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	Texmc_clk	—	ns
$t_{d(CLKL-NexL)}$	EXMC_CLK low to EXMC_Nex low	0	—	ns
$t_{d(CLKH-NexH)}$	EXMC_CLK high to EXMC_Nex high	2*Tfclk-1	—	ns

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	2*Tfclk-1	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

Table 4-76. Synchronous non-multiplexed PSRAM / NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	Texmc_clk	—	ns
$t_{d(CLKL-NexL)}$	EXMC_CLK low to EXMC_Nex low	0	—	ns
$t_{d(CLKH-NexH)}$	EXMC_CLK high to EXMC_Nex high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	2*Tfclk-1	—	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

Table 4-77. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	Texmc_clk	—	ns
$t_{d(CLKL-NexL)}$	EXMC_CLK low to EXMC_Nex low	0	—	ns
$t_{d(CLKH-NexH)}$	EXMC_CLK high to EXMC_Nex high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	2*Tfclk-1	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

Table 4-78. SDRAM read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	EXMC_SDCLK period	2 Tfclk – 0.5	2 Tfclk +0.5	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	3.5	—	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	—	
$t_{d(SDCLKL\_Add)}$	Address valid time	—	2.5	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	—	2.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	—	
$t_{d(SDCLKL\_NRAS)}$	NRAS valid time	—	2	
$t_{h(SDCLKL\_NRAS)}$	NRAS hold time	0	—	
$t_{d(SDCLKL\_NCAS)}$	NCAS valid time	—	2	
$t_{h(SDCLKL\_NCAS)}$	NCAS hold time	0	—	

4.33. TIMER characteristics

Table 4-79. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	3.3	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 300 MHz	0	333	MHz
RES	Timer resolution	TIMER0 & TIMER2 & TIMER3 & TIMER7& TIMER14 & TIMER15 & TIMER16 & TIMER40 & TIMER41 & TIMER42 & TIMER43 & TIMER44	—	16	bit
		TIMER1 & TIMER4 & TIMER5 & TIMER6 & TIMER22 & TIMER23	—	32	bit
		TIMER50 & TIMER51	—	64	bit

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	0.0033	218.45	μs
	32-bit counter clock period when internal clock is selected	—	1	4294967296	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	0.0033	14316557.65	μs
	64-bit counter clock period when internal clock is selected	—	1	18446744073709551616	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	0.0033	61489146912365172.05	μs
t_{MAX_COUNT}	Maximum possible count （16-bit）	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	—	14.3	s
	Maximum possible count (32-bit)	—	—	4294967296x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	—	938249.9	s
	Maximum possible count (64-bit)	—	—	18446744073709551616x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	—	1119375758902.4	h

(1) Value guaranteed by design, not 100% tested in production.

4.34. WDGT characteristics

Table 4-80. FWDGT min/max timeout period at 32 kHz (IRC32K) (1)

Prescaler divider	PR[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.78125	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-81. WWDGT min-max timeout value at 50 MHz (f_{PCLK1}) (1)

Prescaler divider	PSC[2:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	81.92	µs	5.24	ms
1/2	01	163.84		10.49	
1/4	10	327.68		20.97	
1/8	11	655.36		41.94	

(1) Value guaranteed by design, not 100% tested in production.

4.35. EtherCAT SubDevice Controller (ESC) characteristics

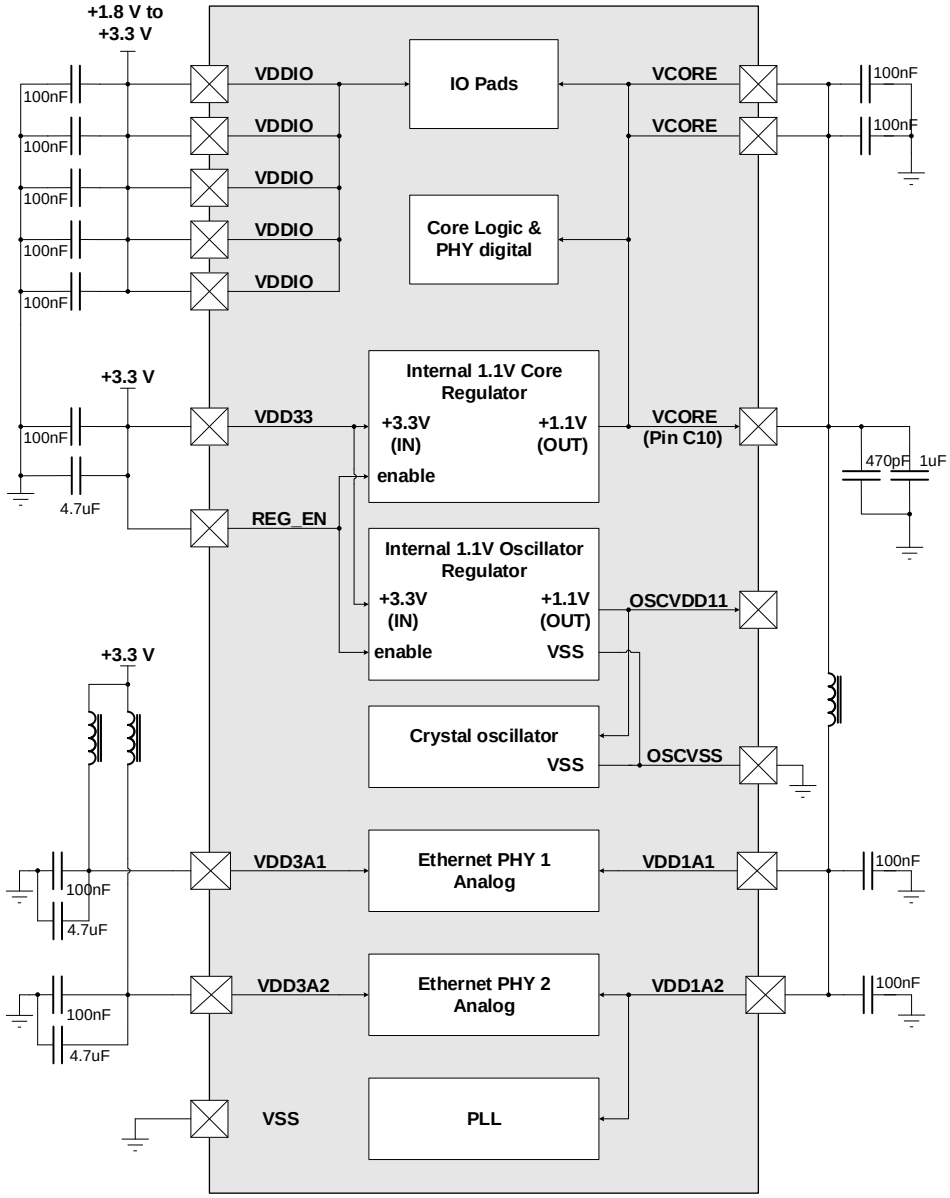
4.35.1. Recommended DC characteristics

Table 4-82. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD1Ax}	Analog 1.1V power for Ethernet PHY	—	1.05	1.1	1.15	V
$V_{OSCVDD11}$	Internal 1.1V oscillator supply voltage	—	1.0	1.1	1.2	V
V_{CORE}	Digital core supply voltage	—	1.05	1.1	1.15	V
V_{DD3Ax}	Analog 3.3V power for Ethernet PHY	—	3.0	3.3	3.6	V
V_{DD33}	Supply voltage for the internal regulator	—	3.0	3.3	3.6	V
V_{DDIO}	IO supply voltage	—	1.8	3.3	3.6	V

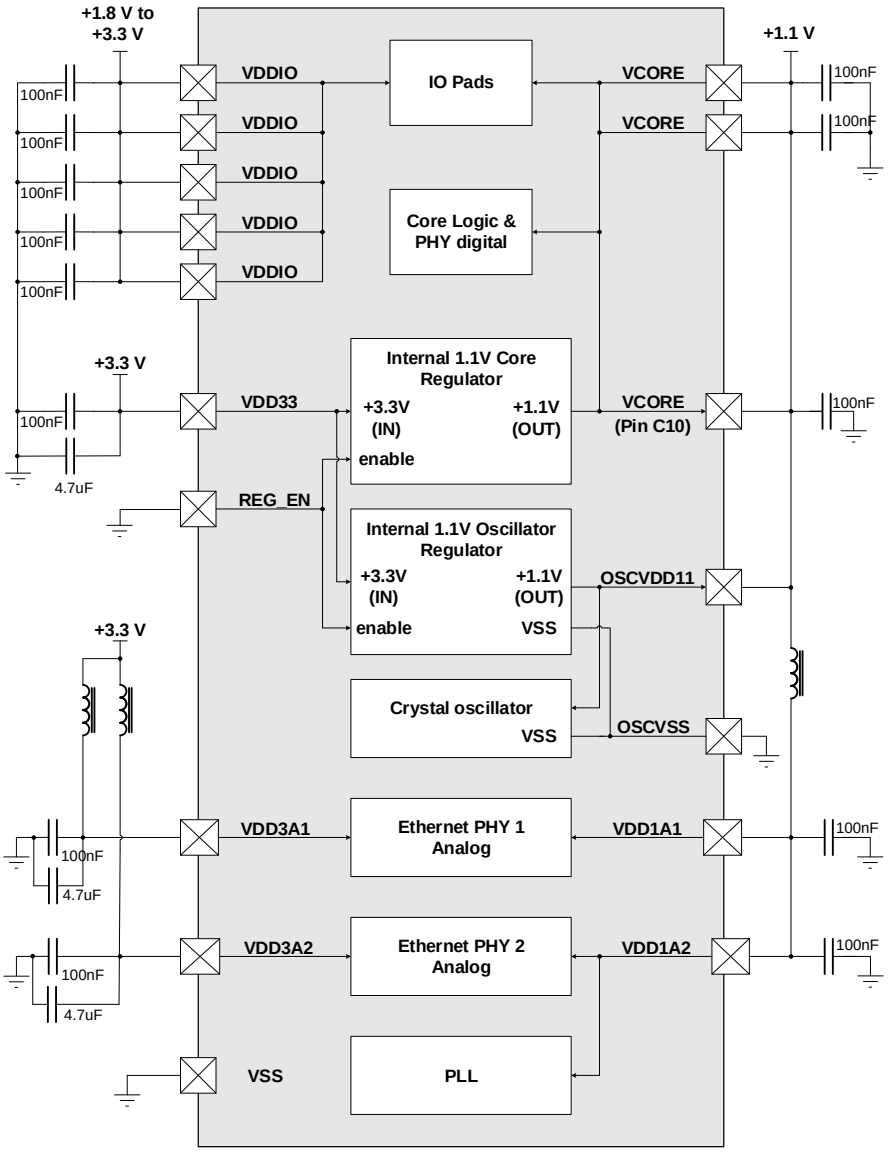
(1) Value guaranteed by characterization, not 100% tested in production.

Figure 4-19. Recommended power connections(regulators enabled)(1)



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Figure 4-20. Recommended power connections(regulators disabled) (1)



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-83. Power supply on and off timing values(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PON}	Power supply turn on time	—	—	—	50	ms
t_{POFF}	Power supply turn off time	—	—	—	500	ms

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-21. Power supply on and off timing (internal regulators)

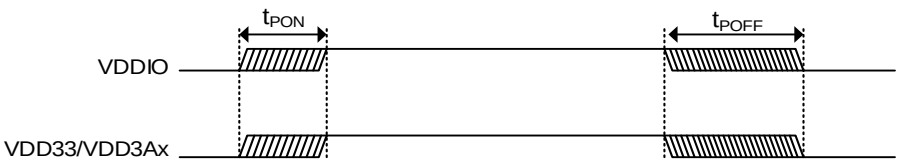


Figure 4-22. Power supply on and off timing (external regulators)

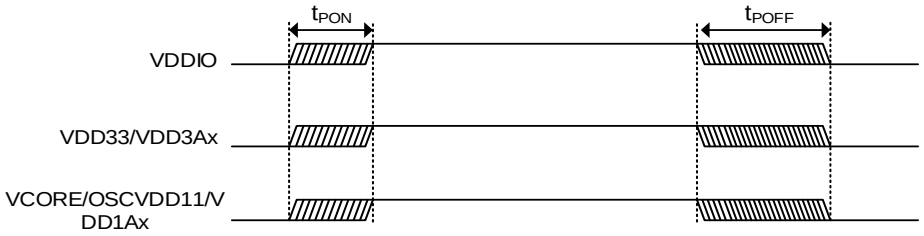


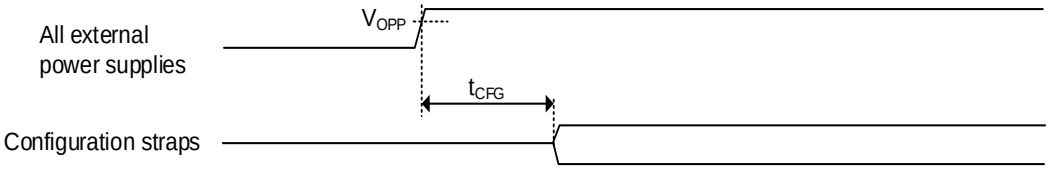
Table 4-84. Power-on configuration strap latching timing values(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CFG}	Configuration strap valid time	—	—	—	15	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) Configuration straps must only be pulled high or low. Configuration straps must not be driven as inputs.

Figure 4-23. Power-on configuration strap latching timing diagram



4.35.2. Power consumption

The power consumption only includes systems EtherCAT SubDevice Controller (ESC) and EtherCAT PHY.

Table 4-85. Power consumption characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Regulators enabled						
3.3V Device Current(2)	Supply current (MOD0)	Disconnect to the Ethernet cable	—	36	—	mA
		100BASE-TX with traffic	—	86	—	
		100BASE-TX with idle	—	85	—	
	Supply current (MOD1)	100BASE-TX with idle	—	82	—	
	Supply current (MOD2)	100BASE-TX with idle	—	80	—	
	Supply current (MOD3)	All clocks off	—	17	—	
Regulators disabled						
3.3V Device Current(2)	Supply current (MOD0)	Disconnect to the Ethernet cable	—	24	—	mA
		100BASE-TX with traffic	—	42	—	
		100BASE-TX with idle	—	42	—	
	Supply current (MOD1)	100BASE-TX with idle	—	40	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Supply current (MOD2)	100BASE-TX with idle	—	40	—	
	Supply current (MOD3)	All clocks off	—	16	—	
1.1V Device Current(3)	Supply current (MOD0)	Disconnect to the Ethernet cable	—	8	—	
		100BASE-TX with traffic	—	44	—	
		100BASE-TX with idle	—	44	—	
	Supply current (MOD1)	100BASE-TX with idle	—	42	—	
	Supply current (MOD2)	100BASE-TX with idle	—	40	—	
	Supply current (MOD3)	All clocks off	—	0	—	

(1) Value guaranteed by sample, not 100% tested in production.

(2) Including the following pins，VDD33,VDD3Ax,VDDIO.

(3) Including the following pins，OSCVDD11,VDD1Ax,VCORE.

4.35.3. I/O characteristics

Table 4-86. Non-variable I/O DC electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog input buffer(RXPA/RXNA/RXPB/RXNB)						
V_{IN_DIFF}	Differential input level	—	—	2	—	V
V_{CM}	Common mode voltage		—	1.65	—	
C_{IN}	Input capacitance		—	3.27	—	pF
Crystal oscillator input buffer(OSCI input)						
V_{ILI}	Low input level	—	-0.3	—	0.35	V
V_{IHI}	High input level		OSCVDD11-0.35	—	3.6	
Low voltage PECL input buffer						
V_{IL}	Low input level	—	-0.3	—	0.8	V
V_{IH}	High input level		2	—	3.93	
Low voltage PECL output buffer						
V_{OL}	Low input level	—	—	—	0.4	V
V_{OH}	High input level		2.4	—	—	
C_{LOAD}	Load capacitance		—	1.1	—	pF

(1) Value guaranteed by design, not 100% tested in production.

Table 4-87. Variable I/O DC electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ		Max	Unit
				1.8V	3.3V		
Schmitt-triggered input buffer							
V_{ILI}	Low input level	—	-0.3	—	—	—	V
V_{IHI}	High input level		—	—	—	3.6	
V_{ILT}	Negative-going threshold		0.65	0.8	1.47	1.75	
V_{IHT}	Positive-going threshold		0.81	0.96	1.61	1.88	
V_{HYS}	Schmitt trigger hysteresis (V_{IHT} – V_{ILT})		120	150	145	210	mV
I_{IH}	Input leakage (V_{IN} = VSS or VDDIO)		-10	—	—	10	uA
C_{IN}	Input capacitance		—	5	5	7	pF
R_{PU}	Weak pull-up equivalent resistor (V_{IN} = VSS)		57.6	68	68	80	kΩ
I_{PU}	Pull-up current (V_{IN} = VSS)		62.5	26	48	20.25	uA
R_{PD}	Weak pull-down equivalent resistor (V_{IN} = VDD33)		57.5	68	68	80.1	kΩ
I_{PD}	Pull-down current (V_{IN} = VDD33)		62.6	26	48	20.2	uA
Variable voltage output with 8 mA sink and 8 mA source buffers							
V_{OL}	Low output level	I_{load} = 8mA	—	—	—	0.4	V
V_{OH}	High output level	I_{load} = -8mA	VDDIO - 0.4	—	—	—	
Variable voltage open-drain output with 8 mA sink buffers							
V_{OL}	Low output level	I_{load} = 8mA	—	—	—	0.4	V
Variable voltage output with 12 mA sink and 12 mA source buffers							
V_{OL}	Low output level	I_{load} = 12mA	—	—	—	0.4	V
V_{OH}	High output level	I_{load} = -12mA	VDDIO - 0.4	—	—	—	
Variable voltage open-drain output with 12 mA sink buffers							
V_{OL}	Low output level	I_{load} = 12mA	—	—	—	0.4	V
Variable voltage open-source output with 12 mA source buffers							
V_{OH}	High output level	I_{load} = -12mA	VDDIO -0.4	—	—	—	V

(1) Value guaranteed by design, not 100% tested in production.

Table 4-88. 100base-TX transceiver characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PPH}(2)	Peak differential output voltage high	950	—	1050	mVpk
V_{PPL}(2)	Peak differential output voltage low	-950	—	-1050	mVpk
V_{SS}(2)	Signal amplitude symmetry	98	—	102	%
T_{RF}(2)	Signal rise and fall time	3	—	5	ns
T_{RFS}(2)	Rise and fall symmetry	—	—	0.5	ns
D_{CD}	Duty cycle distortion	—	—	0.5	ns
V_{OS}	Overshoot and undershoot	—	—	5	%
—	Jitter	—	—	1.4	ns

(1) Value guaranteed by characterization, not 100% tested in production.

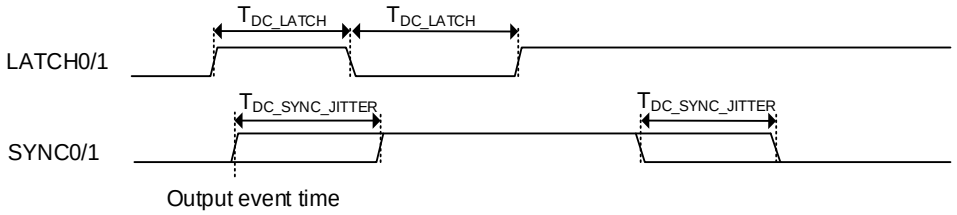
(2) Measured at line side of transformer, line replace by 100ohm(1%) resistor.

Table 4-89. ETHERCAT SYNC/LATCH timing values(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{DC_LATCH}	Time between LATCH0 or LATCH1 events	—	15	—	—	ns
$t_{DC\_SYNC\_JITTER}$	SYNC0 or SYNC1 output jitter	—	—	—	15	ns

(1) Value guaranteed by characterization, not 100% tested in production.

Figure 4-24. Ethercat SYNC/LATCH timing diagram



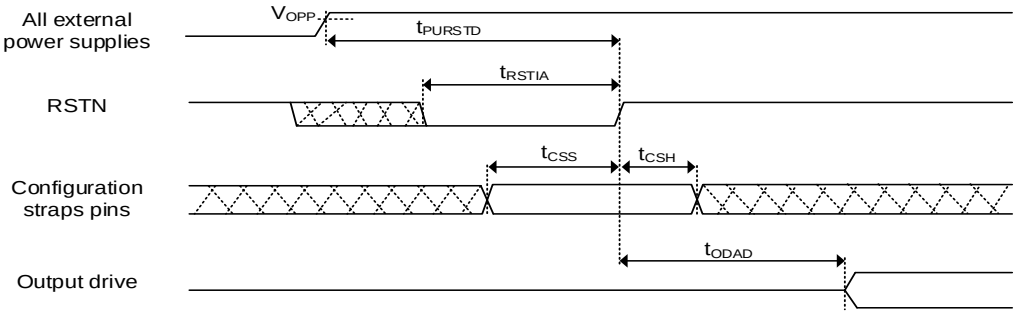
4.35.4. RSTN pin characteristics

Table 4-90. RSTN pin configuration strap latching timing values(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PURSTD}	External power supplies at operational level to RSTN invalid time	—	25	—	—	ms
t_{RSTIA}	RSTN input valid time	—	200	—	—	us
T_{CSS}	Configuration strap pins setup time to RSTN invalid	—	200	—	—	ns
t_{CSH}	Configuration strap pins hold time after RSTN invalid	—	30	—	—	ns
t_{ODAD}	Output drive time after RSTN invalid	—	3	—	—	us

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-25. Power-on configuration strap latching timing diagram



4.35.5. Clock characteristics

Table 4-91. Crystal specifications(1)

Symbol	Parameter	Min	Typ	Max	Unit
Crystal cut		AT, typ			
Crystal oscillation mode		Fundamental mode			
Crystal calibration mode		Parallel resonant mode			
F_{FUND}	Frequency	—	25.000	—	MHZ
F_{TOL}	802.3 Frequency tolerance at 25℃	—	—	±40	ppm
F_{TEMP}	802.3 Frequency stability over temp	—	—	±40	ppm
F_{AGE}	802.3 Frequency deviation over time	—	±3 ~ 5	—	ppm
802.3 total allowable PPM budget		—	—	±50	ppm
F_{TOL}	EtherCAT frequency tolerance at 25℃	—	—	±15	ppm
F_{TEMP}	EtherCAT frequency stability over Temp	—	—	±15	ppm
F_{AGE}	EtherCAT frequency deviation over Time	—	±3 ~ 5	—	ppm
EtherCAT total allowable PPM budget		—	—	±25	ppm
C_O	Parallel Capacitance	—	—	7	pF
C_L	Recommended matching capacitance on OSCI and OSCO	—	10	20	pF
R_1	Equivalent Series Resistance	—	—	100	Ω
Operating Temperature Range		-40	—	125	°C
OSCI Pin Capacitance		—	3	—	pF
OSCO Pin Capacitance		—	3	—	pF

(1) Value guaranteed by design, not 100% tested in production.

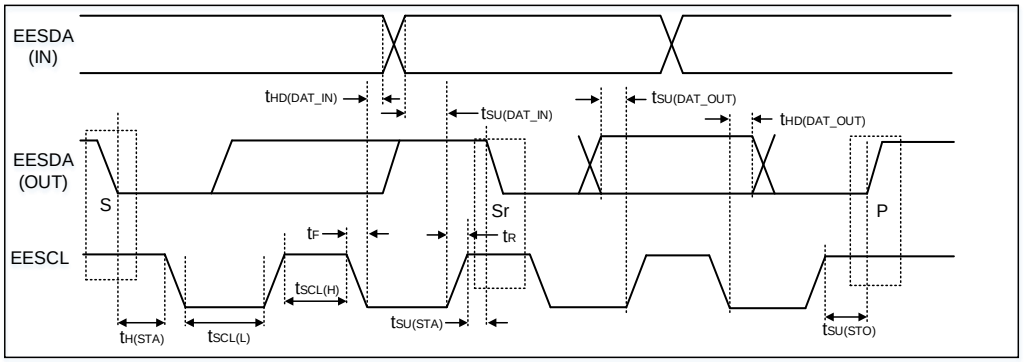
4.35.6. I2C characteristics

Table 4-92. I2C controller timing values(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	EESCL clock frequency	—	—	148.8	—	KHz
$t_{SCL(H)}$	EESCL clock high time	—	3.0	—	—	us
$t_{SCL(L)}$	EESCL clock low time	—	3.0	—	—	us
$t_{r(SDA/SCL)}$	EESDA and EESCL rise time	—	—	—	300	ns
$t_{f(SDA/SCL)}$	EESDA and EESCL fall time	—	—	—	300	ns
$t_{SU(STA)}$(2)	Setup time (provided to target) of EESCL high before EESDA output falling for repeated start condition	—	1000	—	—	ns
$t_{HD(STA)}$(2)	Hold time (provided to target) of EESCL after EESDA output falling for start or repeated start condition	—	1000	—	—	ns
$t_{SU(DAT\_IN)}$(3)	Setup time (from target) EESDA input before EESCL rising	—	200	—	—	ns
$t_{HD(DAT\_IN)}$	Hold time (from target) of EESDA input after EESCL falling	—	0	—	—	ns
$t_{SU(DAT\_OUT)}$(3)	Setup time (provided to target) EESDA output before EESCL rising	—	400	—	—	ns
$t_{HD(DAT\_OUT)}$(3)	Hold time (provided to target) of EESDA output after EESCL falling	—	400	—	—	ns
$t_{SU(STO)}$(2)	Setup time (provided to target) of EESCL high before EESDA output rising for stop condition	—	1000	—	—	ns

(1) Guaranteed by design, not 100% tested in production.
(2) These values provide 400ns of margin compared to the I2C fast-mode specification.
(3) These values provide a margin of approximately 2100ns compared to the I2C fast-mode specification.

Figure 4-26. I2C bus timing diagram



4.36. Ethernet PHY characteristics

Table 4-93. MII TX timing values(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLKP}	MII_CLK25 period	40	—	—	ns
t_{CLKH}	MII_CLK25 high time	18	—	22	ns
t_{CLKL}	MII_CLK25 low time	18	—	22	ns
t_{VAL}	MII_TXD[3:0], MII_TXEN output valid from rising edge of MII_CLK25	—	—	10	ns
t_{HOLD}	MII_TXD[3:0], MII_TXEN output hold from rising edge of MII_CLK25	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-27. MII TX timing diagram

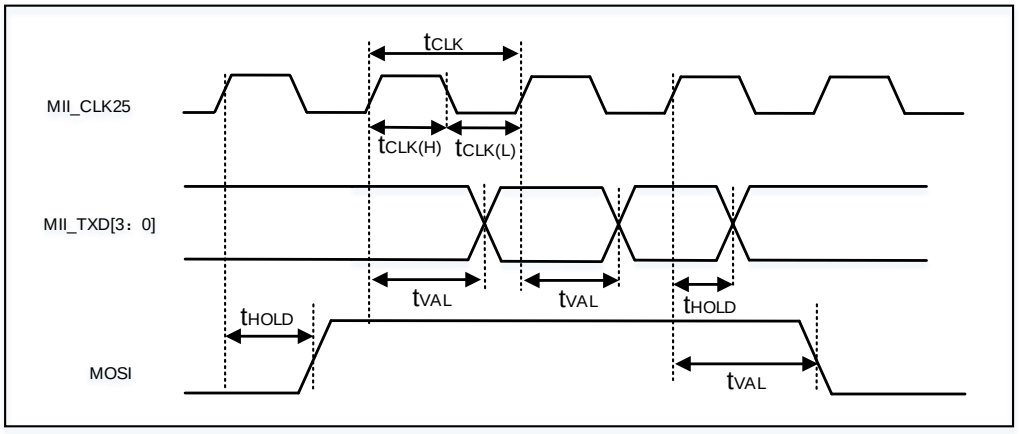


Table 4-94. MII RX timing values(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLKP}	MII_RXCLK period	40	—	—	ns
t_{CLKH}	MII_RXCLK high time	16	—	24	ns
t_{CLKL}	MII_RXCLK low time	16	—	24	ns
t_{SU}	MII_RXD[3:0], MII_RXER, MII_RXDV setup time to rising edge of MII_RXCLK	5	—	—	ns
t_{HOLD}	MII_RXD[3:0], MII_RXER, MII_RXDV hold time after rising edge of MII_RXCLK	6	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-28. MII RX timing diagram

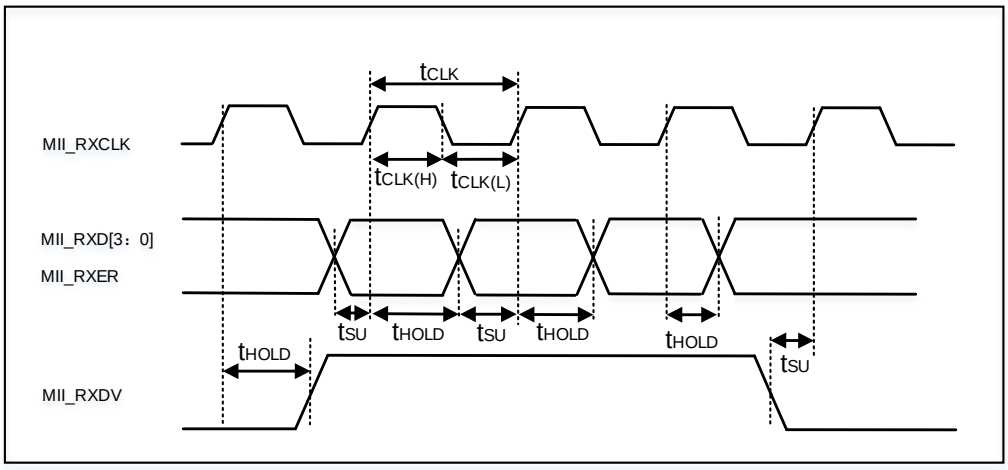
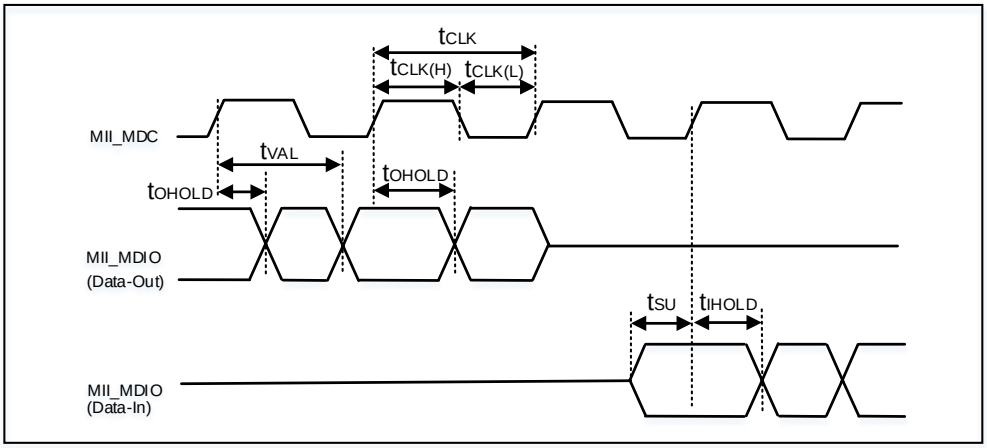


Table 4-95. Management access timing values(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLKP}	MII_MDC period	400	—	—	ns
t_{CLKH}	MII_MDC high time	180	—	—	ns
t_{CLKL}	MII_MDC low time	180	—	—	ns
t_{VAL}	MII_MDIO output valid from rising edge of MII_MDC	—	—	250	ns
t_{OHOLD}	MII_MDIO output hold from rising edge of MII_MDC	150	—	—	ns
t_{SU}	MII_MDIO input setup time to rising edge of MII_MDC	70	—	—	ns
t_{IHOLD}	MII_MDIO input hold time after rising edge of MII_MDC	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-29. Management access timing diagram



5. Package information

5.1. BGA240 package outline dimensions

Figure 5-1. BGA240 package outline

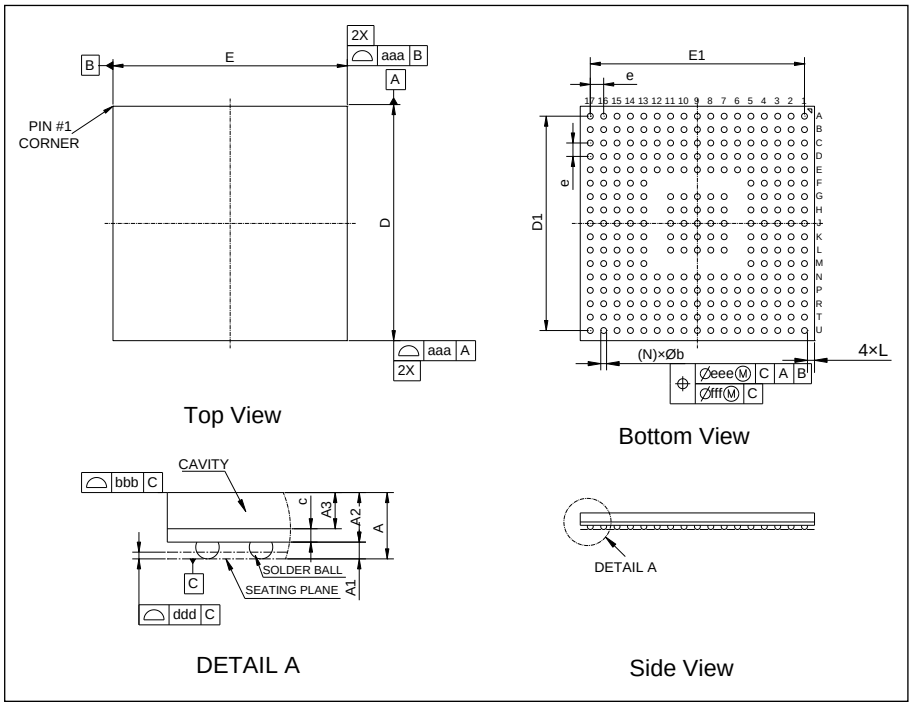
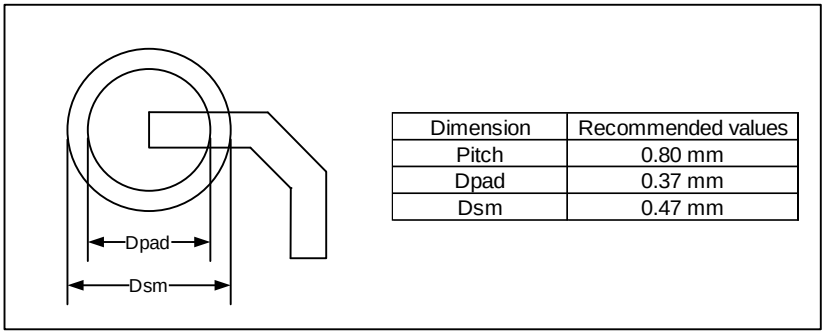


Table 5-1. BGA240 package dimensions

Symbol	Min	Typ	Max
A	0.91	0.99	1.07
A1	0.20	0.25	0.30
A2	0.69	0.74	0.79
A3	—	0.54	—
b	0.31	0.36	0.41
c	0.17	0.20	0.23
D	13.90	14.00	14.10
D1	—	12.80	—
E	13.90	14.00	14.10
E1	—	12.80	—
e	—	0.80	—
L	—	0.425	—
aaa	—	0.15	—
bbb	—	0.20	—
ddd	—	0.10	—
eee	—	0.15	—
fff	—	0.08	—

(Original dimensions are in millimeters)

Figure 5-2. BGA240 recommended footprint



Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.37 mm
Dsm	0.47 mm

(Original dimensions are in millimeters)

5.2. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “θ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\Theta_{JA}=(T_J - T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J - T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J - T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-2. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	BGA240	TBD	°C/W
θ_{JB}	Cold plate, 2S2P PCB	BGA240	TBD	°C/W
θ_{JC}	Cold plate, 2S2P PCB	BGA240	TBD	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	BGA240	TBD	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	BGA240	TBD	°C/W

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32H75Exx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32H75EYMJ6	3840	BGA240	Green	Industrial -40 °C to +85 °C
GD32H75EYMJ7	3840	BGA240	Green	Industrial -40 °C to +105 °C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov.08, 2024
1.1	1. Update ***Figure 2 1. GD32H75Exx block diagram***. 2. Update ***Table 2 2. Memory map of GD32H75Exx devices***. 3. In the Internal clock characteristics section, delete ***Table 4-21. High speed internal clock (IRC48M) characteristics***, ***Table 4-22. High speed internal clock (IRC64M) characteristics***, ***Table 4-23. Low power internal clock (LPIRC4M) characteristics***, and the accuracy range for T7 products in the table. Add the IRC32K frequency min and max values to ***Table 4-24***. Low speed internal clock (IRC32K) characteristics. 4. In the External clock characteristics section, correct the spelling errors in the English words in ***Figure 4-15***, Recommended external OSCIN and OSCOUT pins circuit for oscillator. 5. Electrical characteristics, EMC parameters: Delete mode1 and mode3 parameters from ***Table 4-13***. EMI characteristics(1), and delete VFB=1.8 and 2.5 parameters from ***4.8. Typical SMPS efficiency versus load current and temperature***. 6. Electrical characteristics Add new 14-bit ADC performance parameters in ***Table 4-36.*** 14-bit ADC accuracy. 7. Delete the mode3 diagram from ***Figure 4-3***. External components for SMPS step-down converter. 8. Delete mode1 power consumption from ***Table 4-11***. Power consumption characteristics. 9. Update ***Figure 4 4***. Recommended PDR_ON pin circuit.	Jan.17, 2025
1.2	1. Delete the GD32H75EYMJ6B device and add the GD32H75EYMJ7 device. 2. ***Table 4-11 Power consumption characteristics***, remove Typ SMPS ON consumption and add Typ LDO regulator ON consumption. 3. For pin TXPB, the default function is updated to TXPB, additional function TXP_P2, refer to ***Pin definitions***. 4. Update I2C quantity to 4, refer to ***Inter-integrated circuit (I2C)***. 5. Update important notice	Apr.24, 2025

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