GigaDevice Semiconductor Inc.

GD32G5x3 Comparator User Guide

Application Note
AN198

Revision 1.0

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1 Introduction

This document is specifically designed for engineers developing with GD32G5x3 series devices, with basic functions and typical application cases displayed。

In Chapter 2, basic specifications and design functions are illustrated, and discussion about static voltage offset problem and calibration method is highlighted.

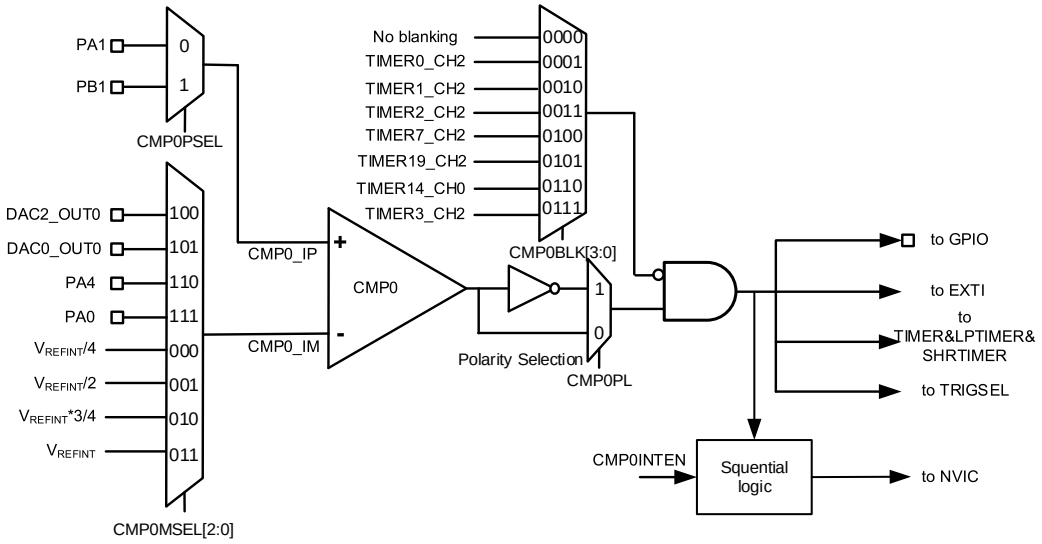
In Chapter 3, typical applicaion cases about GD32G5x3 comparators in digital switching-mode power supply control and motor control, proving advantages of GD32G5x3 comparators. Moreover, in order to learn more application methods about fault protection and extermal event of GD32G5x3 HRTIMER, please refer to ‘AN203 GD32G5x3 High-Resolution Timer User Guide’.

2 GD32G5x3 Comparator Introduction

Eight rail-to-rail comparators (CMPs) CMP0 ~ CMP7 supplied by V_{DDA} are integrated in GD32G5x3, which can realize low propagation delay, programmable inner hysteresis voltage, CMP output blanking, multiple input and output sources of CMP, CMP output hold on during system reset, etc.

In *Figure 2-1. GD32G5x3 comparator system*, basic diagram of GD32G5x3 CMP is presented with CMP0 as example, fitting for CMP1 ~ CMP7 at the same time.

Figure 2-1. GD32G5x3 comparator system



2.1 Input and output connections

Table 2-1. GD32G5x3 comparator input and output connections shows input and output connections sources (I/O, inner signal sources) of GD32G5x3 CMPs; most importantly, input and output channels of CMP must be configured as analog mode.

Table 2-1. GD32G5x3 comparator input and output connections

	CMP0	CMP1	CMP2	CMP3	CMP4	CMP5	CMP6	CMP7
CMP non inverting inputs connected to I/Os	PA1 PB1	PA7 PA3	PA0 PC1	PB0 PE7	PB13 PD12	PB11 PD11	PB14 PD14	PC2 PE9
CMP inverting inputs connected to I/Os	PA4 PA0	PA5 PA2	PF1 PC0	PE8 PB2	PB10 PD13	PD10 PB15	PD15 PB12	PD8 PD9

	CMP0	CMP1	CMP2	CMP3	CMP4	CMP5	CMP6	CMP7
CMP inverting inputs connected to internal signals	$V_{REFINT}/4$, $V_{REFINT}/2$, $V_{REFINT}*3/4$, V_{REFINT}, DAC2_OUT0 DAC0_OUT0	$V_{REFINT}/4$, $V_{REFINT}/2$, $V_{REFINT}*3/4$, V_{REFINT}, DAC2_OUT1 DAC0_OUT1	$V_{REFINT}/4$, $V_{REFINT}/2$, $V_{REFINT}*3/4$, V_{REFINT}, DAC2_OUT0 DAC0_OUT0	$V_{REFINT}/4$, $V_{REFINT}/2$, $V_{REFINT}*3/4$, V_{REFINT}, DAC2_OUT1 DAC0_OUT0	$V_{REFINT}/4$, $V_{REFINT}/2$, $V_{REFINT}*3/4$, V_{REFINT}, DAC3_OUT0 DAC0_OUT1	$V_{REFINT}/4$, $V_{REFINT}/2$, $V_{REFINT}*3/4$, V_{REFINT}, DAC3_OUT1 DAC1_OUT0	$V_{REFINT}/4$, $V_{REFINT}/2$, $V_{REFINT}*3/4$, V_{REFINT}, DAC3_OUT0 DAC1_OUT0	$V_{REFINT}/4$, $V_{REFINT}/2$, $V_{REFINT}*3/4$, V_{REFINT}, DAC3_OUT1 DAC1_OUT1
CMP outputs connected to I/Os	PA0 PA6 PA11 PB8 PF4	PA2 PA7 PA12 PB9	PB7 PB15 PC2	PB1 PB6 PB14	PA9 PC7	PC6 PA10	PC8 PA8	PA13 PA14
CMP outputs connected to EXTI	•							
CMP outputs connected to TRIGSEL	•							
CMP outputs connected to NVIC	•							
CMP outputs connected to internal signals	TIMER0, TIMER1, TIMER2, TIMER3, TIMER4, TIMER7, TIMER19, LPTIMER, HRTIMER							
CMP outputs connected to internal signals	BREAK0(TIMER0, TIMER7, TIMER14, TIMER15, TIMER16, TIMER19)							
	BREAK1(TIMER0, TIMER7, TIMER19)							

2.2 Inner hysteresis and propagation delay

As illustrated in ***Figure 2-2. GD32G5x3 CMP inner hysteresis illustration***, programmable inner hysteresis voltage V_{hyst} can be realized in GD32G5x3 CMP, preventing wrong output logic due to input signal noise. As shown in ***Table 2-2. GD32G5x3 CMP inner hysteresis parameter(1)***, HST[2:0] of CMPy_CS register is used to configure inner hysteresis voltage of CMPy (y = 0..7).

Figure 2-2. GD32G5x3 CMP inner hysteresis illustration

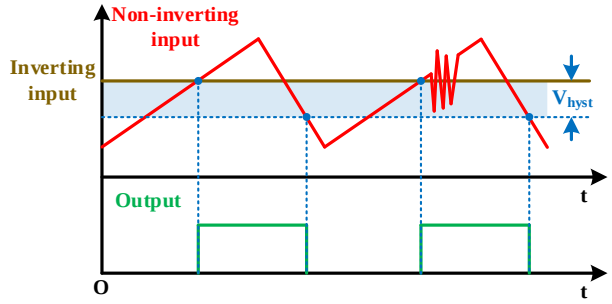


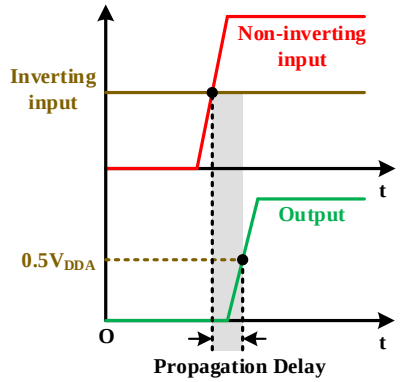
Table 2-2. GD32G5x3 CMP inner hysteresis parameter(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hyst}	Hysteresis Voltage	CMPxHST[2:0] = 000	—	0	—	mV
		CMPxHST[2:0] = 001	6.8	8.8	15.1	
		CMPxHST[2:0] = 010	13.6	17.6	30.4	
		CMPxHST[2:0] = 011	20.4	26.5	46	
		CMPxHST[2:0] = 100	25.7	35.5	62.1	
		CMPxHST[2:0] = 101	28.8	44.6	78.9	
		CMPxHST[2:0] = 110	30.9	53.9	96.6	
		CMPxHST[2:0] = 111	32.5	63.3	116.3	

(1) Value guaranteed by design, not 100% tested in production.

As illustrated in ***Figure 2-3. CMP propagation delay illustration***, propagation delay of CMP is defined as total time betweeen input voltage exceeds comparing voltage threshold and output voltage signal exceeds $0.5V_{DDA}$.

Figure 2-3. CMP propagation delay illustration



Typical propagation delay of GD32G5x3 CMP is 35ns, as shown in ***Table 2-3. GD32G5x3 CMP propagation delay***, while common comparator like LM393 suffers several-hundred ns propagation delay.

Table 2-3. GD32G5x3 CMP propagation delay(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_D	Propagation delay for 200mV step with 100 mV overdrive	50pF load on output	—	35	—	ns

(1) Value guaranteed by sample, not 100% tested in production.

Table 2-4. GD32G5x3 CMP consumption(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA(CMP)}$	Current consumption from V_{DDA}	Static	—	433	436	uA
		With 50 kHz ±100 mV overdrive square signal	—	392	—	

(1) Value guaranteed by design, not 100% tested in production.

As for CMP design, conflicts naturally exist between propagation delay and consumption. GD32G5x3 CMP optimizes propagation delay and curent consumption simutaneously, with ***Table 2-4. GD32G5x3 CMP consumption*** provided.

2.3 Inducments of static offset error

Static offset error is a key index about CMP threshold accracy. For example, if 1.65V is on inverting input of CMP with ±30mV static offset error, the voltage threshold of CMP non-inverting input causing CMP output inverts won't be fixed at 1.65V, varying from 1.62V~1.68V (Inner hysteresis voltage is ignored for simplicity).

Based on various source connections of inverting inputs of GD32G5x3 CMP，static offset error includes CMP itself offset error, and also it can include:

- DAC output offset error, with inverting input connected to DAC.
- Voltage scaler offset error, with inverting input connected to voltage scaler.
- External voltage reference offset error, with inverting input connected to I/O.

Table 2-5. GD32G5x3 CMP offset voltage illustrates GD32G5x3 CMP offset error.

Table 2-5. GD32G5x3 CMP offset voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{offset}	Offset error	Full VDDA voltage range, full temperature range	—	-3 ~ 4	—	mV

(1) Value guaranteed by design, not 100% tested in production.

2.3.1 Inverting input connected to DAC

In this case, static offset error includes CMP offset error and DAC offset error.

DAC output buffers are integrated in DAC0 and DAC1 of GD32G5x3 for saving external operational amplifier, which can be enable or disable flexibly.

Please refer to 'GD32G5x3 Datasheet' for original offset error of DAC and calibrated offset error of DAC(Offsetcal) with output buffer enabled.

2.3.2 Inverting input connected to voltage scaler

In this case, static offset error includes CMP offset error and voltage scaler offset error that is shown in ***Table 2-6. GD32G5x3 voltage scaler offset voltage***。

Table 2-6. GD32G5x3 voltage scaler offset voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SC}	Scaler offset voltage	—	—	3.3	10	mV

(1) Value guaranteed by design, not 100% tested in production.

Enable SEN bit and BEN bit of CMPy_CS register for using GD32G5x3 voltage scale; Then, configure MSEL[2:0] of CMPy_CS register (y = 0..7) and set 1/4, 1/2, 3/4 V_{REFINT} or V_{REFINT} refernece voltage to CMP inverting input. V_{REFINT} is internal 1.2V band-gap reference voltage for CMP and ADC.

2.3.3 Inverting input connected to external voltage

In this case, external DC source and resistor divider circuit sends comparing voltage to I/O pin，and thus static offset error includes CMP offset error and divider output offset error。Band-gap reference voltage can be used for supplying divider for high accuracy, which can also supply VREFP of ADC.

2.4 Calibration of static offset error

Based on Section, as for the case that inverting input is connected to inner DAC output, negative effects about static offset error can be suppressed via calibration as the following steps:

- Turn off inner hysteresis function.
- CMP non-inverting input is connected to I/O pin, which is externally supplied with the designed voltage threshold from DC source.
- CMP inverting input is connected to inner DAC output.
- Increase DAC digital value from zero slowly; when CMP output inverts, record the first corresponding DAC digital value.
- Then, decrease DAC digital value to zero slowly; when CMP output inverts again, record

the second corresponding DAC digital value.

- Calibrated DAC digtal value for the designed voltage threshold is the average on the first and the second DAC digital value.

After calibration, turn on inner hysteresis function:

- When input voltage on non-inverting pin exceeds the designed threshold voltage, CMP output changes from low to high level.
- When input voltage on non-inverting pin drops under that the designed threshold voltage substracts inner hysteresis voltage, CMP output changes from high to low level.

In other word, change input voltage on non-inverting pin slowly, and record input voltage value when CMP output changes from high to low level, then calibrated inner hysteresis voltage that the designed voltage threshold substracts the recorded value can be obtained.

3 Application Cases

3.1 Protection and CMP

In digital switching-mode power supply and motor control applications, serious fault protections like short protection and surge voltage protection have very strict requirements for protection action time, from fault signal generation to predetermined system safety state.

As for MCU software protection, judge system protection on/off with ADC value in fixed-frequency software interrupt. In other word, additional tasks exist between real fault generation and protection action, including ADC samping and hold-on, software interrupt instant error, other tasks interference, which restricts software protection speed.

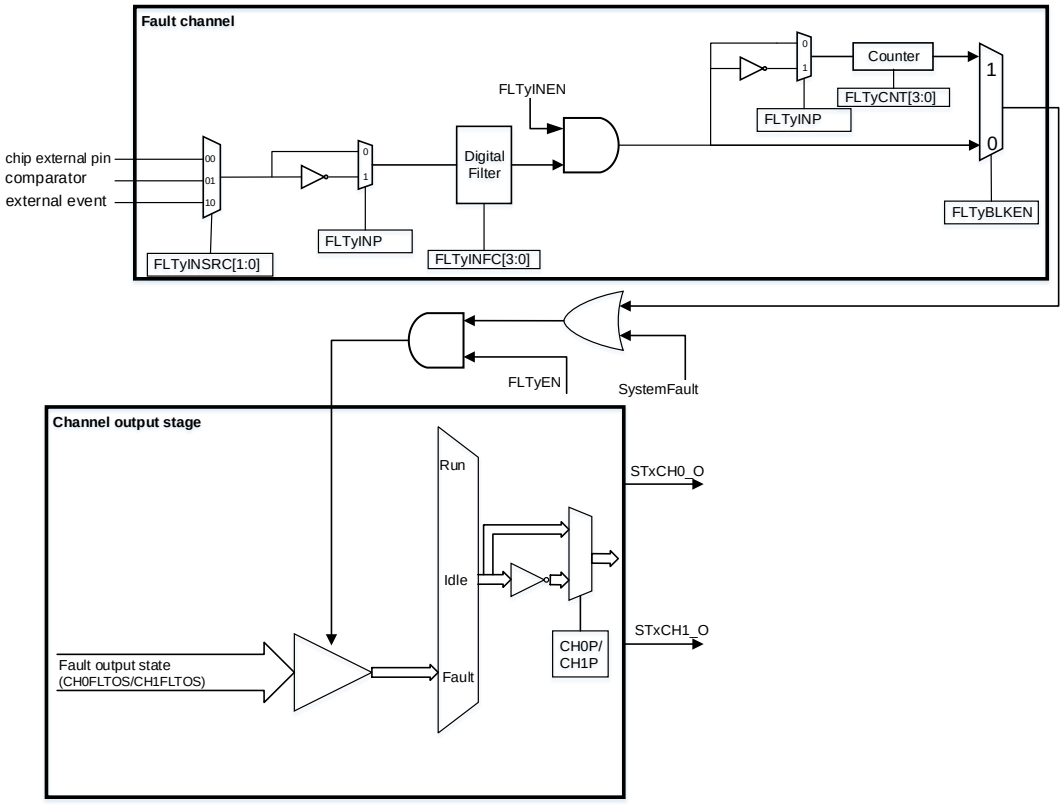
Therefore, hardware protection is necessary compensation for software protection, in order to realize reliable system protection.

In this section, system protection is realized via GD32G5x3 CMP and HRTIMER fault input.

3.1.1 HRTIMER fault input

Figure 3-1. GD32G5x3 fault input block diagram shows GD32G5x3 HRTIMER fault input system block diagram.

Figure 3-1. GD32G5x3 fault input block diagram



Fault input channel can receive three kinds of fault sources:

- Fault event from inner CMP output or digital input pin.
- System fault: signals coming from inside the MCU, for example the Cortex®-M33-lockup signal.
- fault event from extern event y (y=0…9).

Table 3-1. Fault channel mapping

Fault channel	FLTyINSRC = 00 (chip external pin)	FLTyINSRC = 01 (internal signal)	FLTyINSRC = 10 (external event)
Fault channel 0	PA12	Comparator 1	external event 0
Fault channel 1	PA15	Comparator 3	external event 1
Fault channel 2	PB10	Comparator 5	external event 2
Fault channel 3	PB11	Comparator 0	external event 3
Fault channel 4	PB0/PC7	Comparator 2	external event 4
Fault channel 5	PC10	Comparator 4	external event 5
Fault channel 6	PC3	Comparator 6	external event 6
Fault channel 7	PC4	Comparator 7	external event 7

Basic configuration about fault input channel y (y = 0…7) can be realized via HRTIMER_FLTINCFG0 and HRTIMER_FLTINCFG1 registers.

- Configure fault input channel y connection via FLTyINSRC bit, as shown in ***Table 3-1. Fault channel mapping***.
- Configure polarity of fault signal in fault input channel y via FLTyINP bit: if FLTyINP = 0, fault signal is active-low; if FLTyINP = 1, fault signal is active-high.
- Enable fault input channel y via FLTyINEN bit: all channels can be enabled at the same time.
- Write FLTyINPROT bit once time, and then FLTyINEN bit, FLTyINP bit, FLTyINSRC bit and FLTyINFC [3:0] bit region can be protected. Let FLTyINPROT=1, and all the aforementioned bits are read only.

Table 3-2. Fault input channel digital filter configuration

FLTyINFC[3:0]	f_{SAMP} (Digital filter sampling frequency)	N (After N input events, digital output flips)
0000	No filter	
0001	$f_{HRTIMER\_CK}$	2
0010	$f_{HRTIMER\_CK}$	4
0011	$f_{HRTIMER\_CK}$	8
0100	$f_{HRTIMER\_FLTFCK}$ /2	6
0101	$f_{HRTIMER\_FLTFCK}$ /2	8
0110	$f_{HRTIMER\_FLTFCK}$ /4	6
0111	$f_{HRTIMER\_FLTFCK}$ /4	8
1000	$f_{HRTIMER\_FLTFCK}$ /8	6

FLTyINFC[3:0]	f_{SAMP} (Digital filter sampling frequency)	N (After N input events, digital output flips)
1001	$f_{HRTIMER\_FLTFCK}$ /8	8
1010	$f_{HRTIMER\_FLTFCK}$ /16	5
1011	$f_{HRTIMER\_FLTFCK}$ /16	6
1100	$f_{HRTIMER\_FLTFCK}$ /16	8
1101	$f_{HRTIMER\_FLTFCK}$ /32	5
1110	$f_{HRTIMER\_FLTFCK}$ /32	6
1111	$f_{HRTIMER\_FLTFCK}$ /32	8

In addition, digital filter function is intergrated in the fault input channels, to prevent fault trigger caused by input signal noise. As shown in ***Table 3-2. Fault input channel digital filter configuration***, digital filter parameters of fault input channel y (y = 0..7) can be set via FLTyINFC[3:0] bit region of HRTIMER_FLTINCFG0 and HRTIMER_FLTINCFG1 registers, where ratio between clock frequency of HRTIMER $f_{HRTIMER\_CK}$ and clock frequency of digital filter $f_{HRTIMER\_FLTFCK}$ can be decided by FLTFDIV[1:0] bit region, i.e. $f_{HRTIMER\_FLTFCK} = f_{HRTIMER\_CK}/2^{FLTFDIV[1:0]}$.

Figure 3-2. Fault input channel and HRTIMER output stage

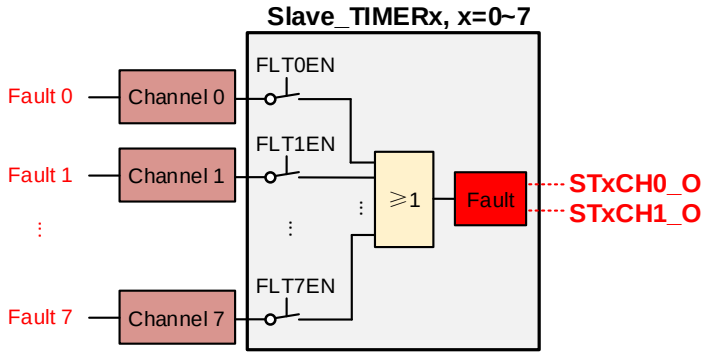


Figure 3-2. Fault input channel and HRTIMER output stage shows relationship between fault input y (y = 0..7) and HRTIMER(Slave_TIMERx, x=0…7):

- Every Slave_TIMERx has fault control register HRTIMER_STxFLTCTL: let FLTyEN=1, and fault input channel y is accepted; let FLTyEN=0, and fault input channel y is rejected. Protect FLTyEN (read only) bit via writing 1 to FLTENPROT bit one time.
- Configure Slave_TIMERx responses to fault input channel y; when fault event happens, output channels of Slave_TIMERx outputs STxCH0_O and STxCH1_O into predetermined voltage level; fault state is kept until software reset instruction (write 1 to STxCHyEN bit).
- Configure Slave_TIMERx responses to multiple fault input channels, if one of these channels exists a fault event, fault state will effect in Slave_TIMERx (Logic: OR).

3.1.2 CMP output connected to fault input

As shown in ***Figure 3-3. Short protection: GD32G5x3 CMP connection***, GD32G5x3 HRTIMER fault input can directly connect to inner CMP module original output, decreasing fault signal propagation delay for the best.

Set fault input channel y connected to inner CMP output via letting FLTyINSRC=1(y = 0…7) of HRTIMER_FLTINCFG0 and HRTIMER_FLTINCFG1 registers, as shown in ***Table 3-1. Fault channel mapping***.

As shown in ***Figure 3-3. Short protection: GD32G5x3 CMP connection***, DC output short protection can be realized via GD32G5x3 CMP and HRTIMER fault input with optimal response time, which refers to ***Table 3-3. GD32G5x3 CMP and fault protection response time***. Besides, inner hysteresis voltage of CMP and inner digital filter function can prevent fault trigger of short protection.

Figure 3-3. Short protection: GD32G5x3 CMP connection

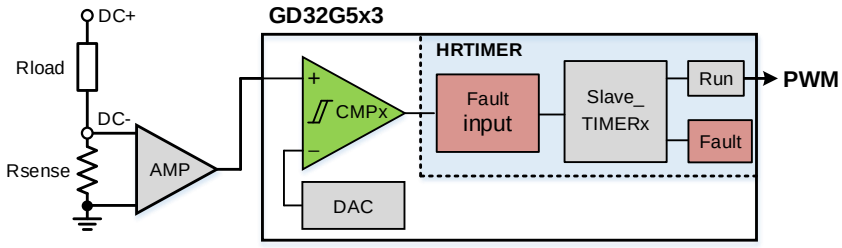


Table 3-3. GD32G5x3 CMP and fault protection response time(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from comparator CMPx_IPx input pin to HRTIMER_STxCHy output pin(30pF load)	—	—	35	ns

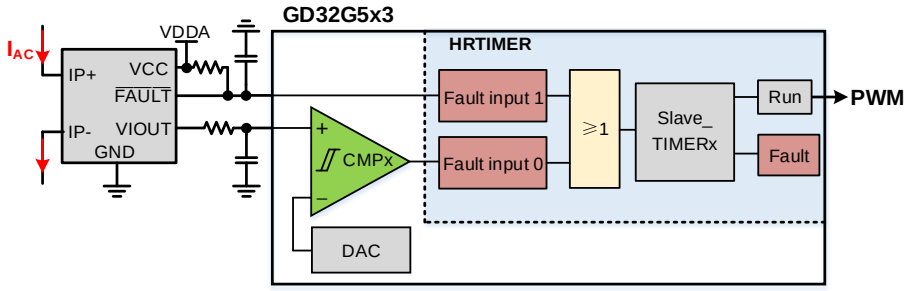
(1) Value guaranteed by design, not 100% tested in production.

3.1.3 Multiple protection

Varying from inner fault signal generated by MCU CMP output, outer fault signal may come from outer device that has integrated fault detection and outer hardware protection circuit. Therefore, inner and outer fault signals can be used at the same time to realize multiple protections with MCU software protection.

As shown in ***Figure 3-4. Multiple over current protection using inner and outer signals***, inner fault signal from GD32G5x3 CMP output and outer fault signal from hall-effect current sensor can be used at the same time for AC over-current protection: configure fault channels connected to inner and outer fault singals and HRTIMER output stage responses these fault channels (Logic: OR).

Figure 3-4. Multiple over current protection using inner and outer signals



3.2 Cycle-by-cycle protection

Cycle-by-cycle(CBC) protection is widely applied in AC-DC、DC-DC power applications. As shown in ***Figure 3-5. CBC protection theory***, in the current switching cycle, PWM signal of main switch is banned when real current exceeds set value Iref; when the novel switching cycle begins, PWM signal recovers. Due to system delay of gate drivers, sampling and so on, real peak current poing lags behind set value point.

Figure 3-5. CBC protection theory

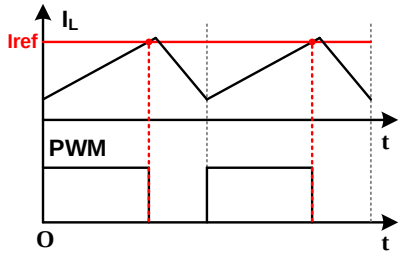


Figure 3-6. CBC: GD32G5x3 CMP connection

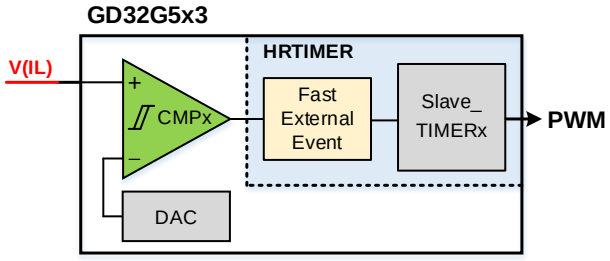


Table 3-4. GD32G5x3 CMP and fast external event response time(1)

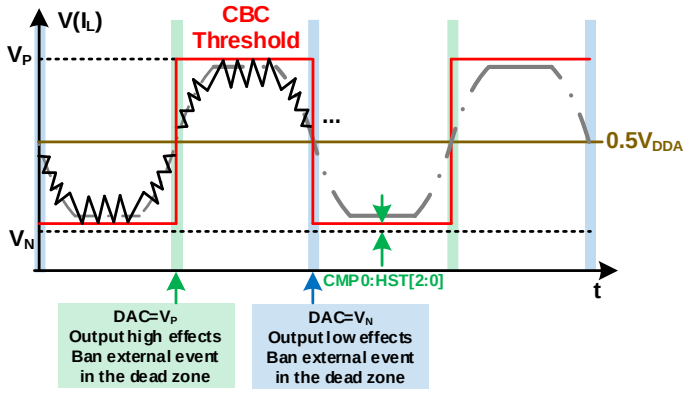
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from comparator CMPx_IPx input pin to HRTIMER_STxCHy output pin(30pF load)	—	—	35	ns

(1) Value guaranteed by design, not 100% tested in production.

CBC protection can be realized via GD32G5x3 CMPand HRTIMER fast external event for optimal response time, as shown in ***Figure 3-6. CBC: GD32G5x3 CMP connection***. CMP

ouput internally connects to HRTIMER fast external event module; in the current switching cycle, fast external event responses to CMP output signal that current exceeds Iref and PWM is banned; PWM is recovered when the novel switching cycle begins; total response time refers to ***Table 3-4. GD32G5x3 CMP and fast external event response time***(1).

Figure 3-7. CBC: configuration in AC zero dead zone



As for bridgeless PFC application, various CBC thresholds and various CMP output logic are obtained in AC positive and negative cycles. However, CBC protection can be realized via single GD32G5x3 CMP, as shown in ***Figure 3-7. CBC: configuration in AC zero dead zone***: In the AC zero dead zone，modify DAC value and CMP configuration correspongdingly; AC ero dead zone is far less than AC power cycle; it's easy for DAC to reach the steady state in the AC zero dead zone, as shown in ***Table 3-5. GD32G5x3 1MSPS DAC setting time***(1).

Table 3-5. GD32G5x3 1MSPS DAC setting time(1)

Symbol	Description	Conditions		Min	Typ	Max	Unit
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ	±1 LSB	—	1.6	2.9	µs
			±2 LSB	—	1.55	2.85	
			±4 LSB	—	1.48	2.8	
			±8 LSB	—	1.4	2.75	
		Normal mode, DAC output buffer OFF, ±1LSB CL=10 pF		—	2	3.5	

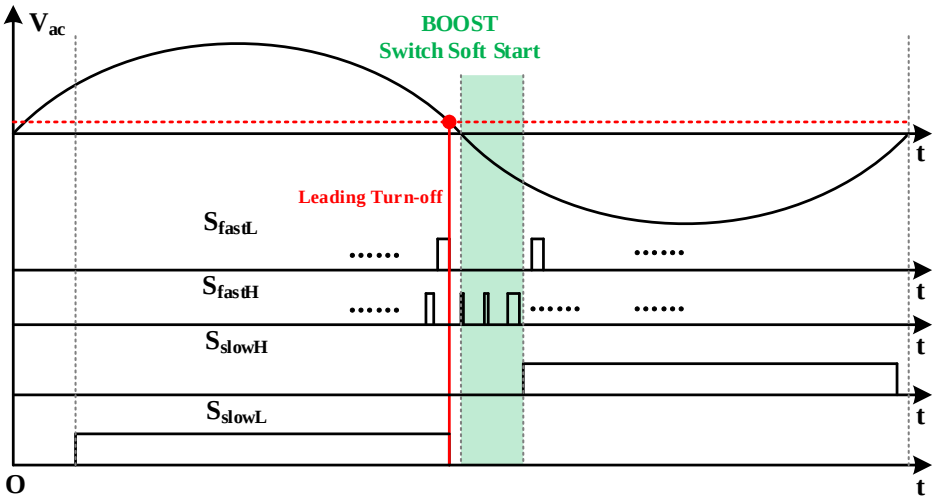
(1) Value guaranteed by design, not 100% tested in production.

3.3 AC zero detection

Totem-pole PFC topology is one of the main choices for medium to high power AC-DC application; AC zero detection and management is one of the main control challenges for Totem-pole PFC. Take the transition process from AC positive cycle to AC negative cycle as example; in order to suppress AC current peak at AC voltage zero crossing, all switches should be turned off before entering into the AC negative cycle; when the AC negative cycle begin, current peak is suppressed by a duty soft start process of boost switch, as shown in ***Figure 3-8. Suppress AC current peak at AC zero crossing for Totem-pole PFC***. In other

word, zero crossing signal should lead to real AC zero crossing for leading turn-off; otherwise, zero dead zone will be larger with poor THD, and soft start process will be delay.

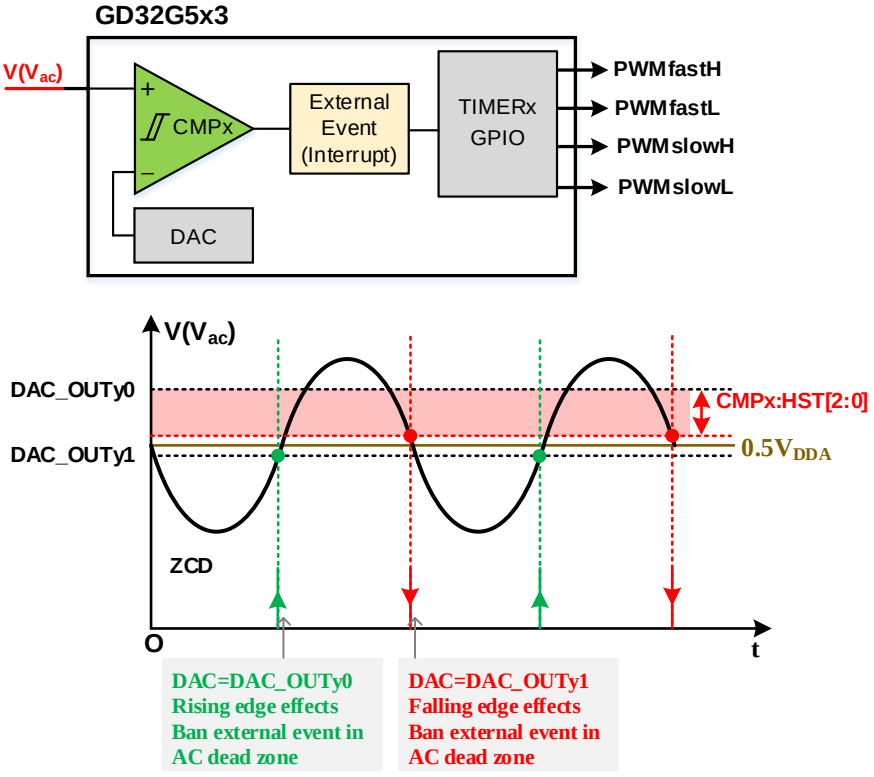
Figure 3-8. Suppress AC current peak at AC zero crossing for Totem-pole PFC



As shown in ***Figure 3-9. Totem-pole PFC zero detection via GD32G5x3 CMP***, AC zero detection can be realized via single GD32G5x3 CMP with cooperation between CMP and HRTIMER and configuration adjustment in the AC zero dead zone, similar to ***Figure 3-7. CBC: configuration in AC zero dead zone***.

With the help of programmable inner hysteresis voltage of GD32G5x3 CMP and DAC value, AC zero dead zone can be optimized conveniently and THD can be improved.

Figure 3-9. Totem-pole PFC zero detection via GD32G5x3 CMP



4 Revision history

Table 4-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov.12 2024

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