GigaDevice Semiconductor Inc.

GD32E501 Hardware Development Guide

Application Note
AN101

Revision 1.2

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1. Introduction

The article is specially provided for developers of 32-bit general-purpose MCU GD32E501 series based on Arm® Cortex®-M33 architecture. It provides an overall introduction to the hardware development of GD32E501 series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32E501 series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32E501 series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32E501 series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32E501 series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32E501 series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32E501 series.
6. Reference circuit and PCB Layout design, mainly introduces GD32E501 series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32E501 series.

This document also satisfies the minimum system hardware resources used in application development based on GD32E501 series products.

Table 1-1. Applicable Products

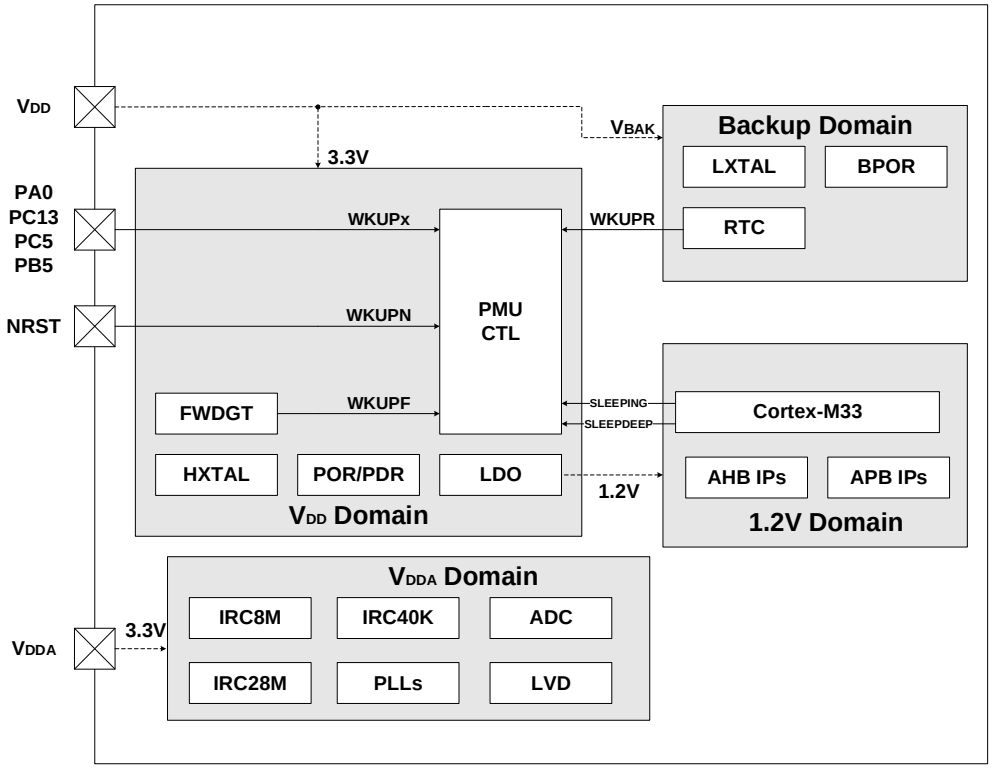
Type	Part Numbers
MCU	GD32E501xx series

2. Hardware design

2.1. Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32E501 series products is 1.8 V ~ 3.63V. As shown in ***Figure 2-1. GD32E501 Power supply overview***, the GD32E501 series device has three power domains, including the V_{DD} / V_{DDA} domain, 1.2V domain and backup domain. The V_{DD} / V_{DDA} domain is directly powered by the power supply, and an LDO is embedded in the V_{DD} / V_{DDA} domain to power the 1.2V domain. The backup domain is directly powered by the V_{DD}. When the V_{DD} is powered off, the power supply to the backup domain is lost. There is a separate power supply V_{DDIO} for PB12 ~ PB15 and PC6 ~ PC9 pins.

Figure 2-1. GD32E501 Power supply overview



LVD: Low Voltage Detector
LDO: Voltage Regulator
BPOR: V_{BAK} Power On Reset
POR: Power On Reset
PDR: Power Down Reset

2.1.1. Backup domain

The backup domain power supply voltage range is 1.8 V~3.63 V. In order to ensure the content of the Backup domain register and RTC supply, when the V_{DD} is turned off. Once the V_{DD} power is turned off, all Backup domain data and registers will be reset.

Note: GD32E501 series MCU has no V_{BAT} pin, so it cannot use RTC and Backup domain to work normally after power failure.

2.1.2. V_{DD} / V_{DDA} domain

The V_{DD} / V_{DDA} power domain includes two parts: V_{DD} domain and V_{DDA} domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two should not exceed 300mV (the internal V_{DDA} and V_{DD} of the chip are connected through a back-to-back diode). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and the corresponding V_{SSA} is connected to V_{SS} through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. GD32E501 is internally integrated with V_{REFP} pin specially designed for independent power supply of ADC (external power supply: 2.4 V ≤ V_{REFP} ≤ V_{DDA}).

- V_{DD} power supply range: 1.8 V ≤ V_{DD} ≤ 3.63 V
- If ADC function is not used, V_{DDA} power supply range (1.8 V ≤ V_{DD} ≤ 3.63 V); If ADC function is used, V_{DDA} power supply range (2.4 V ≤ V_{DD} ≤ 3.63 V).

2.1.3. V_{REF} domain

In order to improve the performance of ADC / DAC, a precise internal voltage reference circuit is integrated in the chip of GD32E501 series products, which provides accurate reference voltage for ADC / DAC, and can also supply external power to V_{REFP} pin. Typical value of internally generated V_{REF}: 2.5V, the precision reference is enabled by set the VREF_EN bit in SYSCFG_CFG2 register. If VREF_EN bit is not set, V_{REFP} pin can also be powered by external power supply or V_{DDA}, at this time, the VREF_EN bit in SYSCFG_CFG2 register must keep 0.

It is recommended that the V_{REFP} pin be externally connected with a 10nF + 1uF ceramic capacitor to the ground. If conditions do not allow, at least one 100nF ceramic capacitor should be connected to the ground.

2.1.4. V_{DDIO} domain

GD32E501 series products supply power through V_{DDIO} for the eight pins PB12 ~ PB15 and PC6 ~ PC9. The power supply range of V_{DDIO} is 1.2 V to 3.63 V, which meets the flexible demand of MCU and chips working in different power domains.

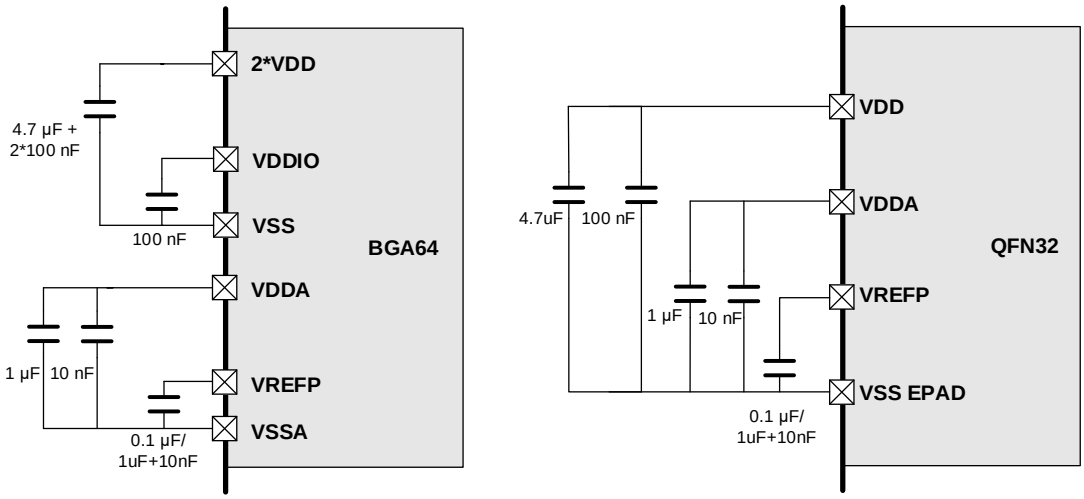
It should be noted that when the V_{DD} is not powered on, do not supply power to the V_{DDIO} separately. When the V_{DD} is powered on, do not leave the V_{DDIO} suspended.

2.1.5. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF).
- The VDDA pin must be connected with an external capacitor (10nF + 1uF ceramic capacitor is recommended).
- The V_{REF} voltage can be generated internally or directly connected to V_{DDA}, and a 100nF or a 10nF + 1uF ceramic capacitor should be connected between the VREFP pin and ground.
- The external part of VDDIO pin needs to be connected with 100nF ceramic capacitor to ground.

Figure 2-2. GD32E501 Recommended Power Supply Design



Note:

1. All decoupling capacitors must be placed close to the corresponding VDD, VDDA, VREFP, VDDIO pins of the chip.
2. The recommended VREFP selection is generated internally, and can also be provided externally according to the customer's actual application.
3. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
4. BGA64: VSSA and VREFN are connected internally.
5. QFN32: VDD and VDDIO are connected internally, VSS, VSSA and VREFN are connected internally.

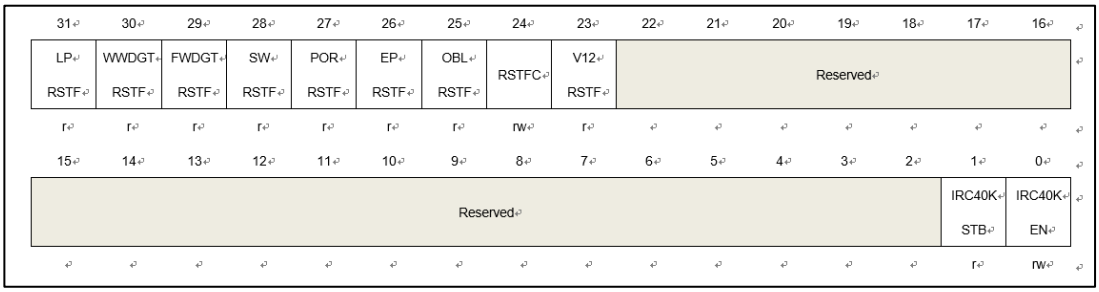
2.2. Power Detection and Reset

In this section, the default VDD and VDDA pins remain connected and are powered by the same power supply.

GD32E501 series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain when the power is turned on.

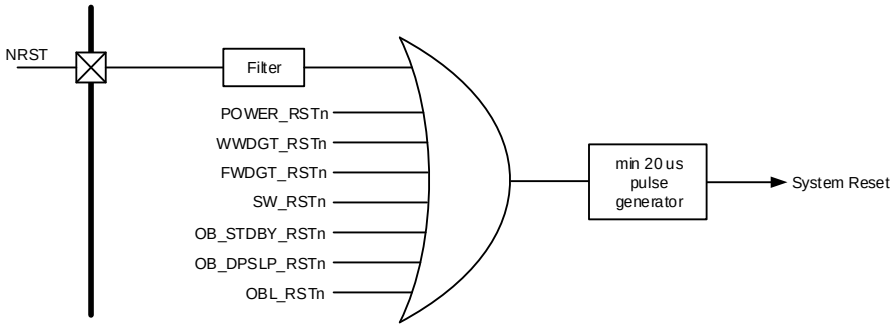
The MCU reset source can be searched by the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register:

Figure 2-3. RCU_RSTSCK Register



MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20μs.

Figure 2-4. System Reset Circuit

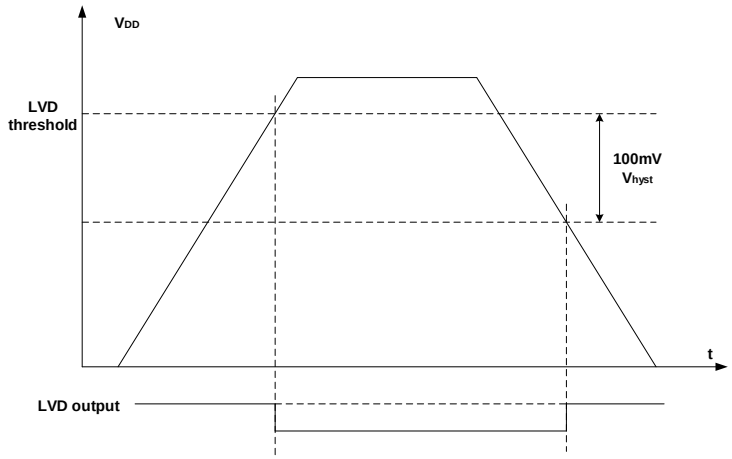


2.2.1. LVD

The function of LVD is to detect whether the V_{DD} supply voltage is lower than the low voltage detection threshold (2.1 V ~ 3.1 V), which is configured by the LVDT[2:0] bit in the power control register (PMU_CTL). LVD is enabled by LVDEN setting. The LVDF bit in the power supply status register (PMU_CS) indicates whether a low voltage event occurs. This event is connected to the 16th line of EXTI. The user can generate a corresponding interrupt by configuring the 16th line of EXTI. (LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16). The hysteresis voltage Vhyst value is 100 mV.

LVD application: When the MCU power supply is subject to external interference, such as a voltage drop, we can set the low voltage detection threshold (the threshold is greater than the PDR value) through LVD. Once it falls to the threshold, the LVD interrupt is turned on, which can be used in the interrupt function. Set operations such as soft reset to avoid other exceptions from the MCU.

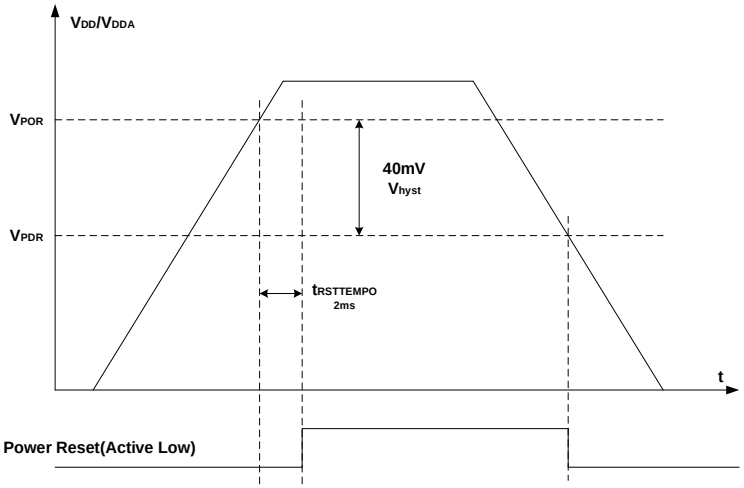
Figure 2-5. LVD Threshold Waveform



2.2.2. POR / PDR

The chip integrates a POR / PDR (power-on / power-down reset) circuit to detect V_{DD} / V_{DDA} and generate a power reset signal to reset the entire chip except the backup domain when the voltage is lower than a certain threshold. V_{POR} is the threshold voltage of power-on reset, and the typical value is about 1.71 V, and V_{PDR} is the threshold voltage of power-down reset, and the typical value is about 1.67 V. The value of the hysteresis voltage V_{hyst} is about 40 mV. It should be noted that the GD32E501 series reset pin only has the input function, and the low level generated by the system reset cannot be seen from the reset pin.

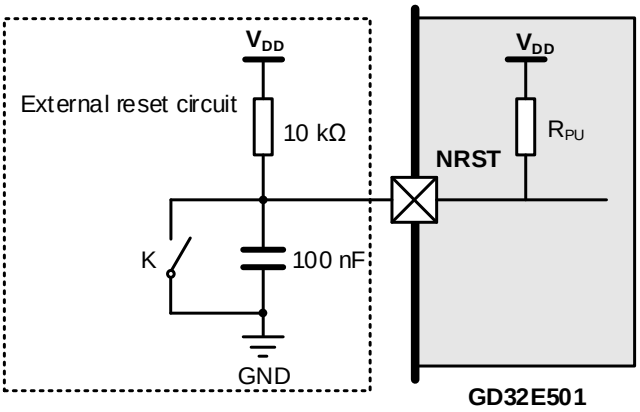
Figure 2-6. Power-on/power-down reset waveforms



2.2.3. NRST Pin

For the MCU's NRST pin, to prevent accidental reset triggering, it is recommended to place a capacitor (typically 100 nF) on the NRST pin.

Figure 2-7. Recommend External Reset Circuit

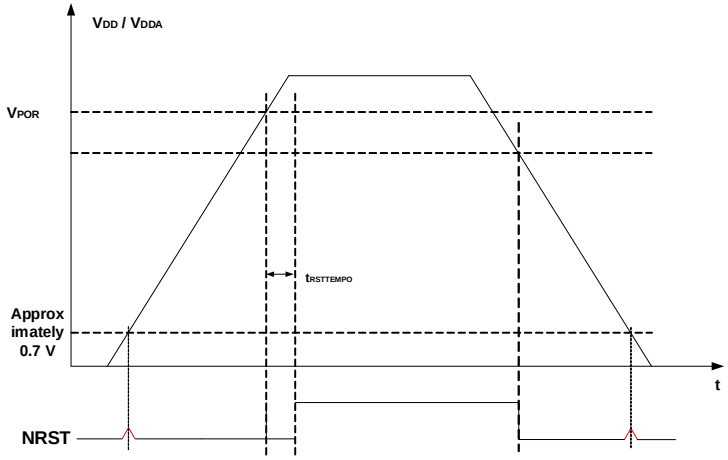


Note:

1. Internal pull-up resistance R_{PU} = 40 kΩ. You are advised to use an external pull-up resistance of 10 kΩ to ensure that voltage interference does not cause chip abnormalities
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

Due to the threshold voltage characteristics of the MOS transistor, during the power-up and power-down process of the chip, when VDD / VDDA < 0.7 V, the internal pull-down MOS transistor of the chip will not pull down the NRST pin. Therefore, during the power-up and power-down process, when VDD / VDDA ≈ 0.7 V, a small pulse occurs, which does not affect the normal operation of the chip, as shown by the red pulse in ***Figure 2-8. The illustration of the pulse of the NRST pin power-up/down MOS transistor***.

Figure 2-8. The illustration of the pulse of the NRST pin power-up/down MOS transistor



Due to the difference in charge and discharge speeds, the duration of the pulse on the falling edge is slightly longer than that on the rising edge, both of which are at the

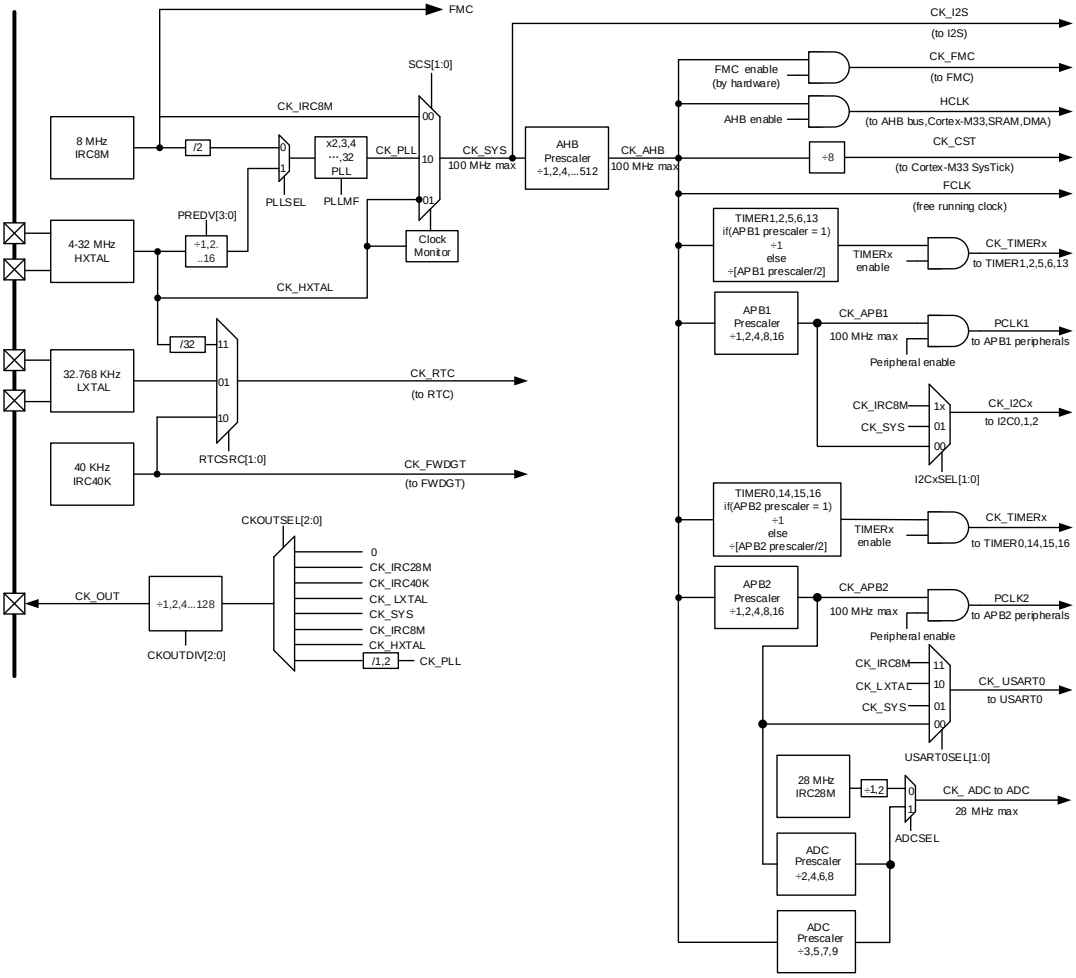
millisecond level.

2.3. Clock

GD32E501 series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

- 4-32 MHz external high-speed crystal oscillator (HXTAL)
- Internal 8 MHz RC oscillator (IRC8M)
- Internal 28 MHz RC oscillator (IRC28M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- Internal 40 kHz RC oscillator (IRC40K)
- PLL clock source can be selected from HXTAL or IRC8M.
- HXTAL clock monitor

Figure 2-9. GD32E501 Clock Tree



2.3.1. External high-speed crystal oscillator clock (HXTAL)

4-32MHz external high-speed crystal oscillator (passive crystal) can provide accurate main

clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSCIN, and OSCOUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-10. HXTAL External Crystal Circuit

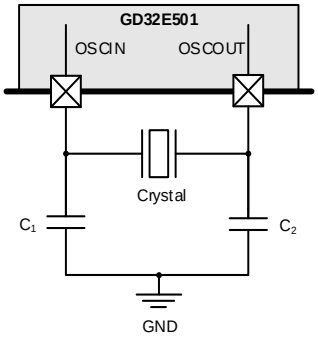
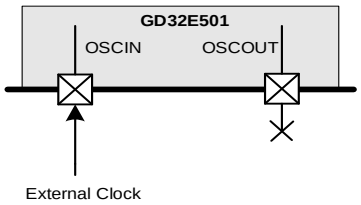


Figure 2-11. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSCIN, and OSCOUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC8M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}.
7. The traces connecting the resonator to the MCU clock pins may cause inconsistent

lengths of the traces connected to the OSCOUT and OSCIN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768KHz low-speed external crystal (passive crystal), which can provide a low-power and high-precision clock source for RTC(Package models below 48 pin do not have LXTAL pin). The RTC module of the MCU is equivalent to a counter. The accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-12. LXTAL External Crystal Circuit

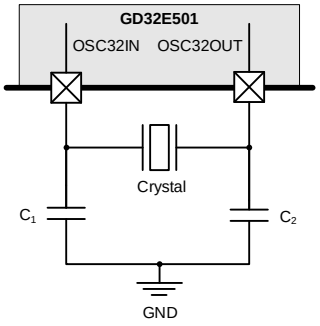
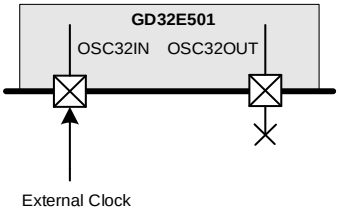


Figure 2-13. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32IN, and OSC32OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF ~ 7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and

C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.

2.3.3. Clock Output Capability (CKOUT)

GD32E501 series MCU can output clocks from 32kHz to 100MHz. Different clock signal outputs can be selected by configuring CKOUT0SEL[2:0] bit of clock register RCU_CFG0. The corresponding GPIO pin PA8 / PA9 needs to be configured for multiplexing function to output the selected signal.

Table 2-1. CKOUT0SEL[2:0] Control Bits

CKOUT0SEL[2:0]	Clock source
000	No Clock
001	CK_IRC28M
010	CK_IRC40K
011	CK_LXTAL
100	CK_SYS
101	CK_IRC8M
110	CK_HXTAL
111	CK_PLL or CK_PLL/2

2.3.4. HXTAL Clock Monitor (CKM)

Set the clock monitoring enable bit CKMEN in the clock control register RCU_CTL. The clock monitoring function can be enabled by HXTAL. This function needs to be enabled after HXTAL startup is delayed and disabled after HXTAL is stopped. Once HXTAL fails, HXTAL is automatically disabled, and the clock blocking flag CKMIF in the clock interrupt register RCU_INT is set, generating the HXTAL fault event. The interrupt raised by this failure is connected to the Arm® Cortex®-M33 non-maskable interrupt NMI.

Note: If HXTAL is selected as the system clock, PLL, or RTC clock source, the fault of HXTAL causes IRC8M to be selected as the system clock source. The PLL is automatically disabled and the RTC clock source needs to be reconfigured

2.4. Startup Configuration

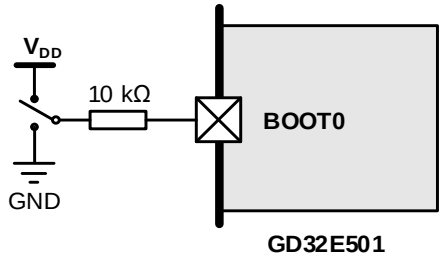
The GD32E501 series provides three boot modes, which can be selected by the user option byte BOOT1_n bit and the BOOT0 pin. When designing the circuit, run the user program, the BOOT0 pin cannot be suspended, it is recommended to go through a 10kΩ resistor to GND; To run the System Memory for program update, the BOOT0 pin should be connected high, and the option byte OB_USER[4] should keep BOOT1_n as 1 (at this time, the corresponding BOOT1 bit is 0). After the update is completed, the user program can be run only after BOOT0 is connected low and powered on; the SRAM execution program is mostly used in the debugging status.

The embedded Bootloader is stored in the system storage space for reprogramming the FLASH memory. In GD32E501 series, Bootloader can interact with the outside world through I2C0 (PB6 and PB7).

Table 2-2. BOOT mode

BOOT mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-14. Recommend BOOT0 Circuit Design



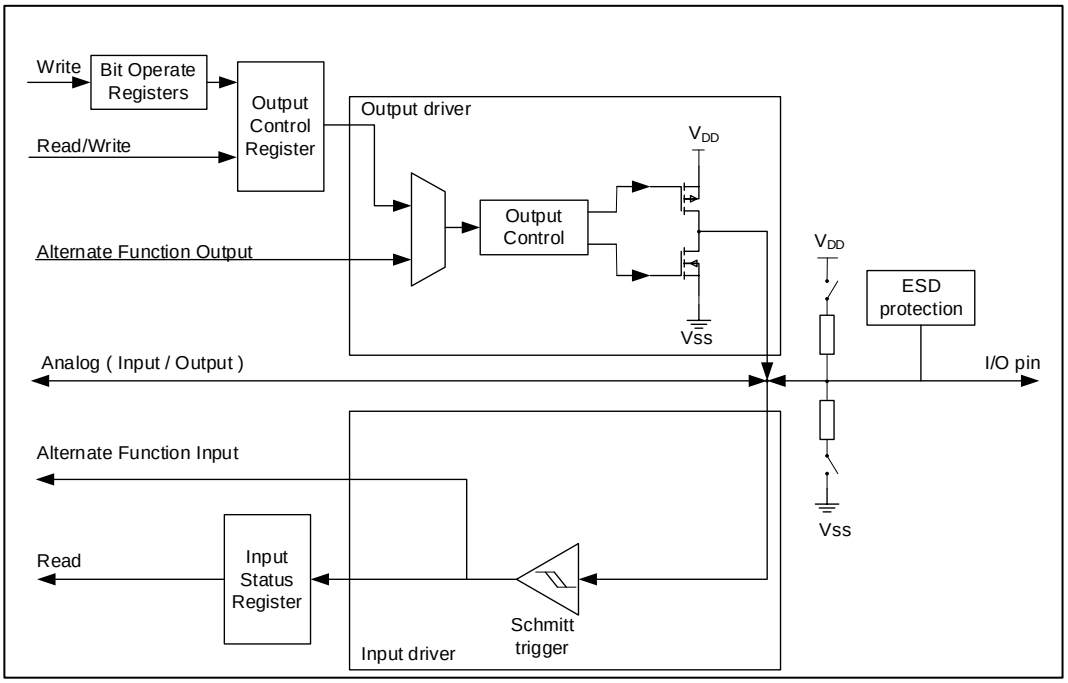
Note: After the MCU is running, if the BOOT state is changed, it will take effect after the system is reset. MCU.

2.5. Typical Peripheral Modules

2.5.1. GPIO Circuit

GD32E501 can support up to 55 general-purpose I/O pins (GPIO), which are PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD2, PF0 ~ PF1, PF4 ~ PF7; each pin can be independently configured through registers, the basic structure of the GPIO port is shown in the following figure ***Figure 2-15. Basic structure of standard IO***:

Figure 2-15. Basic structure of standard IO



Note:

1. The IO port is divided into 5V tolerant and non-5V tolerant. When using, pay attention to distinguish the IO port withstand voltage.
2. When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.
3. The eight pins PB12 ~ PB15, PC6 ~ PC9 have a separate power supply pin V_{DDIO}, and the power supply range is 1.2V to 3.63V.
4. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
5. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
6. The three IO ports of PC13, PC14, PC15 have weak drive capability and limited output current capability(about 3mA). When configured in output mode, their working speed cannot exceed 2MHz(Maximum load is 30pF).
7. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.
8. Non-5V tolerance I/O, external voltage over V_{DD}, may generate perfusion current

2.5.2. ADC Circuit

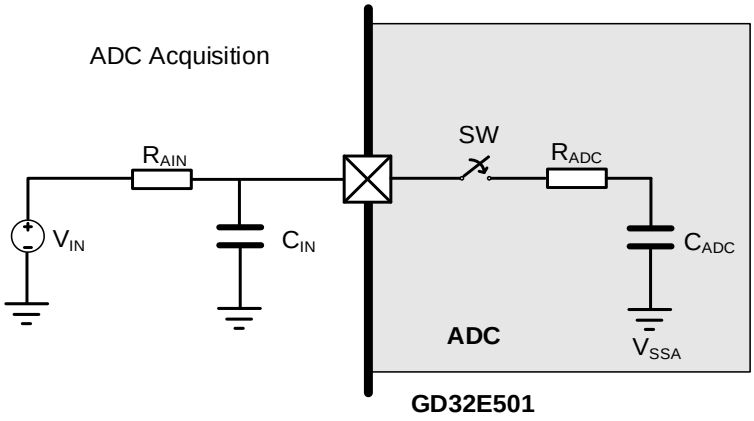
The GD32E501 integrates a 12-bit SAR ADC with up to 18 channels, which can measure 16 external and 2 internal signal sources. The internal signal is the temperature sensor channel

(ADC0_IN16), the internal reference voltage input channel (ADC0_IN17). Temperature sensors reflect temperature changes and are not suitable for measuring absolute temperature. If accurate temperature measurements are required, an external temperature sensor must be used. Internal reference voltage V_{REFINT} provides a stable voltage output (1.2V) to the ADC and is internally connected to ADC0_IN17.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin. It is recommended to place a small capacitor of 500pF.

Figure 2-16. ADC Acquisition Circuit Design



When f_{ADC} = 28MHz, the relationship between the input impedance and the sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, and select a larger value for the sampling period. When designing external circuits, try to reduce the input Impedance, if necessary, use the op amp to follow to reduce the input impedance.

Table 2-3. f_{ADC} =28MHz Relationship between sampling period and external input impedance

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (KΩ)
1.5	0.05	0.5
7.5	0.27	4.5
13.5	0.48	8.5
28.5	1.02	18.6
41.5	1.48	27.3
55.5	1.98	36.6
71.5	2.55	47.3
239.5	8.55	159.76

2.5.3. Internal temperature sensor calibration

GD32E501 series MCU is internally integrated with a temperature sensor, which is internally

connected to the ADC channel 16. The effective range of temperature measurement is -40°C to 105°C. The output voltage of the temperature sensor varies linearly with the temperature. To ensure accurate temperature measurement, ADC needs to be provided with an accurate, low-temperature drift reference voltage V_{REF}.

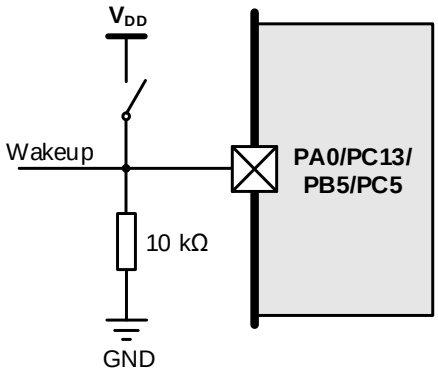
At the same time, due to different process offset, the offset of temperature curve will be different in different chips (up to 45°C). To solve this problem, GD32E501 series MCU provides an internal temperature sensor calibration method. The specific operation is to measure the temperature sensor sampling values at two standard temperatures during the production test phase of the chip, and store the two values in the FLASH. In practice, the two values can be read from FLASH, a straight line can be fitted, and then the actual temperature sampling value can be substituted to obtain a relatively accurate test temperature.

Note: There are differences in the standard calibration temperature values used by different MCU during the production test phase; The locations of the two standard temperature samples stored in FLASH during the production test stage also differ from MCU to MCU.

2.5.4. Standby mode wake-up circuit

The GD32E501 series supports three low-power modes, sleep mode, deep sleep mode and standby mode. The standby mode has the lowest power consumption and the longest wake up time. Wake up from Standby mode can be awakened by WKUP pin rising edge, a total of four WKUP pins, do not need to configure the corresponding GPIO, just configure the WUPENx bit in the PMU_CS register. The reference circuit design corresponding to WKUP wake up pin is shown in ***Figure 2-17. Recommend Standby external wake-up pin circuit design***.

Figure 2-17. Recommend Standby external wake-up pin circuit design



Note: In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.

2.6. Download the debug circuit

The GD32E501 series kernel supports only the SWD debugging interface and does not

support the JTAG interface. The standard SWD interface is a 5-pin interface, with two signal interfaces.

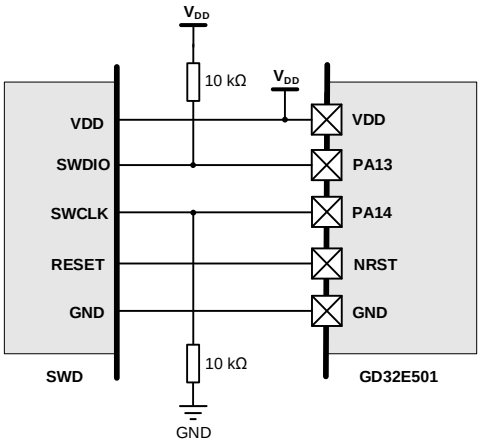
Note: After reset, the debug related ports are in input PU / PD mode, where:

PA13: SWDIO in pull-up mode.
PA14: SWCLK in pull-down mode.

Table 2-4. SWD download debug interface assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-18. Recommend SWD Wiring Reference Design

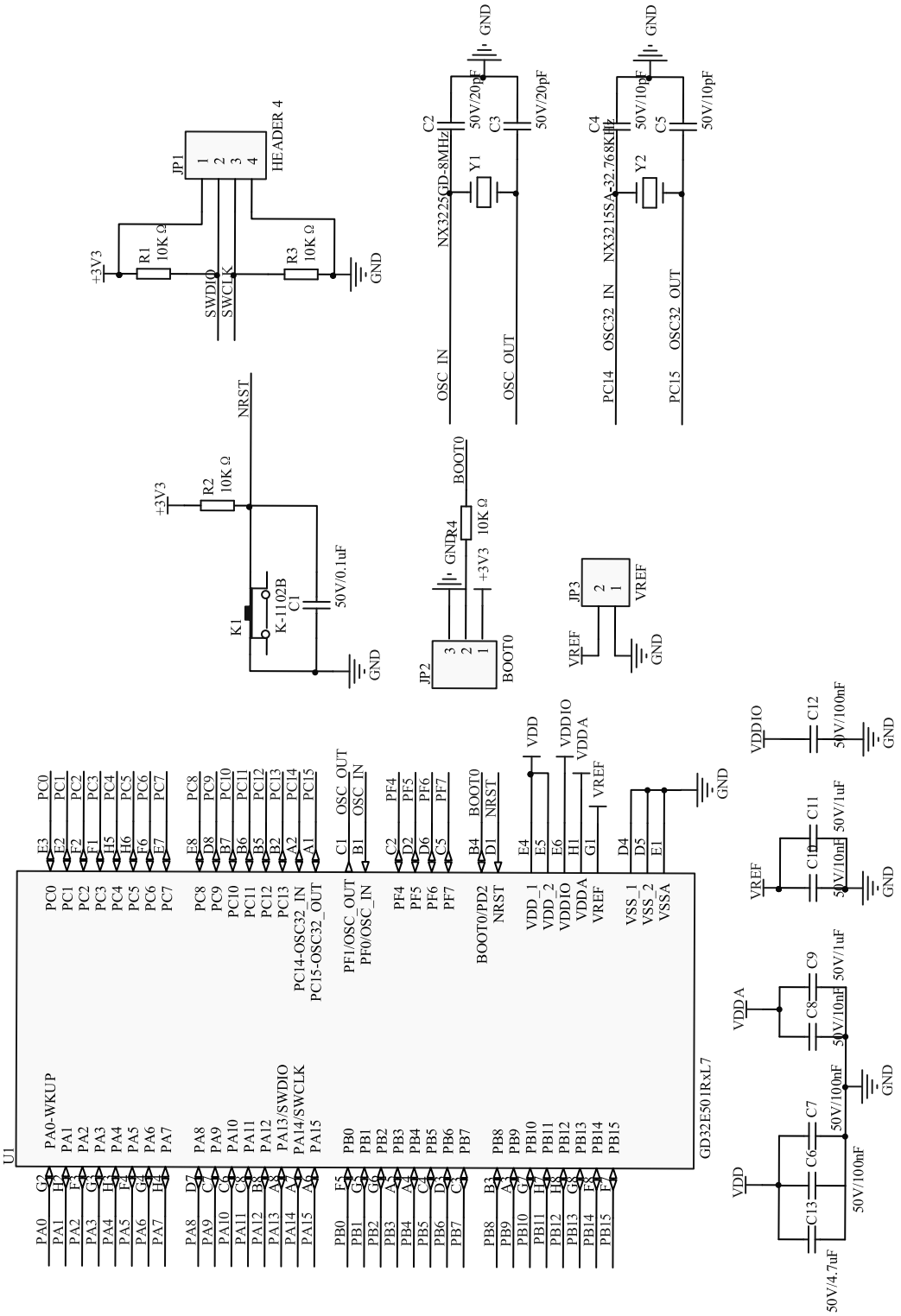


There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω~1KΩ resistor.

2.7. Reference Schematic Design

Figure 2-19. GD32E501 Recommend Reference Schematic Design



3. PCB Layout Design

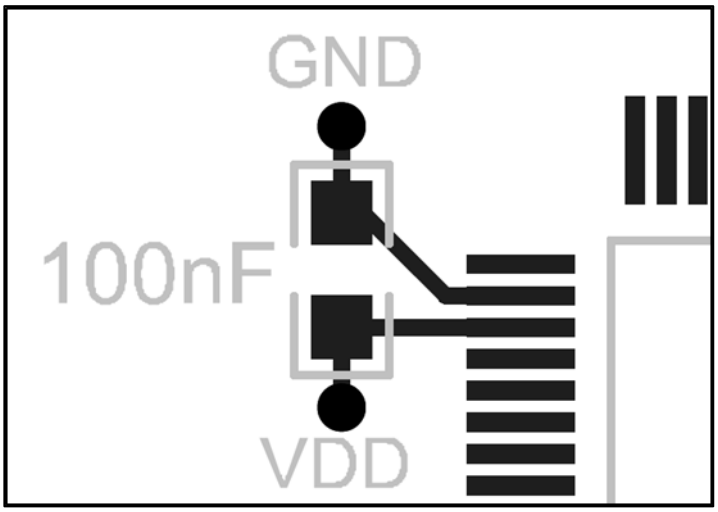
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32E501 series power supply has V_{DD}, V_{DDA}, V_{REFP}, V_{DDIO} and other power supply pins. Ceramic MLCC can be used for the 100nF decoupling capacitor, and the position should be as close to the power pin as possible. The power cable should be routed through the capacitor before reaching the MCU power pin. It is recommended to lay out a Layout in the form of Via near the capacitor PAD

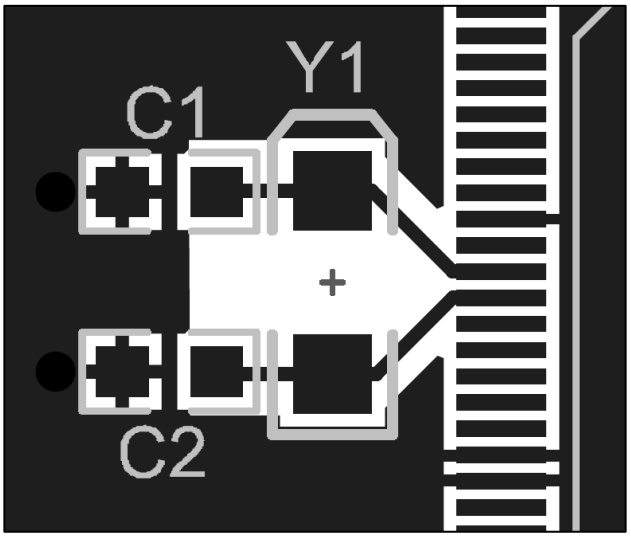
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32E501 series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



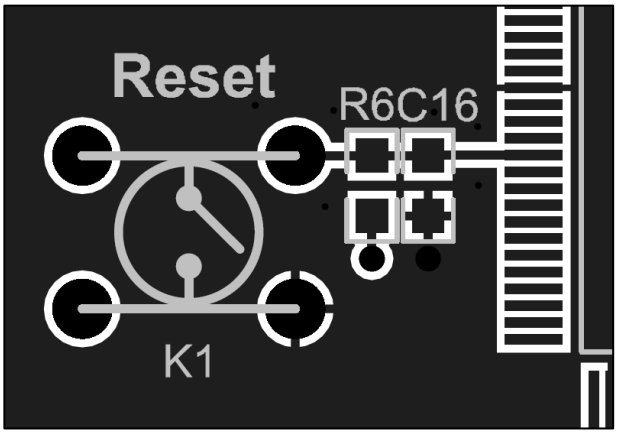
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design



Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better

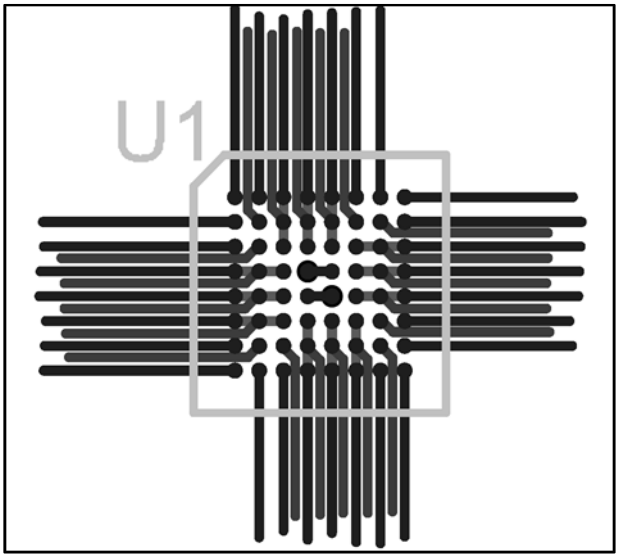
to wrap the NRST traces for better shielding effect.

3.4. BGA Circuit

GD32E501 series MCU has small-size BGA packaging, which needs to adopt high-density interconnected HDI board process, directly drill laser blind holes on the pad to fan out all signal lines, and it needs to do hole stacking process. If all pins need to be extracted, a 6-layer and 2-stage HDI board must be used. The Layout of a possible fan out method is as follows:

The recommended PCB wiring is as follows: laser blind hole Size: 4/10mil, inner mechanical hole Size: 8/16mil, and cable width: 4mil.

Figure 3-4. A BGA pin fan out method is recommended



4. Package Description

The GD32E501 series is available in one package form, BGA64

Table 4-1. Package Description

Ordering code	Package
GD32E501RxL7	BGA64(4x4, 0.4 pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.03, 2023
1.1	Update section 2.1.5 to provide all packaging power supply design drawings, explaining the connection of relevant pins within the chip.	Jun.21, 2023
1.2	Refine the content related to power supply detection and reset, and add Section 2.2.	Dec.15, 2024

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