GigaDevice Semiconductor Inc.

Device Limitations of GD32C2x1

Errata Sheet

Revision 1.0

(Jun. 2025)

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1. Introduction

This document applies to GD32C2x1 product series, as shown in ***Table 1-1. Applicable products***. It offers technical guidance for using GD32MCU and provides workaround to current device limitations.

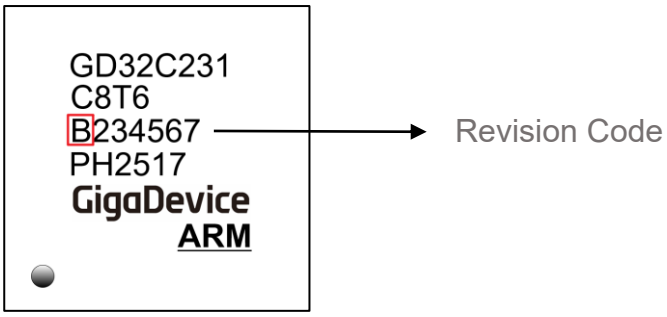
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32C221xx series
	GD32C231xx series

1.1. Revision identification

The device revision can be identified according to the mark on the top of the package. The 1st code on Line 3 of the mark is the product revision code, as shown in ***Figure 1-1. Device revision code of GD32C2x1***.

Figure 1-1. Device revision code of GD32C2x1



1.2. Summary of device limitations

The device limitations of GD32C2x1 are shown in ***Table 1-2. Device limitations***, please refer to Section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code B
PMU	*When the chip is powered on, the PORRSTF flag probability cannot be set*	Y
RCU	*The clock monitor of the HXTAL is abnormal*	Y
GPIO	*PA12 port LOCK function is abnormal*	Y
ADC	*ADC data acquisition error occurs when the ADC clock is much slower than the PCLK clock*	Y
I2S	*The I2S MCK clock output function is abnormal*	Y

Module	Limitations	Workaround
		Rev. Code B
I2C	***When I2C works in 7/10 address slave mode, receiving an abnormal timing will cause the SDA line to stuck***	Y

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. PMU

2.1.1. When the chip is powered on, the PORRSTF flag probability cannot be set

Description & impact

When the chip is powered on, the PORRSTF flag probability cannot be set, making it impossible to use the PORRSTF flag to detect whether a power-on reset has occurred.

Workarounds

During the application initialization phase, the code should first check whether a specified backup domain register (such as RTC_BKP0) contains a marked value (such as 0xA5). If it does not contain the marked value, it is considered that a power-on reset has occurred, and the software should then write the marked value to the backup domain register. Otherwise, it is considered that a power-on reset has not occurred. This method requires occupying one backup domain register.

2.2. RCU

2.2.1. The clock monitor of the HXTAL is abnormal

Description & impact

After the HXTAL clock monitor is enabled, when the HXTAL clock is lost, there is a probability that the NMI interrupt will not be generated. That is, the HXTAL clock monitor cannot reliably detect the loss of the HXTAL clock.

Workarounds

After enabling the HXTAL clock monitor function, the software polls the current clock source of the system to check whether a clock switch has occurred.

2.3. GPIO

2.3.1. PA12 port LOCK function is abnormal

Description & impact

When the PA12 port LOCK function is enabled, the CTL12 bit field in the GPIOA_CTL register

can still be configured, but the configuration result does not match expectations.

Workarounds

For the PA12 port, do not use the LOCK function. Or after enabling the LOCK function, ensure in software not to configure the CTL12 bit field in the GPIOA_CTL register.

2.4. ADC

2.4.1. ADC data acquisition error occurs when the ADC clock is much slower than the PCLK clock

Description & impact

When the ADC clock is much slower than the PCLK clock,the ADC_RDATA register is read immediately after the EOC is set and a data acquisition error occurs.

Workarounds

When the delay between reading EOC flag and reading ADC_RDATA is no more than two ADC clocks, after the EOC flag is set, software need to delay two ADC clocks before reading the ADC_RDATA register.

2.5. I2S

2.5.1. The I2S MCK clock output function is abnormal

Description & impact

When the I2S master clock output function (MCKOEN = 1) is enabled, the MCK clock cannot be output properly, which makes it impossible to provide clock input to devices that require an additional master clock.

Workarounds

Emulating MCK clock outputs by using timers to generate PWM signals. For specific implementation details, refer to the <11_I2S_Audio_Player> example in “GD32C2x1_Demo_Suites\GD32C231C_EVAL_Demo_Suites”.

2.6. I2C

2.6.1. When I2C works in 7/10 address slave mode, receiving an abnormal timing will cause the SDA line to stuck

Description & impact

When the I2C is operating as a slave device in 7-bit address mode and the I2C master simulates I2C communication via IO. If the master sends the following sequence, the I2C slave will enter an error state, causing it to malfunction and the SDA line to remain low:

Start + 10-bit Match Head Address + Start + 7-bit Address Read + Wait ACK + Start

When the I2C is operating as a slave device in 10-bit address mode and the I2C master simulates I2C communication via IO. If the master sends the following sequence, the I2C slave will enter an error state, causing it to malfunction and the SDA line to remain low:

Start + 10-bit Mismatch Head Address + Start
or
Start + 10-bit Match Head Address + Wait ACK + 10-bit Mismatch 8-bit Address + Start

Workarounds

Software periodically checks the status of the SDA line. If SDA is detected to be stuck low, reinitialize the I2C module.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jun.7 2025

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