GigaDevice Semiconductor Inc.

GD32F1 series of
ARM® Cortex®-M3 32-bit MCUs

Application Note
AN002

Table of Contents

List of Figures **2**

List of Tables **3**

1 Introduction **4**

2 Main features **4**

3 Function description **4**

3.1 On-chip Flash memory 4
3.2 Flash memory characteristics 8
3.3 In-Circuit Programming (ICP) 9
3.4 In-System Programming (ISP) 9
3.5 USART protocol of bootloader 9
3.6 Reading the Flash memory 10
3.7 Programming the Flash memory 10
3.8 Erasing the Flash memory 11
3.9 Option bytes features 13
3.10 Page protection 16

4 Revision history **17**

List of Figures

Figure 1. Flash programming flowchart 11
Figure 2. Flash page erase operation flowchart 12
Figure 3. Flash mass erase operation flowchart 13

List of Tables

Table 1. GD32F1 series product lines 4
Table 2. Flash module organization (GD32F10x4/6/8/B) 5
Table 3. Flash module organization (GD32F10xC/D/E/F/G/I/K) 5
Table 4. Flash module organization (GD32F1x0x4/6/8) 6
Table 5. System addr value and system memory size 6
Table 6. GD32F10x4/6/8/B and GD32F10xC/D/E/F/G/I/K Boot mode 7
Table 7. GD32F1x0x4/6/8 Boot modes 7
Table 8. Flash memory access latency 8
Table 9. Flash memory operation characteristics 8
Table 10. Bootloader supported peripherals 9
Table 11. USART parameters 9
Table 12. USART frame structure 10
Table 13. USART protocol command set 10
Table 14. GD32F10x4/6/8/B and GD32F10xC/D/E/F/G/I/K option bytes memory map 14
Table 15. GD32F1x0x4/6/8 option bytes memory map 15
Table 16. Revision history 17

1 Introduction

The Flash Memory Control Unit (FMCU) provides the on-chip Flash memory of GD32F1 device with all the necessary functions for routinely updated and re-programmed. Benefit from the Flash technology and innovative system architecture, the CPU waiting time which will cause CPU instruction execution delays has been eliminated and realized zero wait. Flash Memory operation as word/half-word program and page erase functions are also described in this document.

2 Main features

- Up to 3072 KB of on-chip Flash memory for storing instruction/data and options
- Page read accesses can be performed 32 bits per cycle with zero wait state
- Page erase and mass erase capability
- Word (32 bits) or Half-word (16 bits) program
- Interrupt function to indicate end of flash memory operations or an error occurs
- Page erase/program protection functions to prevent unwilling read/write operations on the Flash memory.

3 Function description

3.1 On-chip Flash memory

The GD32F1 series of devices provide up to 3072 KB of on-chip flash memory. The table below shows the product lines and relevant P/Ns. Read accesses can be performed 32 bits per cycle without any wait state. Besides, all of byte, half-word (16 bits) and word (32 bits) read accesses are supported. The flash memory can be programmed half-word (16 bits) or word (32 bits) at a time. Each page of the flash memory can be erased individually. The whole flash memory space except information blocks can be erased at a time. A data storage or firmware upgrade can be implemented using several methods such as In System Programming (ISP), In Application Programming (IAP) or In Circuit Programming (ICP).

Table 1. GD32F1 series product lines

Product lines	Product
Basic line	GD32F101xx
Mainstream line	GD32F103xx
Connectivity line	GD32F105xx GD32F107xx
Value line	GD32F130xx GD32F150xx

For GD32F10x4/6/8/B products that on-chip Flash up to 128KB, refer to below table for the module organization.

Table 2. Flash module organization (GD32F10x4/6/8/B)

Block		Name	Base addresses	Size (bytes)
Main memory	Flash (0 – 128KB)	Page 0	0x0800 0000 - 0x0800 03FF	1 KB
		Page 1	0x0800 0400 - 0x0800 07FF	1 KB
		…	…	…
		Page 127	0x0801 FC00 - 0x0801 FFFF	1 KB
Information block		System memory	**System addr** - 0x1FFF F7FF	
		Option bytes	0x1FFF F800 - 0x1FFF F80F	16B

For GD32F10xC/D/E/F/G/I/K products that on-chip Flash up to 256KB-3072KB, The Flash module is divided into two banks for management. Refer to below table for the module organization.

Table 3. Flash module organization (GD32F10xC/D/E/F/G/I/K)

Block		Name	Base addresses	Size (bytes)
Main memory	Bank 1 (0 - 512KB)	Page 0	0x0800 0000 - 0x0800 07FF	2 KB
		Page 1	0x0800 0800 - 0x0800 0FFF	2 KB
		…	…	…
		Page 255	0x0807 F800 - 0x0807 FFFF	2 KB
	Bank 2 (512 - 3072KB)	Page 256	0x0808 0000 - 0x0808 0FFF	4 KB
		Page 257	0x0808 1000 - 0x0808 1FFF	4 KB
		…	…	…
		…	…	…
		Page 895	0x082F EFFF - 0x082F FFFF	4 KB
Information block		System memory	**System addr** - 0x1FFF F7FF	
		Option bytes	0x1FFF F800 - 0x1FFF F80F	16B

For GD32F1x0x4/6/8 products that on-chip Flash up to 64KB, refer to below table for the module organization.

Table 4. Flash module organization (GD32F1x0x4/6/8)

Block		Name	Base addresses	Size (bytes)
Main memory	Flash (0 – 64KB)	Page 0	0x0800 0000 - 0x0800 03FF	1 KB
		Page 1	0x0800 0400 - 0x0800 07FF	1 KB
		…	…	…
		Page 64	0x0800 FC00 - 0x0800 FFFF	1 KB
Information block		System memory	**System addr** - 0x1FFF F7FF	
		Option bytes	0x1FFF F800 - 0x1FFF F80F	16B

The table below shows the beginning address of system memory that represented as system addr value.

Table 5. System addr value and system memory size

Products line	Products Num		System addr	Size (bytes)
Basic line Mainstream line	GD32F101xx GD32F103xx	Flash<768KB	0x1FFF F000	2 KB
		Flash>768KB	0x1FFF E000	6 KB
Connectivity line	GD32F105xx / GD32F107xx		0x1FFF B000	18 KB
Value line	GD32F130xx / GD32F150xx		0x1FFF EC00	3 KB

The GD32F10x4/6/8/B and GD32F10xC/D/E/F/G/I/K devices provide three kinds of boot sources which can be selected using the BOOT1 and BOOT0 pins. The values on the BOOT pins are latched on the 4th rising edge of SYSCLK after a reset. It is up to the user to set the BOOT1 and BOOT0 pins after a power-on reset or a system reset to select the required boot source. The details are shown in the following table.

Table 6. GD32F10x4/6/8/B and GD32F10xC/D/E/F/G/I/K Boot mode

Selected boot source	Boot mode selection pins	
	Boot1	Boot0
Main Flash Memory	x	0
System Memory	0	1
On-chip SRAM	1	1

The GD32F1x0x4/6/8 devices provides three kinds of boot sources which can be selected using the bit nBOOT1 in the user option byte and the BOOT0 pins. The value on the BOOT0 pin is latched on the 4th rising edge of SYSCLK after a reset. It is up to the user to set the nBOOT1 and BOOT0 after a power-on reset or a system reset to select the required boot source. The details are shown in the following table.

Table 7. GD32F1x0x4/6/8 Boot modes

Selected boot source	Boot mode selection pins	
	Boot1(1)	Boot0
Main Flash Memory	x	0
System Memory	0	1
On-chip SRAM	1	1

Note. 1: the BOOT1 value is the opposite of the nBOOT1 value.

After power-on sequence or a system reset, the ARM® Cortex®-M3 processor fetches the top-of-stack value from address 0x0000 0000 and the base address of boot code from 0x0000 0004 in sequence. Then, it starts executing code from the base address of boot code.

Due to the selected boot source, either the main flash memory (original memory space beginning at 0x0800 0000) or the system memory (original memory space beginning at 0x1FFF F000 or 0x1FFF EC00) is aliased in the boot memory space which begins at the address 0x0000 0000. When the on-chip SRAM whose memory space is beginning at 0x2000 0000 is selected as the boot source, in the application initialization code, you have to relocate the vector table in SRAM using the NVIC exception table and offset register.

The embedded boot loader is located in the system memory, which is used to reprogram the Flash memory. In GD32F1 devices, the boot loader can be activated through the USART and USB interface.

3.2 Flash memory characteristics

The table below shows the on-chip Flash memory access latency and operation characteristics

Table 8. Flash memory access latency

Block	Ranges	Base addresses	Size	Access Latency
Main memory	Page 0 ~ Page 127	0x0800 0000 - 0x0803 FFFF	256 KB	0
	Page 128 ~ Page 255	0x0804 0000 - 0x0807 FFFF	256 KB	1
	Page 256 ~ Page 895	0x0808 0000 - 0x082F FFFF	2560 KB	2

Table 9. Flash memory operation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{wait}	Read wait time	0 ~ 256 KB	-	-	0	nCLK
		256 ~ 512 KB	-	-	1	nCLK
		512 ~ 3072 KB	-	-	2	nCLK
t_{PROG}	16-bit / 32-bit programming time	0 ~ 256 KB	28	28.9	30	us
		256 ~ 512 KB				
		512 ~ 3072 KB				
t_{ERASE}	Page erase time	1 KB Page	100	300	500	ms
		2 KB Page				
		4 KB Page				
t_{MERASE}	Mass erase time	16 KB	-	-	1.2	s
		32 KB	-	-	2.4	s
		64 KB	-	-	4.8	s
		128 KB	-	1.8	9.6	s
		256 KB	-	1.3	9.6	s
		384 KB	-	-	14.4	s
		512 KB	-	2.2	19.2	s
		768 KB	-	-	16	s
		1024 KB	-	2.4	19.2	s
		2048 KB	-	-	32	s
		3072 KB	-	7.7	44.8	s

3.3 In-Circuit Programming (ICP)

GD32F1 MCU Flash memory can be programmed using standard JTAG and SWD protocol all the time. But GD32F130xx and GD32F150xx series of value line supports SWD only.

3.4 In-System Programming (ISP)

GD32F1 MCU embedded bootloader supports multi interfaces to update the Flash memory. There will be one or two USART ports, and standard USB port can be used on GD32F105xx and GD32F107xx connectivity line products.

Table 10. Bootloader supported peripherals

Products line	Products		Supported serial peripherals
Basic line Mainstream line	GD32F101xx GD32F103xx	Flash<768KB	USART1
		Flash>768KB	USART1 / USART2
Connectivity line	GD32F105xx		USART1 / USART2 / USB DFU
	GD32F107xx		USART1 / USART2 / USB DFU
Value line	GD32F130xx		USART1/USART2
	GD32F150xx		

3.5 USART protocol of bootloader

After system boot from bootloader by boot pin or boot bit, the bootloader is waiting for receiving the AutoBaudrate (0x7F) command, and using the Systick timer to get the baud rate of the ISP service program. Then bootloader send the ACK(0x79) to notify the ISP service program. It's ready to receive next command.

The checksum is used to ensure the safety of communication. The checksum byte is XOR of all previous bytes. So XORing the whole frame, the result must be 0x00.

Table 11. USART parameters

Parameter	Min	Type	Max	unit
Baud Rate	1200	9600	115200	bps
Data bit	-	8	-	bit
Stop bit	-	1	-	bit
Parity mode	-	Even Parity	-	-

Table 12. USART frame structure

Type	Command and Data Bytes	checksum
Length	>= 1 Byte	1 Byte
type	uint8_t	uint8_t

Table 13. USART protocol command set

Code	Command	Description
0x7F	AutoBaudrate	Auto baud rate detection
0x00	Profile	Gets the version and the allowed commands supported by the current version of the bootloader
0x01	Version & Protection Status	Gets the bootloader version and the Read Protection status of the Flash memory
0x11	Read Memory	Reads up to 256 bytes of memory starting from an address specified by the application
0x21	Jump to	Jumps to an address located in the Flash or SRAM
0x31	Program	Programs up to 256 bytes to the RAM or Flash memory starting from an address specified by the application
0x43	Erase_CMD1	Erases from one to all the Flash memory pages
0x44	Erase_CMD2	Erases from one to all the Flash memory pages using two byte addressing mode.
0x63	Program Protect	Enables the Program protection for special sectors
0x73	Program Unprotect	Disables the Program protection for all Flash memory sectors
0x82	Readout Protect	Enables the read protection
0x92	Readout Unprotect	Disables the read protection
0x79	ACK	Acknowledge
0x1F	NACK	Not acknowledge

3.6 Reading the Flash memory

The Flash memory access is performed through the AHB bus and can be addressed directly. Reading operation accesses the requested data of the content of the Flash memory by steps of read sequence, which under control of the hardware read interface in FMCU.

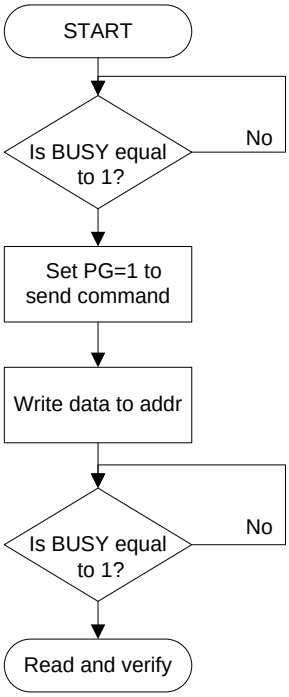
3.7 Programming the Flash memory

After system reset, the FMCU function is protected. There needs an unlocking sequence to write value into FLAG1 and FLAG2 of the FLASH_FMCUFR register to enable the FMCU function and access the FLASH_OCR register.

The GD32F103xx provides a word (32 bits) / half-word (16 bits) programming function which is used to modify the Flash memory contents at a time. The following steps show the half word programming operation register access sequence.

- Check the BUSY bit in the FLASH_OSR register to confirm that no Flash memory operation is in progress.
- Set the PG bit in the FLASH_OCR register to write the page program command
- Write the word (32 bits) / half-word (16 bits) data to the target address
- Wait until the operations have been completed by checking the reset of the BUSY bit in the FLASH_OSR register
- Read and verify the programmed page

Figure 1. Flash programming flowchart



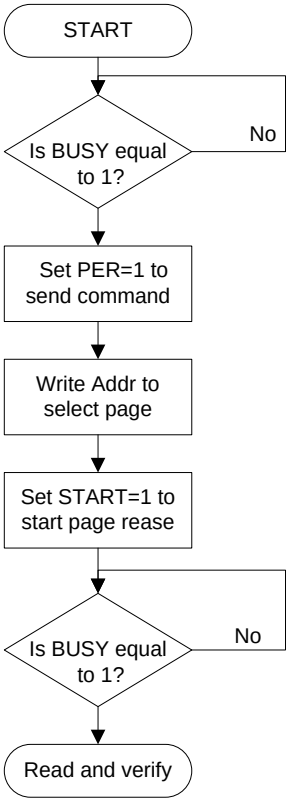
3.8 Erasing the Flash memory

3.8.1 Page erase

A page of the Flash memory can be erased using the Page Erase feature of the FMCU. Each page can be erased independently without affecting the contents of other pages. The following steps show the access sequence of the register for a page erase operation.

- Check the BUSY bit in the FLASH_OSR register to confirm that no Flash memory operation is in progress.
- Set the PER bit in the FLASH_OCR register to write the page erase command
- Write the FLASH_TAR register to select page of which to be erased
- Set the START bit in the FLASH_OCR register to trigger the erase operation
- Wait until the operations have been completed by checking the reset of the BSY bit in the FLASH_OCR register
- Read and verify the erased page

Figure 2. Flash page erase operation flowchart

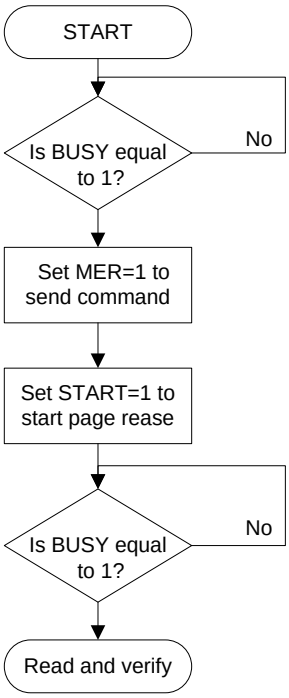


3.8.2 Mass erase

The user pages of the Flash memory can also be completely erase using the mass erase function. The following steps show the mass erase register access sequence.

- Check the BUSY bit in the FLASH_OSR register to confirm that no Flash memory operation is in progress.
- Set the MER bit in the FLASH_OCR register to write the mass erase command
- Set the START bit in the FLASH_OCR register to trigger the erase operation
- Wait until the operations have been completed by checking the reset of the BSY bit in the FLASH_OCR register
- Read and verify the erased page

Figure 3. Flash mass erase operation flowchart



3.9 Option bytes features

The option byte block can be treated as an independent Flash memory in which the base address is 0x1FFF F800. The following table shows the functional description and the memory map of the option byte.

Table 14. GD32F10x4/6/8/B and GD32F10xC/D/E/F/G/I/K option bytes memory map

Address	Name	Description
0x1FFF F800	OB_RDPT	option byte Security Protection value 0xA5 : no security protection any value except 0xA5 : under security protection
0x1FFF F801	OB_RDPT_N	OB_RDPT complement value
0x1FFF F802	OB_USER	[7:4]: reserved [3]: BFB2 0: boot from bank2 or bank1 if bank2 is void, when configured boot from main memory 1: boot from bank1, when configured boot from main memory [2]: OB_STDBY_RSTn 0: generator a reset instead of entering standby mode 1: no reset when entering standby mode [1]: OB_DEEPSLEEP_RSTn 0: generator a reset instead of entering Deep-sleep mode 1: no reset when entering Deep-sleep mode [0]: OB_WDG_SW 0: hardware independent watchdog 1: software independent watchdog
0x1FFF F803	OB_USER_N	OB_USER complement value
0x1FFF F804	OB_DATA[7:0]	user defined data bit 7 to 0
0x1FFF F805	OB_DATA_N[7:0]	OB_DATA complement value bit 7 to 0
0x1FFF F806	OB_DATA[15:8]	user defined data bit 15 to 8
0x1FFF F807	OB_DATA_N[15:8]	OB_DATA complement value bit 15 to 8
0x1FFF F808	OB_WP[7:0]	Page Erase/Program Protection bit 7 to 0 0: protection active 1: unprotected
0x1FFF F809	OB_WP_N[7:0]	OB_WP complement value bit 7 to 0
0x1FFF F80A	OB_WP[15:8]	Page Erase/Program Protection bit 15 to 8
0x1FFF F80B	OB_WP_N[15:8]	OB_WP complement value bit 15 to 8
0x1FFF F80C	OB_WP[23:16]	Page Erase/Program Protection bit 23 to 16
0x1FFF F80D	OB_WP_N[23:16]	OB_WP complement value bit 23 to 16
0x1FFF F80E	OB_WP[31:24]	Page Erase/Program Protection bit 31 to 24 OB_WP[30:0]: Each bit is related to 4KB flash protection, that means 4 pages for GD32F10X_MD and 2 pages for GD32F10X_HD, GD32F10X_XD and GD32F10X_CL. Bit 0 configures the first 4KB flash protection, and so on. These bits totally controls the first 124KB flash protection. OB_WP[31]: Bit 31 controls the protection of the rest flash memory.
0x1FFF F80F	OB_WP_N[31:24]	OB_WP complement value bit 31 to 24

Table 15. GD32F1x0x4/6/8 option bytes memory map

Address	Name	Description
0x1FFF F800	OB_RDPT	option byte Security Protection value 0xA5 : no protection any value except 0xA5 or 0xCC : protection level low 0xCC : protection level high
0x1FFF F801	OB_RDPT_N	OB_RDPT complement value
0x1FFF F802	OB_USER	option byte which user defined [7]: reserved [6]: OB_SRAM_PARITY_CHECK 0: enable sram parity check 1: disable sram parity check [5]: OB_VDDA_VISOR 0: disable VDDA monitor 1: enable VDDA monitor [4]: OB_BOOT1_n 0: BOOT1 bit is 1 1: BOOT1 bit is 0 [3]: reserved [2]: OB_STDBY_RSTn 0: generator a reset instead of entering standby mode 1: no reset when entering standby mode [1]: OB_STOP_RSTn 0: generator a reset instead of entering stop mode 1: no reset when entering stop mode [0]: OB_WDG_SW 0: hardware windows watchdog 1: software windows watchdog
0x1FFF F803	OB_USER_N	OB_USER complement value
0x1FFF F804	OB_DATA[7:0]	user defined data bit 7 to 0
0x1FFF F805	OB_DATA_N[7:0]	OB_DATA complement value bit 7 to 0
0x1FFF F806	OB_DATA[15:8]	user defined data bit 15 to 8
0x1FFF F807	OB_DATA_N[15:8]	OB_DATA complement value bit 15 to 8
0x1FFF F808	OB_WP[7:0]	Page Erase/Program Protection bit 7 to 0
0x1FFF F809	OB_WP_N[7:0]	OB_WP complement value bit 7 to 0
0x1FFF F80A	OB_WP[15:8]	Page Erase/Program Protection bit 15 to 8
0x1FFF F80B	OB_WP_N[15:8]	OB_WP complement value bit 15 to 8

3.10 Page protection

The GD32F1 device provides page erase/program protection functions to prevent unwilling read/write operations on the Flash memory.

3.10.1 Read protection

Read protection is enabled by setting the OB_RDPT option byte and need a power on reset to reload the new OB_RDPT option byte after that.

Read protection is disabled by erasing the entire option byte area and program the correct relevant OB_RDPT code (described in the user manual) to the unprotect memory, then need a power on reset to reload the new OB_RDPT option byte after that.

3.10.2 Write protection

Write protection is enabled by configuring the OB_WP option bytes, and need a power on reset to reload the new OB_WP option bytes after that.

Write protection is disabled by erasing the entire option byte area using the OBER bit in the FMC_CSR register and program the correct OB_WP code which described in the user manual to the unprotect memory, then need a power on reset to reload the new OB_WP option byte after that.

4 Revision history

Table 16. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.8, 2013
2.0	New product lines updated	Jun.20, 2014
3.0	New product lines updated	Jan.20, 2015